Trap-induced Apparent Linearity of CNTFETs

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ABSTRACT

Charge trapping effects are observed in non-pulsed DC and AC measurements of CNTFETs with time constants in the range of 1 ms to 100 s. A compact model is discussed that qualitatively matches pulsed and non-pulsed measurements. The model predicts the apparent linearity seen in non-pulsed AC measurements of trap-affected CNTFETs. This apparent linearity is a result of trapping processes and cannot be exploited in circuits for e.g. mobile communication systems. A characterization technique is proposed that reveals the trap-free characteristics of CNTFETs enabling a realistic performance evaluation and projection of CNTFET technologies.

Keywords: CNTFET, hysteresis, compact model, traps, linearity, electrical characterization

1 INTRODUCTION

Compared to conventional bulk semiconductors, carbon nanotube (CNT) field-effect transistors (FETs) possess a number of properties which may make CNTFET technologies superior for certain applications [1]. In particular, the one-dimensional transport in CNTs leads not only to a low scattering rate and high current carrying capability but also to a linear relation between drain current and input (gate-source) voltage under specific conditions [2], [3]. This linearity is expected to be beneficial for e.g. mobile communication systems [1].

Currently, one of the major issues of these technologies are trap centers in the channel which can strongly impact the electrical behavior of the device and significantly worsens the applicability of these technologies. In addition, depending on the measurement technique, traps can either conceal a possible inherent linearity [4] or can lead to an experimentally observed apparent linearity [5] which can not be exploited in circuits.

A schematic cross-section of the CNTFETs analyzed here is shown in Fig. 1. The transistors consist of approximately 3000 semiconducting and metallic CNTs in parallel which were grown on-wafer in a CVD process. The channel length is 800 nm with a gate length of 350 nm. Details of the technology can be found in [6].

Trap centers are present in several areas of the device, which are indicated in Fig. 1. Depending on the nature of the trap, the capture and emission of carriers occurs over a wide range of time constants [7], [8].

Short capture and emission times are expected for *interface traps* (a) [9] due to e.g. Silanol groups at the SiO_2 surface [10] as well as water molecules [11] or dirt on the CNT. Short capture and long emission times are expected for *oxide defects* (b) in the SiO_2 and HfO_2 close to the CNTs. *Deep oxide defects* (c) are expected to be characterized by long capture and emission times [12]. The large range of capture and emission times has a huge impact on the experimental results, making consistent device characterization a difficult task.

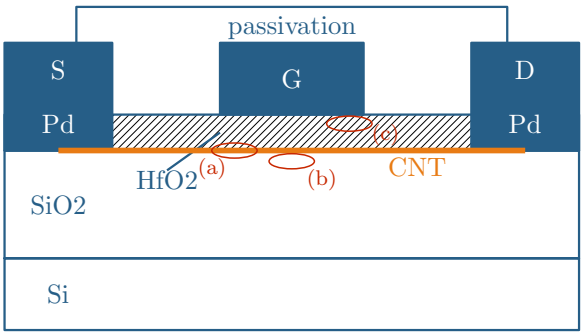

Fig. 1: Schematic cross-section of a top-gate CNTFET. Typical trap areas are indictated: (a) interface traps, (b) oxide defects close to the CNTs, and (c) deep oxide defects.

Although it has been shown that trap effects can be eliminated by optimized materials and growth procedures [9] it may take quite a while for wafer-scale processes to reach a point where the devices are completely free of trap effects. Thus, models for circuit design are required that can predict the behavior of the trap-affected device behavior for several reasons: (*i*) The behavior of trap-affected devices in circuits can be predicted. (*ii*) A trap model can help defining the measurement conditions needed to characterize the trap-free device behavior which is needed for technology evaluation and modeling purposes. (*iii*) The model also helps to understand experimental observations such as the apparent linearity [5] of CNTFETs that has been observed in non-pulsed AC measurements.

2 MEASUREMENT TECHNIQUES

For the experimental characterization of traps in CNTFETs, several measurement techniques are employed: (*i*) non-pulsed DC and AC measurements, and (*ii*) pulsed DC and AC measurements with either narrowband (NB) or wideband (WB) detection.

Non-pulsed measurements are characterized by a staircase voltage sweep with step lengths in the range of several milliseconds. Fig. 2a shows a sketch of the input voltage and output current over time of such a staircase sweep. The measurement window where the actual measurement of the current takes place is usually placed towards the end of the step where a steady-state current is expected. However, for the devices studied here and the typically used step lengths of several milliseconds, the measured current does not reach its steady-state value as indicated in Fig. 2a. In non-pulsed AC measurements, a sine wave with a small amplitude is superimposed over the DC signal.

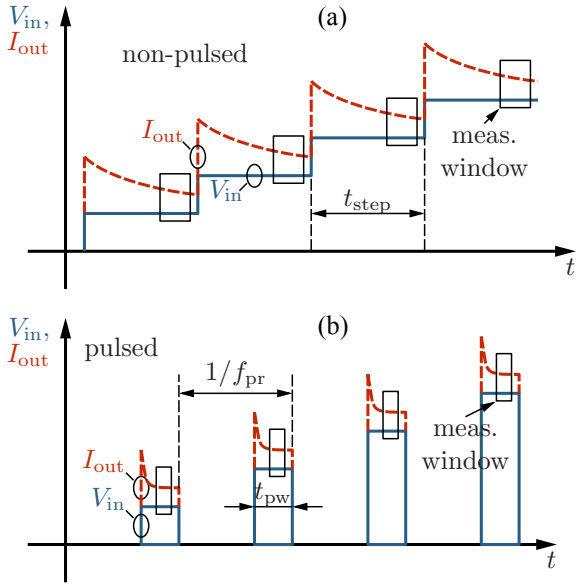

Fig. 2: Input voltage and output current over time for (a) non-pulsed and (b) pulsed measurements.

Pulsed measurements (see Fig. 2b) are characterized by very short pulses of as low as 100 ns pulse width and very long intervals of up to 100 ms between the pulses. If the time constants associated with trap charging are much larger than the pulse width, the measurement during the pulse is hardly affected by traps and the current reaches a constant value. For the studied CNTFETs a constant current is reached after a transient response of typically a few hundred nanoseconds. Due to the observed region of constant current during the pulse and due to the good thermal conductivity of CNTs, we expect self-heating effects to be much faster than the measurement pulse and therefore to be negligible. The main difference between narrowband and wideband detection is which part of the measured spectrum of a signal is evaluated (see Fig. 3) [13]. The spectrum is the result of the convolution of the rectangular DC pulse with the sinusoidal AC signal. It consists of discrete frequency components that have a magnitude of

$$P = \left| sinc((f - f_0) \cdot t_{pw}) \right| \quad (1)$$

with the frequency f_0 of the AC signal and the DC pulse width t_{pw}. Thus, the signal power is distributed across the various frequency components in the spectrum. The distance between neighboring frequency components is equal to the repetition frequency f_{pr} of the DC pulses, which is given by the duty cycle D and t_{pw} through

$$f_{pr} = \frac{D}{t_{pw}}. \quad (2)$$

For wideband detection, the measured signal power results from an integration over (ideally) the entire spectrum. The advantage is that no power is lost leading to a high dynamic range (the ratio of the largest to the smallest measurable signal). However, the spectrum can only be evaluated within the bandwidth of the network analyzer (NWA). A very short pulse width may spread the spectrum too wide for the receiver to measure it completely. The available receiver bandwidth therefore limits the minimum pulse width. For the NWA used in our experiments the minimum pulse width would be 100 ns. However, the minimum pulse width is already limited to 500 ns by the used DC pulse system. The duty cycle is limited by the DC pulse system's minimum f_{pr} of 10 Hz which results in a minimum duty cycle of 0.001 % for a pulse width of 1 µs.

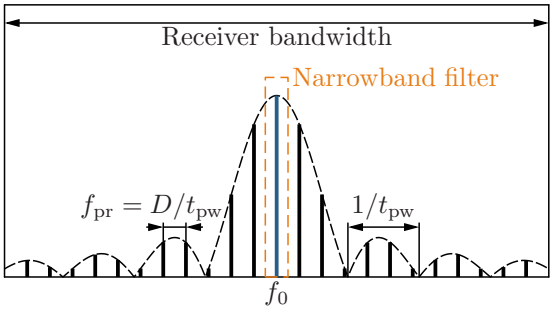

Fig. 3: Schematic frequency domain view of a pulsed RF signal (adapted from [13]).

For narrowband detection, all but the central frequency component at f_0 are filtered out. This means that only a fraction of the available power can be measured which reduces the dynamic range significantly. Additionally, the neighboring frequency components must be filtered out completely which is only possible if they have a certain distance. Since their distance is governed by (2), a sufficiently large duty cycle or small pulse width is required. At a pulse width of 1 µs the minimum duty cycle is limited to 1 % for the narrowband NWA used in this work.

3 EXPERIMENTAL OBSERVATIONS

The large range of capture and emission times leads to a **step response** (see Fig. 4) that can span many decades of time. For the tested device, the current does not reach a steady-state even after 100 s, which can be explained with a continuous capturing of electrons during a measurement step. This leads to a gradual shielding of the tube from the gate, which constantly changes the tube potential and, thus, the current. The wide time span of the step response can be explained by a combination of different trap time constants from microseconds up to seconds [7], [8].

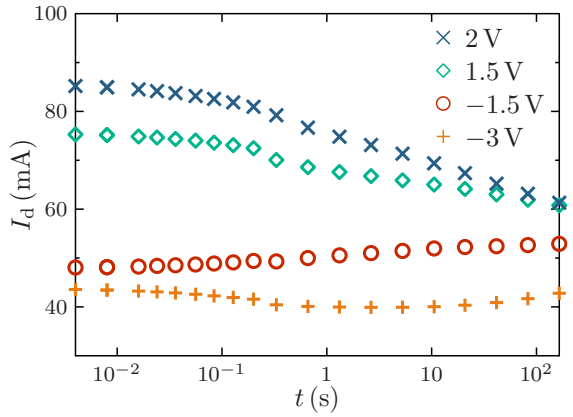

Fig. 4: Measured step response of the drain current for a step at t=0 from (V_{GS}=0V, V_{DS}=0V) to V_{DS}=2V and various V_{GS}.

In a typical *non-pulsed* setup, **transfer characteristics** of a transistor are measured with a staircase voltage sweep (see Fig. 2a). Since typical step sizes are in the range of several milliseconds, electrons are captured. Hence, the current is trap-affected and depends significantly on the measurement history (i.e. the actual trap state). If a transfer characteristic is measured with a non-pulsed forward and backward sweep of the gate voltage, the current measured with the backward sweep does not match the current of the forward sweep leading to a hysteresis as shown in Fig. 5.

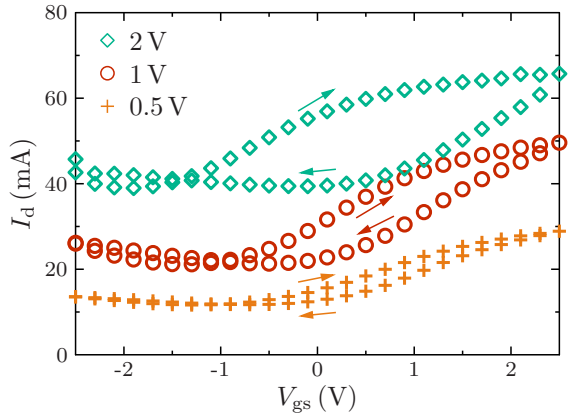

Fig. 5: Measured transfer characteristics in non-pulsed mode for several drain voltages. The gate voltage was swept forwards and backwards consecutively.

Obviously, the hysteresis is more pronounced for higher drain voltages.

The hysteresis is not apparent in pulsed measurements if the pulse width is well below the time constant of the traps' charging process. The resulting transfer characteristics, hence, differ strongly from non-pulsed measurements (see Fig. 9).

In *pulsed* measurements, two parameters, the pulse width and the duty cycle are important. The impact of both on the hysteresis width V_{hyst} is shown in Fig. 6. The hysteresis width is measured as the difference of the threshold voltages of the forward and backward path. The threshold voltages are extracted by means of the Y-function method [14]. If the pulse width t_{pw} is changed from 500 ns to 2 µs, there is only a slight difference in V_{hyst} since t_{pw} is much smaller than the trap time constants. However, a change in duty cycle from 0.1 % to 0.001 % reduces V_{hyst} considerably.

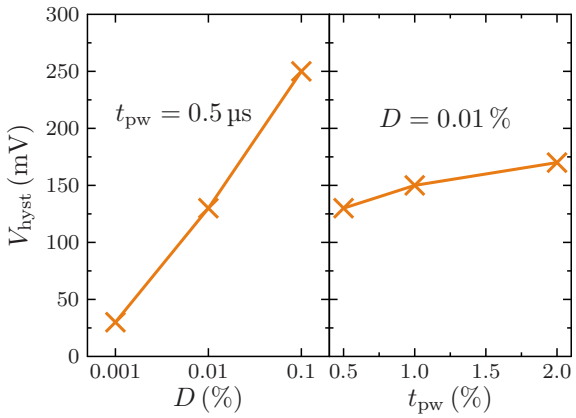

Fig. 6: Measured hysteresis width V_{hyst} as a function of (left) duty cycle and (right) pulse width for V_{DS}=2V.

If a measurement is trap-affected, another effect that can be observed in pulsed and non-pulsed measurements is an inconsistency between DC and AC measurements. This is apparent in a comparison of the **transconductance**, g_m, extracted from the DC transfer characteristics,

$$g_{m,\,DC} = \frac{\Delta I_D}{\Delta V_{GS}}, \tag{3}$$

and from the AC Y-parameters,

$$g_{m,\,AC} = \Re\{Y_{21} - Y_{12}\}. \tag{4}$$

$g_{m,DC}$ is calculated from the DC current of two measurements for different gate voltages that are close together. In case of a device with trap centers, the result will be strongly affected by the trap states (i.e. the measurement history) of the two measurements. The AC measurement, however, which is performed at high frequencies, is not affected by the traps due to the large time constants associated with the traps.

Fig. 7 shows experimental results for the transconductance of a device measured with a constant pulse width of 1 µs and two different duty cycles of 1 % and 0.001 %. While narrow band detection only allows a duty cycle down to 1 %, a VNA enabling wideband detection was employed for the extraction of $g_{m,AC}$ from measurements with a duty cycle of 0.001 %. The experimental results of $g_{m,DC}$ and $g_{m,AC}$ are in a good agreement for a duty cycle of 0.001 % and, thus, can be assumed not to be trap-affected (i.e. trap-free). However, for a duty cycle of 1 %, $g_{m,DC}$ is lower than $g_{m,AC}$ for high V_{DS}. As can be seen in Fig. 7, a duty cycle of 1% leads to a significant trap-induced threshold voltage shift.

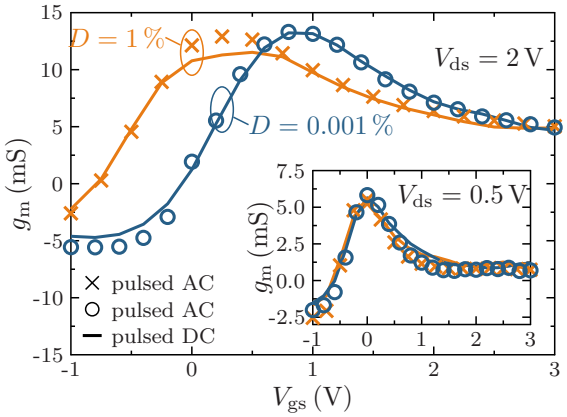

Fig. 7: Transconductance from pulsed measurements for several drain voltages: $g_{m,DC}$ (solid lines) and $g_{m,AC}$ from measurements with a D of 1 % (x) and $g_{m,AC}$ from measurements with a D of 0.001 % (o).

It can be concluded that for trap-free characterization purposes pulsed measurements are necessary as they can reveal the trap-free characteristics of a CNTFET. Two parameters are important: pulse width and duty cycle. The pulse width must be much smaller than the time constants of the trapping processes so that as few charges as possible are trapped during the pulse. The duty cycle has to be very low and therefore the time between the pulses is very long so that the charges that were trapped during a pulse are released (i.e. to delete the measurement history). For the devices analyzed here, pulsed measurements with a pulse width of 1 µs and a duty cycle of 0.001 % are sufficient to characterize the trap-free device behavior. However, for these low duty cycles, pulsed AC measurements must be performed with wideband detection.

4 TRAP MODEL

An empirical approach that has been used for modeling self-heating effects [15] was adapted to model the impact of traps. It uses the RC ladder network shown in Fig. 8. Capture and emission of traps corresponds to charging and decharging of the network's capacitors. The number n of network elements is typically around 4. The trap voltage V_{tr}, which is the difference of the tube potential with and without trapped charges, is determined by the RC ladder network.

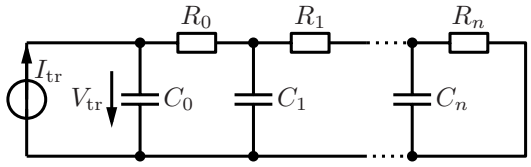

Fig. 8: Adjunct trapping network, I_{tr} is defined by (6).

The trap-free behaviour of the multi-tube transistors analyzed here is modeled with the semi-empirical transistor model published in [16]. The trap voltage V_{tr} is incorporated into this model as a threshold voltage shift,

$$I_D = f(V_{GS} + V_{tr}) . \tag{5}$$

The trap current, which determines the steady-state value $V_{tr,SS}$ of the trap voltage, is modeled by an empirical function

$$I_{tr} = a \cdot V_{GS} + b \cdot V_{DS} \cdot V_{GS} + c , \tag{6}$$

with the parameters a, b and c which can be fitted to the step response measurements. The release of trapped carriers is expected to occur with different time constants than the filling of traps. This is so far not included in the proposed model and left for future work.

5 COMPARISON OF MODEL TO MEASUREMENTS

A possible parameter extraction method is briefly summarized in the following. The semi-empirical model [16] of the internal transistor without traps can be fitted to pulsed measurements as they are unaffected by trapping effects. The network elements of the trapping network shown in Fig. 8 and the trap current parameters are fitted to the step response measurements shown in Fig. 4. The steady-state value of the step response before and after the step is fitted with the parameters of (6). The resistances in Fig. 8 are chosen so that their sum equals 1. The steady-state value $V_{tr,SS}$ of the trap voltage can then be expressed as

$$V_{tr,SS} = I_{tr} \cdot \sum_i R_i = I_{tr} . \tag{7}$$

Inserting (7) into (5) results in the steady-state drain current

$$I_{D,SS} = f(V_{GS} + a \cdot V_{GS} + b \cdot V_{DS} \cdot V_{GS} + c) . \tag{8}$$

From (8) the trap current parameters can be determined if steady-state values of the current are measured for different step responses. The capacitances in Fig. 8 determine the shape of the step response. The experimental results shown in this section are all from the same device and the simulations were done with one single set of parameters.

Fig. 9 shows a comparison between experimental results and simulations of the transfer characteristics. The simulation results for the non-pulsed measurements are extracted from transient simulations where charging and de-charging of traps are considered. For these simulations, the time-dependent input voltages mimic the staircase sweeps in the experiments with the same step length and measurement window.

Compared to the pulsed measurements, the non-pulsed measurement results are stretched along the x-axis as a consequence of the trap effects. Additionally, the drain current stays almost constant for high gate and drain voltages in the non-pulsed measurements and in the related simulations as shown in Fig. 9. Trap effects lead to a change of the charging current I_{tr} and a decrease of V_{tr}, which balances the increasing gate voltage. This corresponds to an almost constant tube potential and thus an almost constant current.

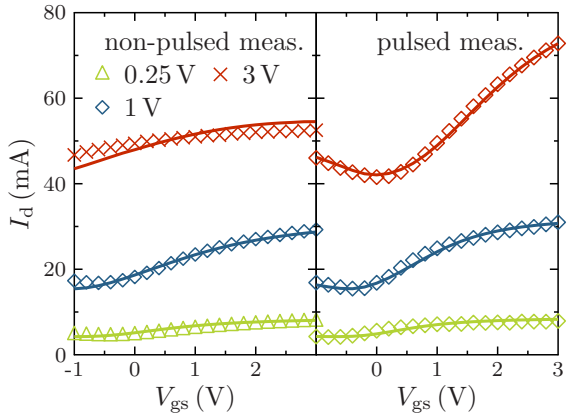

Fig. 9: Left: Transfer characteristics for various V_{DS} from non-pulsed standard measurements (symbols), simulation of non-pulsed measurements (lines) Right: pulsed measurements (symbols), and simulation of pulsed measurements (lines).

A simulation of the pulsed measurements is acquired by a DC simulation of the model without trapping network (as long as the pulsed measurements are trap-free). As can be seen in Fig. 9 both pulsed and non-pulsed DC measurements are correctly reproduced by the model.

Fig. 10 shows a comparison of the corresponding transconductances. For non-pulsed AC measurements, a very broad and constant peak is caused by the trap effects which could be interpreted as a very linear $I_D(V_{GS})$ relation. This apparent linearity is just a consequence of the trap effects and can be explained as follows: As discussed before, the tube potential stays almost constant in a non-pulsed measurement for an increasing gate voltage at high drain voltage leading to an almost constant tube potential. AC signals, however, are fast enough and, thus, directly change the tube potential. Hence, the non-pulsed AC response for consecutive gate voltages corresponds to the AC response of the same internal bias point (i.e. the same tube potential). If the AC response (e.g. g_m) is plotted against V_{GS}, it is almost constant for high V_{GS} and V_{DS} as can be seen in Fig. 10.

The transconductance from pulsed measurements, which correspond to trap-free data, has a very different shape. Fig. 10 also shows $g_{m,DC}$ from non-pulsed measurements which has no resemblance with the $g_{m,AC}$ results of pulsed and non-pulsed measurements. As a consequence, these devices should always be characterized in pulsed mode and with very low duty cycles which makes wideband detection indispensable. As confirmed by the trap model, the trap-effect free characteristics are revealed. The main differences in g_m from non-pulsed measurements compared to pulsed measurements, i.e. the apparent linearity and a threshold voltage shift, are qualitatively reflected in the simulations. The simulation of the non-pulsed AC measurements was achieved by performing a transient simulation at the DC operating points and saving the trap states (V_{tr}) for every operating point. A standard AC simulation was then performed with the model without trapping network but with the pre-computed V_{tr}.

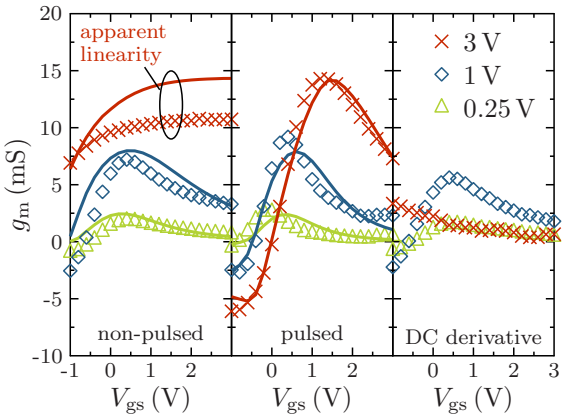

Fig. 10: Transconductance $g_{m,AC}$ vs. V_{GS} for various V_{DS}. Left: from non-pulsed (standard) AC measurement (symbols), simulation of standard measurement conditions (lines). Center: from pulsed DC measurement (symbols), simulation of pulsed measurement (lines). Right: $g_{m,DC}$ from non-pulsed measurements.

6 CONCLUSION

The understanding and modeling of trap effects has serious implications on CNTFET fabrication, characterization and circuit design.

It has been shown that trap effects lead to a step response with changing current of the CNTFET that spans several decades of time. In addition trap effects can lead to a strong hysteresis in the transfer characteristics from non-pulsed measurements. The results of non-pulsed measurements depend strongly on measurement parameters and can show an apparent linearity that is caused by the trap effects. This apparent linearity cannot be exploited in circuits. In a typical HF circuit, the HF behavior of the device is trap-free as the

circuit is operated at frequencies that are much faster than the time constants of the trap effects. However, this is only the case after the trap-affected DC operating point of the circuit has reached a steady state. For the devices studied here it can take several 100 s.

A characterization technique has been proposed that reveals the trap-free device behavior. This is possible with DC pulses of 1 µs pulse width and 0.001 % duty cycle combined with AC measurements with wideband detection.

A trap model was developed that can qualitatively reproduce experimental results that are affected by trap effects. Modeling of different capture and emission times of traps is left for future work.

7 APPENDIX

DC and AC measurements for non-pulsed operation were performed with a semiconductor parameter analyzer HP4142 and a vector network analyzer PNA 8361C controlled with Agilent's IC-CAP software.

The pulsed DC measurements were performed with the Auriga Microwave pulsed IV/RF system AU4550 in combination with different PNAs. The narrowband pulsed AC measurements were performed with an Agilent E8361C PNA network analyzer with a pulse width of 1 µs, a duty cycle of 0.95 % and an IF bandwidth of 50 Hz.

The wideband pulsed AC measurements were performed with an Agilent PNA-X 5247A with a pulse width of 1 µs and a duty cycle of 0.001 %.

Diplexers SHF DX65 (0.8-65 GHz) were used for the pulsed bias supply and separation from the RF measurement path. RF ground-signal-ground probes 1MX 67V3N GSG100 with a semiautomatic probe station PA200 from Cascade Microtech were employed to contact the pads of the DUT.

8 ACKNOWLEDGEMENT

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