A Threshold Voltage Modeling for A Spacer-Trapping Memory Cell Using Verilog-A

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ABSTRACT

The threshold voltage of the flash memories varies with respect to the applied voltages at the respective terminal of a memory cell. This paper presents the modeling of the threshold voltage variation for an embedded spacer-trapping memory cell. The effects such as velocity saturation of the transistor and the band-to-band tunneling mechanism have been incorporated in the model. The proposed memory model has been simulated in a standard 0.18 μm CMOS technology. The output results of the proposed model using Verilog-A shows 94.9 ms of erasing time for the programing time of 33.4 ms and for a memory speed of 10 kHz. An increment of 930 mV of the threshold voltage during the programming mode has been recorded.

Keywords: EEPROM memory characteristics simulation, MOS capacitance characteristics, non-volatile memory, tunneling.

1 Introduction

The non-volatile memory (NVM) becomes an important circuit block in the past decade. In literature [1–3], various types of flash memories have been discussed as a promising field of invention. The sidewall-flash (S-Flash) memory is an embedded NVM, available in small or medium volume, few time programmable and a cheap alternative to the SONOS, the EPROM and the NROM. The SONOS, the EPROM and the NROM are intended for storing large amounts of data (greater than 1 MB). Nevertheless, many applications require the storage capacity from a single byte to hundreds of kilobytes. The complexity of the process increases for the embedded NVM block into CMOS.

In [4–6], the flash memory cell for the DC analysis and transient analysis has been modeled. Ref. [6] developed the compact model for the floating gate memories using PSP transistor models [7]. This paper presents the behavioral model for the S-Flash memory cell, including the threshold voltage variation. The model has been implemented using a hardware descriptive language (HDL) viz. Verilog-A. During the programming and the erasing mode, the resulting threshold voltage of an S-Flash memory cell varies with respect to the available amount of charge trapped inside the spacer. The channel hot electrons (CHE) [8] and Fowler-Nordheim [9] injection current equations enable the programming or the erasing operations in order to perform the transient analysis. The model includes velocity saturation of the transistor and the tunnelling mechanism. The proposed memory model can be further used in the standard design flow tools such as Cadence Spectre and Eldo.

The paper has been organized as follows. Sect. 2 explains the working principle of an S-Flash memory cell. Sect. 3 explains the modeling equations used to model the program and the erase mode of the memory cell. Section. 4 is the simulated results of the modeled memory and sect. 5 summarizes the paper with conclusions.

2 The Working principle of S-Flash

Figure 1 shows the cross sectional view of an S-Flash memory cell transistor. The spacer in the nMOS transistor acts as a programming media. The spacer is made of silicon nitride which is a material with high density of deep electron traps [10]. The silicon nitride spacer is a material with high density of deep electron traps. The threshold voltage (V_{th}) of the transistor is increased or decreased with respect to injected charge into the spacer regions. The working of the memory cell is divided into three mode operations i.e., the program, the read and the erase mode. The different modes are operated through the extra circuitry feed to four terminals of the memory cell. In general, the programming mode is a fast operation of about microseconds, whereas the erasing mode is a slow operation of about milliseconds.

During the program mode of operation, the transistor experiences the channel hot electrons (CHE) injection mechanism. The use of high voltages at the gate and the drain terminal of the transistor allows transistor to be in the strong inversion mode. The source and the body terminal are connected to the ground potential. During the programming mode, the hot electrons are available in the pinch-off region of an nMOS S-Flash memory cell. These hot electrons have sufficient kinetic energy to cross the potential barrier of the SiO_2. Moreover, the channel hot electrons generate the electron-hole pairs due to impact ionization in the channel region. The generated holes drift towards the substrate

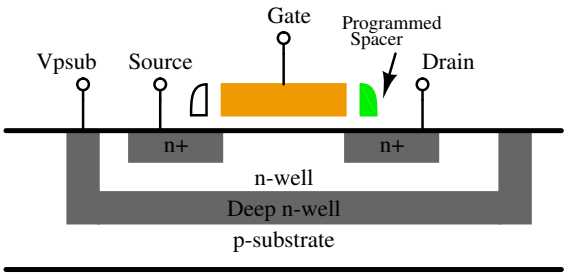

Figure 1: The cross sectional view of an S-Flash memory cell transistor.

contact. Hence, the CHE mechanism contributes to the drain current, in opposite direction of the electron flow. The CHE current can be monitored by measuring the substrate current. Because of trapping of charges, the threshold voltage is increased as shown in equation (1). The new threshold voltage during the program mode ($V_{th,new}$) can be expressed as:

$$V_{th,new} = V_{th} + \frac{Q_T}{\alpha}, \qquad (1)$$

where Q_T is the trapped charges in the spacer and α is the small signal capacitance between the drain and the gate terminal. Because of increased trapped charges in the spacer, threshold voltage increases.

During the read mode of operation, the memory element stays as a stand by mode with the voltages at the gate terminal is connected to the supply voltage of the circuit, keeping the drain voltage grounded. During the read mode the programmed bit is available to read at the input of the sense amplifier. The threshold voltage in the read mode stays at the initial threshold voltage i.e. at V_{th}.

The trapped charges can be erased by applying negative voltage at the gate terminal of the transistor. During the erase mode of operation, the trapped charges are erased using the band-to-band (BTB) tunneling mechanism. Because of trapping of charges, the threshold voltage is decreased as shown in equation (1). The new threshold voltage during the erase mode ($V_{th,new}$) can be expressed same as equation (1). However, because of decreased amount of trapped charges in the spacer, threshold voltage decreases. The spacer charge during the erase mode depends on the band-to-band tunneling current. The tunneling current (i_{TUN}) can be written as:

$$i_{TUN} = A \cdot S_{TUN} \cdot E_{TUN}^2 \cdot exp\left(-\frac{B}{E_{TUN}}\right), \qquad (2)$$

where E_{TUN} ($= v_{TUN}/t_{spacer}$) is the fringe field through the tunnel, v_{TUN} is available voltage at the spacer, t_{spacer} is the spacer thickness, S_{TUN} is the tunneling area under the floating gate, A and B are the tunneling parameters.

3 An HDL Modeling using Verilog-A

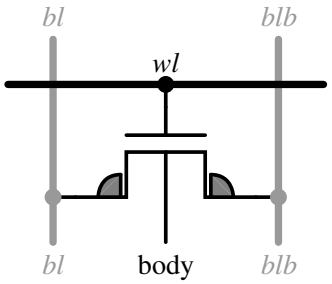

Figure 2: The schematic diagram of the S-Flash memory cell.

Figure 2 shows the schematic diagram of an S-Flash memory cell. The gate, the drain and the source of the transistor is connected to the word line (wl), the bit line (bl) and the inverted version of bit line (blb) respectively. The spacer is shown between the drain/source and the gate terminal.

Figure 3 is the flow-chart diagram, used to model the S-Flash memory. At the beginning of program, the various model parameters for the DC analysis have been defined. These model parameters include an aspect ratio of the transistor (W/L), threshold voltage (V_{th}), the body effect co-efficient (γ), (ϕ), (λ), the oxide thickness (t_{ox}), the transconductance parameters, the overlap capacitances, the transit frequency of the device (f_t), the time constant (τ), the velocity saturation (V_{sat}), the FN parameters (A and B) and flat-band voltage (V_{FB}). For a better comparison, the model parameters have been taken from the standard 0.18 μm CMOS technology with supply voltage of 3.3 V.

To calculate the correct value of the voltage, the current or the charge quantity at the respective terminal of the memory cell, the initial conditions have been set. The S-Flash memory cell has three modes of operations, program, read and erase. The mode of operation is decided with the input conditions of wl, bl and blb. During the program mode. These conditions is shown in the flow-chart. As explained in section 2, the threshold voltage increases in the program mode and decreases in the erase mode. The increment or decrement depends upon the amount of trapped charge in the spacer whose small signal net-capacitance is α. The achieved threshold voltage value will be used further to determine $I-V$ characteristics of the transistor. The program ends when the set simulation time is completed.

4 The simulation results

The simulations has been performed for a standard 0.18 μm nMOS transistor memory cell. The width and

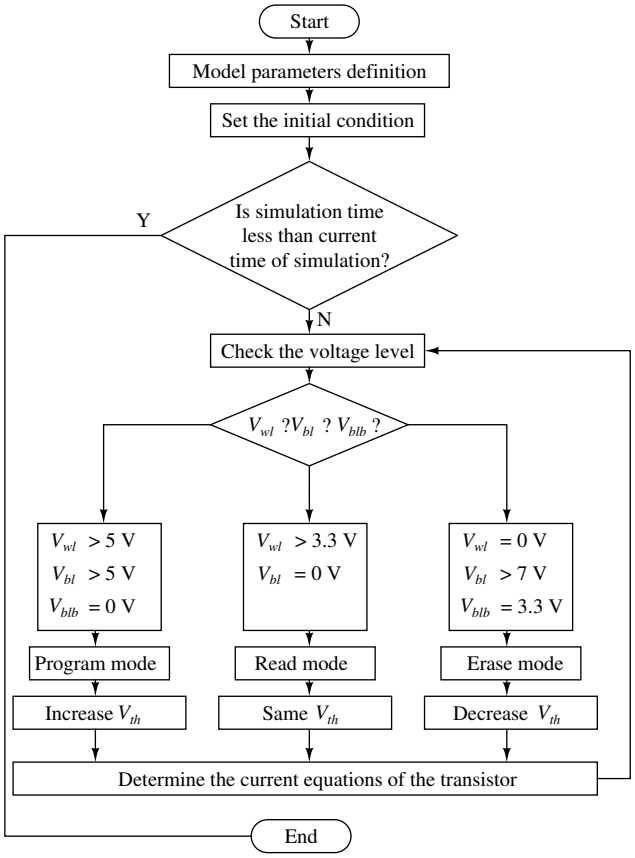

Figure 3: The flow chart for the S-Flash memory cell.

length of the nMOS transistor are 0.35 μm and 0.22 μm respectively. The value of α and the model parameters [11] have been chosen with reference to the TowerJazz semiconductor fabrication process [12]. The value of α is 2 fF. The initial value of the threshold voltage is 650 mV.

In order to perform the program, the read and the erase mode operation, the nodes of memory cell such as *wl*, *bl* and *blb* are biased at the voltage levels as shown in Figure 4. The mode of operation with the applied voltage level is as shown in table 1.

Table 1: The applied voltage level definition for the S-Flash memory cell.

Parameter	Program voltage [V]	Read voltage [V]	Erase voltage [V]
V_{wl}	5.0	3.3	0.0
V_{bl}	5.0	0.0	≥ 7
V_{blb}	0.0	–	3.3

Applying the voltage signal as shown in Figure 4, Figure 5 shows the transient drain current, the trapped charges in the spacer and threshold voltage variations. The simulated results show 94.9 ms of erasing time for 33.4 ms of programing time and for a memory speed of 10 kHz.

The 4×4 memory has been simulated using a proposed memory cell and the results are shown in Figure 6. The programming of the respective memory cell can be identified through the threshold voltage. In Figure 6, the cell at position (0,0) is programmed.

5 Conclusions

The threshold voltage modeling for the S-Flash memory has been presented using Verilog-*A*. The definition of threshold voltage and the spacer trapped charges, using HDL, enable the continuous monitoring of the programmed cell.

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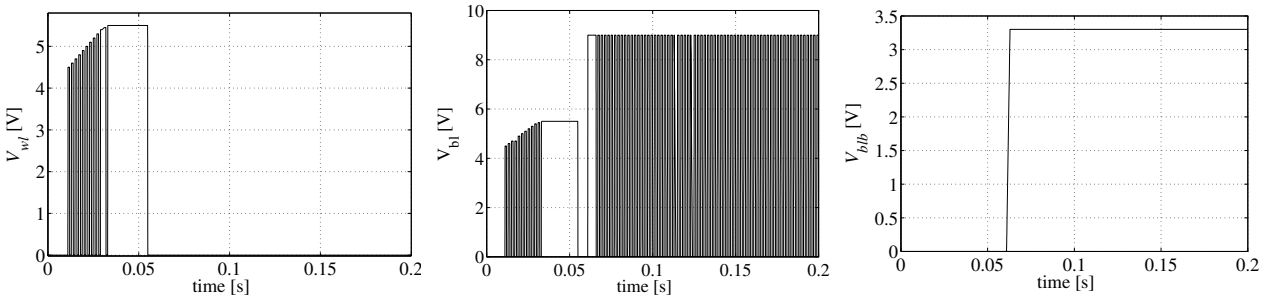
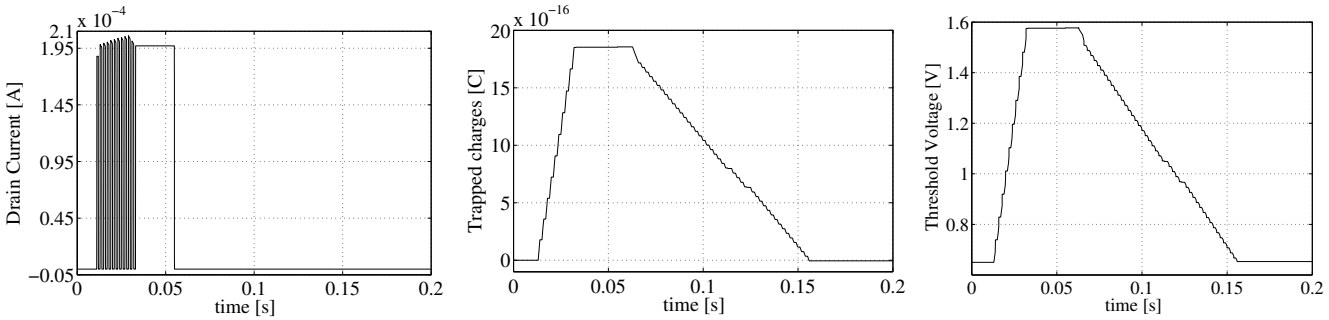


Figure 4: The applied input voltage levels at *wl*, *bl*, and *blb*.



(a) (b) (c)

Figure 5: (a) The transient drain current, (b) the trapped charges in the spacer and (c) the threshold voltage variation, with the applied voltage levels at *wl*, *bl* and *blb* (refer Figure 4).

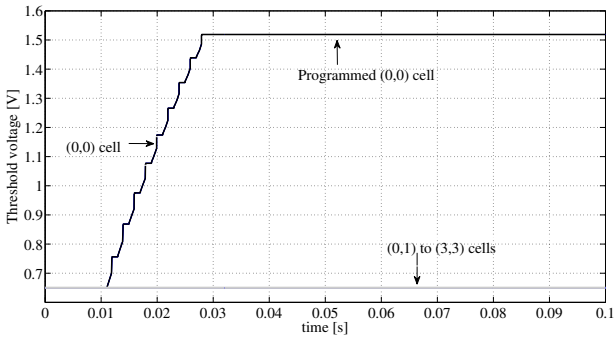


Figure 6: Variation of the threshold voltage for a 4×4 memory array.

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