TCAD Thermal Analysis of Gate Electrode Workfunction Engineered Recessed Channel MOSFET

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ABSTRACT

This paper discusses the thermal analysis of Gate Electrode Workfunction Engineered Recessed Channel (GEWE-RC) MOSFET involving an RC and GEWE design integrated onto a conventional MOSFET. Furthermore, it focuses on the comparative study of conventional MOSFET with GEWE-RC MOSFET in terms of various thermal parameters such as lattice temperature, heat conductivity, heat capacity and impact generation rate. This paper thus optimizes and predicts the feasibility of a novel design, i.e., GEWE-RC MOSFET for high-performance applications where self-heating effects and thermal behavior is a major concern. TCAD simulations using ATLAS demonstrate that the GEWE-RC MOSFET structure exhibits significantly improved thermal performance, where low power consumption is required and in digital logic and memory applications where fast switching action of MOS is needed.

Keywords: Gate Electrode Workfunction Engineered Recessed Channel, lattice temperature, heat conductivity, heat capacity, impact generation rate

1 INTRODUCTION

In the search of improved performance, the past several years have witnessed miniaturization of the basic MOS device structure. As the device technology is penetrating into the sub-50 nm era, some unwanted effects are observed such as punchthrough, hot carrier injection, noise in RF range, and dependence of threshold voltage on channel dimensions, DIBL and other short channel effect (SCEs) which affect the performance of the device in a negative manner. Furthermore, with this shrinkage in transistor size, inherent self heating effects have become critical in low power applications. As the issue of heat becomes increasingly important in deep-submicron MOSFETs, it is necessary to be able to accurately measure and model the thermal parameters of MOSFET to fully characterize its thermal performance.

Grooved gate MOSFETs are considered to enhance the device performance by suppressing SCEs and improving the hot carrier immunity; and thus the device reliability. In this structure, two potential barriers are formed at the concave corners due to high density of field lines. These potential barriers attribute to the improvement in SCEs. Although, the carriers in channel now require higher energy to overcome the barriers, which leads to driving current degradation, poor carrier transport efficiency and decrease in controllability of gate over the channel.

In order to overcome these limitations, Gate Material Engineering was proposed. The GME consists of two materials in the gate region such that the work function of metal gate 1 (M1) is greater than metal gate 2 (M2).The work function difference and the introduced step potential profile ensures screening of the channel region from drain potential variations.

Gate Electrode Workfunction Engineered Recessed Channel (GEWE-RC) MOSFET presented in this paper integrates RC MOSFET with GEWE architecture. Some past works on this device such as RF analysis and Noise analysis have been done before and they predict the feasibility of this novel device [2]-[8]. In this paper, the various thermal characteristics of GEWE-RC MOSFET have been compared with those of conventional MOSFET and Single Material Gate (SMG) MOSFET. The thermal parameters examined are lattice temperature, heat conductivity, heat capacity and impact generation rate. For this purpose, the structural design parameters , such as gate metal workfunction, oxide layer thickness, substrate doping, junction depth and gate length are optimized to achieve best performance.

This analysis has been done using ATLAS device simulator [1].The models activated in the simulation comprise Arora for doping and temperature dependence of low mobility, along with Concentration dependent Shockley-Read-Hall (CONSRH) which simulates leakage current due to thermal generation and the Auger recombination models for minority carrier recombination. Also, high electric field velocity saturation is modeled through the field dependent mobility model (FLDMOB) , heat flow simulation is enabled through Lat.Temp model, Selberherr's impact ionization generation is simulated by IMPACT SELB model.

Design Parameters	
Effective Channel Length (L_G)	40 nm
Source/Drain Junction Depth (X_j)	30 nm
Negative Junction Depth (NJD)	20 nm
Substrate Doping(N_A)	2 x e^{17} cm^{-3}
Source/Drain Doping (N^+_D)	2 x e^{20} cm^{-3}
Physical Oxide Thickness (t_{ox})	2 nm
Permittivity of Oxide	3.9
Work Function of Gates (Φ_{m1}/ Φ_{m2})	4.77/4.1

Table 1: Design Parameters for GEWE-RC MOSFET used in the analysis

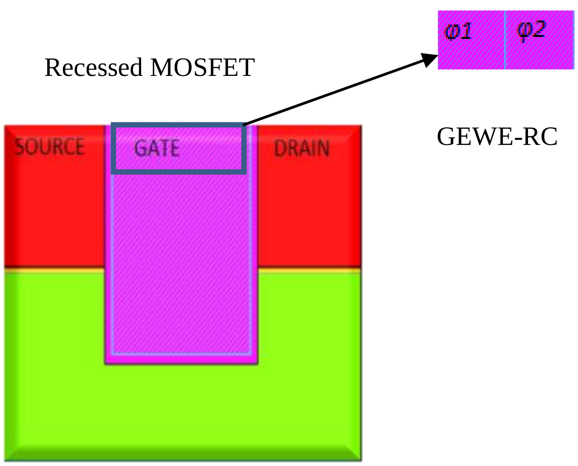

Figure 1: Architecture of GEWE-RC MOSFET

The architecture of RC MOSFET is obtained by recessing the channel i.e. separating the source and drain with a groove and the architecture of GEWE-RC MOSFET, is achieved by incorporating gate electrode workfunction engineering onto the RC MOSFET(Figure 1).

The drain bias (V_{ds}) applied on the devices is 3.5 V. GEWE-RC MOSFET has yet not been fabricated, so the simulation results have been calibrated with Single Material Gate-RC MOSFET which has been fabricated.

The thermal analysis is done without considering temperature variations induced by multi devices interconnection, a single device is simulated and temperature of all the contact electrodes is 300 K.

2 THERMAL ANALYSIS

While analyzing various thermal parameters, the position along the channel has been normalized. Furthermore, in all the curves where normalization has been carried out, x = 0 represents the source end and x = 1 represents the drain end.

2.1 Lattice Temperature

In GEWE- RC MOSFET, high electric field is redistributed across the channel, i.e. it relatively increases near the source region and decreases near the drain region resulting in more uniform field along the channel. This screens the channel regime from potential variations at the drain, leading to reduced energy carrier heating, thereby diminishing energy transmission which accounts for decreased lattice temperature as shown in Figure 2 [9].

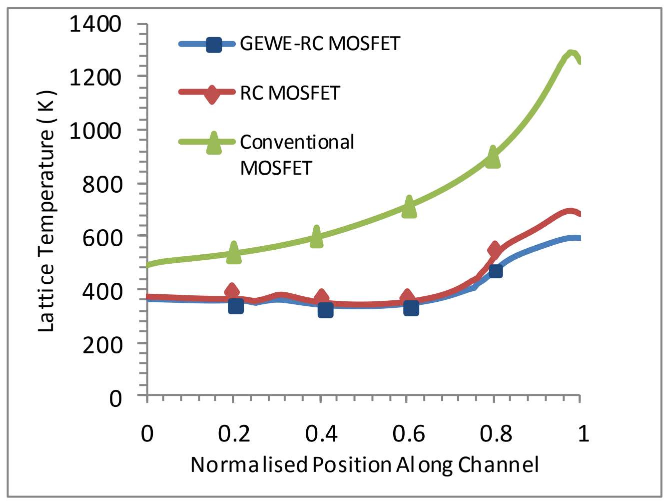

Figure 2: Variation in Lattice temperature along the channel

2.2 Heat Conductivity

The kinetic theory relates the mean free path **Λ** of the dominant heat carrier to the specific heat due to that carrier per unit volume C, the thermal conductivity k, and the speed of the carrier v, by

$$k = \frac{1}{3} C\, v\, \Lambda \qquad (1)$$

In Recessed channel MOSFET as the channel length increases for the same gate length as that of conventional MOSFET, the mean free path of the energy carriers increase. Consequently, they would experience less collisions (representative of resistance against motion), both with other energy carriers and with the boundaries of the channel, enhancing the thermal conductivity [10]. In recessed MOSFET, the potential barriers formed at the

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corners leads to less density of carriers in the middle of the channel than at the drain and source end. Therefore, collisions experienced by the carriers would be less, hence showing a peak in conductivity in middle of the curve. Furthermore, with GEWE architecture, the step potential profile, due to different work functions of two metal gates, ensures reduction of SCEs and screening of the channel region under gate 1 from drain potential variations [8]. Thus, the average electric field in the channel is enhanced, improving the energy carrier velocity which enhances the thermal conductivity.

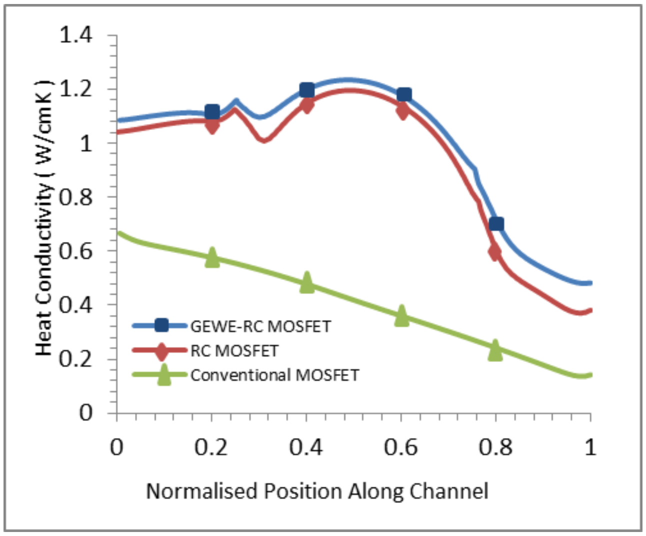

Figure 3: Variation in Heat Conductivity along the channel

2.3 Heat Capacity

Heat capacity of solid i.e. the ability to store heat and cool down, increases with temperature, due to the increasing number of excited degrees of freedom, requiring more energy to cause the same temperature rise as it is shown in figure 4. Heat capacity shows the same variations along the channel as lattice temperature. The gate metal contribute very less to the heat capacity of the device because there are small fraction of electrons which are within k_BT of the Fermi level which contribute to the specific heat. Therefore, there is not much difference in the curves obtained for Single material Gate and Dual Metal Gate. However, as compared to conventional MOSFETs, there is a decrease in heat capacity since the temperature of the device is lowered in the GEWE-RC design.

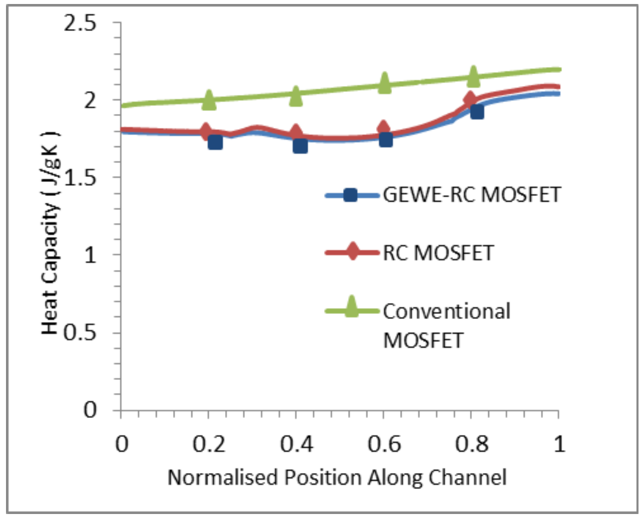

Figure 4: Variation in Heat Capacity along the channel

2.4 Impact Generation Rate

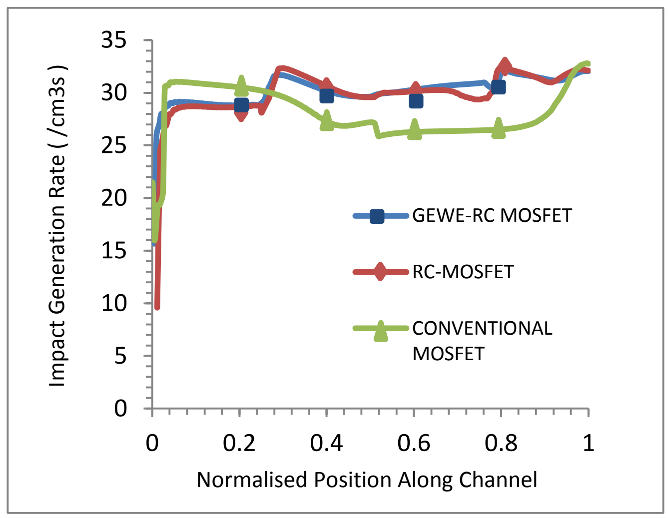

Figure 5: Variation in Impact generation rate along the channel

Impact-ionization is a three-particle generation process. Carriers that gain high energies while traveling through high field regions undergo scattering events with bonded electrons in the valence band. The excess energy is transferred to this electron which is lifted into the conduction band creating a new electron-hole pair. This can lead to impact-ionization substrate current. It is one of the important components of the off-state leakage current. Also, substrate current provides a good monitor to the heating of the channel carriers and to the electric field in the drain region. GEWE-RC MOSFET, enhances drain current characteristics and average electric field and suppresses SCEs due to the screening of the channel region from drain bias variations [2]-[5]. Consequently, a uniform impact generation rate is observed in case of GEWE-RC MOSFET.

3 CONCLUSION

As shown in this work, from the analysis of the microscopic thermal sources and dynamic performance of the devices; GEWE-RC MOSFET exhibits superior thermal performance in comparison to its conventional counterpart. It can be concluded that the redistribution of high electric field along the channel and lower collisions experienced by the energy carriers are responsible for the noticeable improvements observed in the thermal performance. Hence, proving its potency for higher packing limits and digital logic and memory applications where fast switching action of MOS is needed. Lower lattice temperature, heat capacity, higher heat conductivity and uniform impact generation rate pertained by the GEWE-RC architecture strengthens the concept of using it for such applications, thereby giving a new opening for usage in low power consumption devices.

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