Effects of sub-threshold operation on 32 nm technology node PMOSFETs evaluated from the perspective of 2-stage NBTI model

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ABSTRACT

In ultra low-power applications, operations in the transistor's sub-threshold regime are critically important for meeting the system's stringent power requirements. However, due to the aggressive downscaling of CMOS transistors, the stress-induced NBTI has emerged as a reliability threat even in low-power systems. In this work, the characterization of NBTI in this simulation-based study is demonstrated during sub-threshold operation application. The two-stage model was implemented to simulate the positively charged E'centers, interface trap generation and the resulting threshold voltage shift. The observed threshold voltage shift was found to exhibit power-law time dependence of n ~ 0.1, suggesting a hole-trapping mechanism. Moreover, the generation of switching oxide trap and interface trap in sub-threshold regime shows similar characteristics to that of super-threshold operation, hence, the sub-threshold NBTI is just as critical to the system's reliability.

Keywords: NBTI; interface trap, switching oxide trap; p-MOSFET; high-k dielectric

1 INTRODUCTION

In ultralow-power applications, operations in a transistor's sub-threshold regime are critically important for meeting a system's stringent power requirements. However, considering the aggressive downscaling of complementary metal-oxide-semiconductor (CMOS) transistors, stress-induced NBTI has emerged as a reliability threat even in low-power systems. As a result of scaled oxide thickness in sub-nanometer regime devices, the increased electric field further enhanced the NBTI degradation effects. Many studies that used circuit-level simulation used the R-D model to investigate the effects of NBTI degradation on a circuit's performance [1], [2]. However, as the oxide trapping/de-trapping effect mechanism affect device performance considerably [3], [4], a device-level analysis of the effect of NBTI, which involves both oxide and interface traps under sub-threshold operation regime, is necessary. From the device-level perspective, operation in sub-threshold regime for UT-EOT devices is contributed by the minority carrier and holes under the gate, which diffuses due to the application of V_{DS}. However, different mechanisms occurred given the very thin EOT. Direct tunnelling of holes from substrate to bulk oxide will be trapped in E'center defect precursor, which further degrades device performance [5]. Our earlier research, which was based on a simulation study [6]–[9], used the R-D model to analyse the NBTI effect on devices. Thus, the oxide trap effect has no contribution in the NBTI degradation assessment. In this paper, we used two-stage NBTI model to model the NBTI degradation effects caused by the minority carrier, holes, and tunnel in bulk oxide and trapped in the defect precursor in HKMG PMOSFET devices.

2 SIMULATION SETTINGS

The simulated testbed PMOSFET devices with high-k/SiO_2 gate stacks used in this work are based on the gate-first scheme of the foundry-standard 32 nm CMOS process [10], [11]. The device process had incorporated shallow trench isolation with intrinsic stress, deposition of high-k dielectrics with metal gate, with incorporated stress engineering where epi-SiGe pockets is used for PMOSFETs, silicidation and dual stress liner.

In the simulation, the Two Stage NBTI model is activated at interface region using the NBTI command by specifying the density of the precursor N_0, where, the N_0 = 5.0E12 cm^{-2} [9]. The interface charge density is determined based on equation (1) [10] and the relationship of threshold voltage shift with trap concentrations and interfacial charge is highlighted as in equation (2) [12][13].

$$Q = Q_{ox} + Q_{it} = qN_0\langle S_2 + S_4\rangle + qN_0\langle S_4 f_{it}^p\rangle \quad (1)$$

$$\Delta V_{th}(t) = -\Delta Q_{ox}(t) + \Delta Q_{it}(t)/C_{ox} \quad (2)$$

The threshold voltage shift, ΔVth, in this work is determined by the commonly used On-The-Fly (OTF) technique [14]–[16]. The pre-stress voltage applied in this simulation is to ensure all states are filled at the early phase of stress period by equilibrate the occupancy of different states [17]. The stress time in this simulation is increased up to 1000 s to ensure time-zero delay in OTF technique which introduces an artefact can be reduced [15]. The artefact for the measured ΔVth will not give BTI power-law (ΔVth = $A.t^n$). In order to investigate the degradation kinetics in sub-threshold operation regime, the stress time (and relaxation time) in this simulation is increased up to 10^9s to fully monitor the degradation kinetics.

3 RESULTS AND DISCUSSION

3.1 Sub-threshold operation in the perspective of Two-stage NBTI model

The degradation in the both sub-threshold and super threshold operating regime in the perspective of Two-Stage model is validated by the observed the power law time dependence of the resulting ΔVth shown in Figure 1(a). For thin and thick EOT devices, both shows a relatively small exponent within the range of n ~ 0.1 which attributed to hole trapping effect as in agreement with ultrafast switching measurement in [3]. The hole trapping occurred at pre-existing oxide traps which fully explained by the Two-stage NBTI model where E'centers acted as switching trap thus support the intrinsic limitation of reaction-diffusion (R-D) model as commonly experimental in most NBTI studies [12].

To further investigate the kinetics of NBTI degradation under sub-threshold operation, the concentrations of positively charged E'centers, S_2, and interface traps, S_4, are extracted in this work. Figure 1(b) shows the kinetics of S_2 and S_4 as the stress time increased for sub-threshold operating regime. The generation of S_2 is explained by the mechanism of hole captured at the E' center precursor. From the graph, the S_2 is shown to be higher than S_4 for both sub-threshold voltages implies that the bulk defect is dominant contribution in NBTI degradation which in agreement with standard charge pumping measurement work in [13]. The kinetics of S_2 and S_4 were observed in dynamic NBTI experimental works where the level of Vth degradation reflects the switching hole-trap mechanism [18], [19]. As the application of stress bias is below threshold voltage, the holes are believed to be the minority carriers in the substrate which present under the gate.

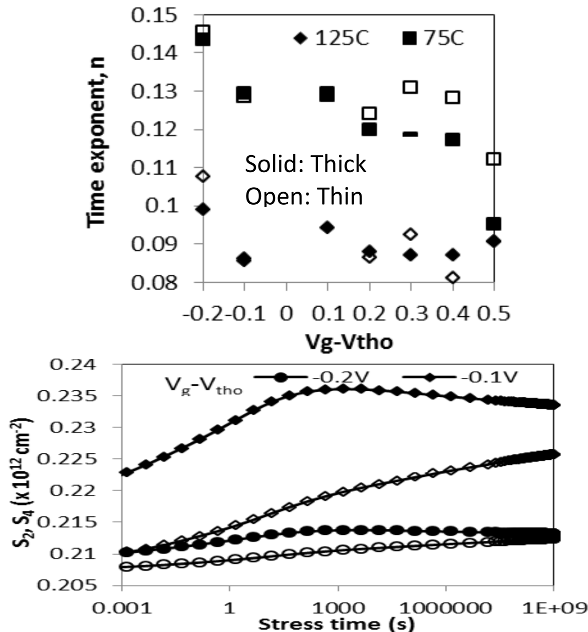

Fig. 1(a) Time exponent, n (b) Simulated S_2 and S_4

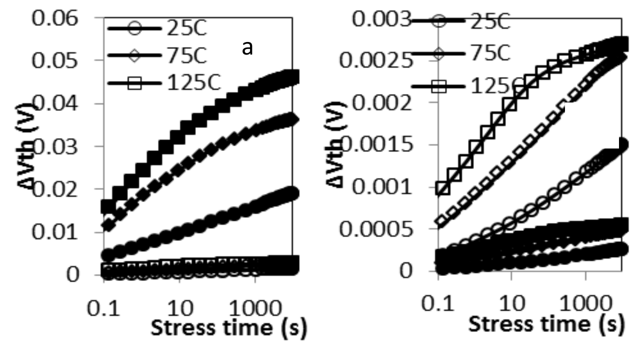

Fig. 2 Simulated ΔVth trends for different operating temperatures at (a) a wide range of V_g-V_{tho} (Solid: -0.5V, Open: -0.1V) (b) a sub-threshold voltages V_g-V_{tho} (Solid: -0.1V, Open: -0.2V)

Figure 2 (a) shows the ΔVth trends for different operating temperatures at sub-threshold and super-threshold stress voltages. A very weak temperature-dependence is observed for the sub-threshold stress voltage as in agreement with [20]. However, the ΔVth of sub-threshold stress voltage is shown to be temperature dependence as shown in Figure 2 (b) when plotted is shown for sub-threshold voltage regime only. The smaller values of both sub-threshold voltage and stress temperature show smaller ΔVth as in agreement with most NBTI studies [19]. This proves that the NBTI which is a temperature- activated mechanism also happen in sub-threshold operation regime where the level of degradation is smaller as compared to su per-threshold regime.

3.2 Recoverable component under sub-threshold operation regime

In the Two-stage NBTI model, the recovery of E'center defects is delayed when hydrogen moves to the E'center due to the hydrogen is locks in the positive charge. This mechanism is as explained in Section 3.1 which can reduce the recovery effect thus producing the power- law time exponent, n ~ 0.1.

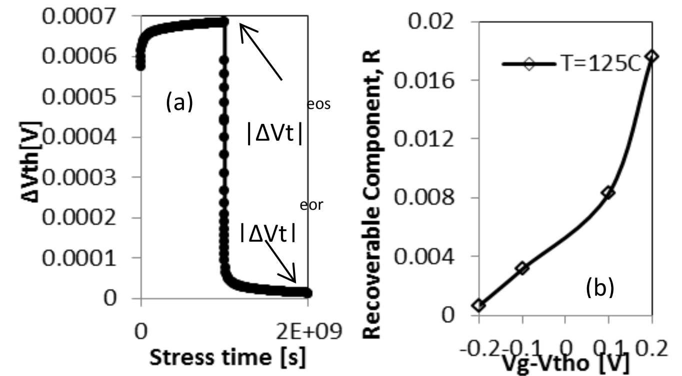

Fig. 3. (a) Evolution of ΔVth and defination of recovery component, R = $|\Delta Vt|^{eos}$ - $|\Delta Vt|^{eor}$ in a typical dynamic NBTI cycle (b) R as a function of sub-threshold and super-threshold voltage

To further relates the NBTI degradation effect under sub-threshold operation regime, the recoverable component is extracted from graph as shown in Figure 3 (a) and plotted in Figure 3 (b). Figure 3 (a) shows the evolution of dynamic NBTI as a result from a simulated stress and relax cycle. The recoverable component, R or |ΔVt| recovered per cycle is defined as eq. (3) according to [21]

$$R = |\Delta Vt|^{eor} - |\Delta Vt|^{eos} \quad (3)$$

where $|\Delta Vt|^{eor}$ is |ΔVt| at the end of relaxation cycle and $|\Delta Vt|^{eos}$ is |ΔVt| at the end of stress cycle. The value for $|\Delta Vt|^{eor}$ represents the permanent part of |ΔVt| that is not recovered at the end of relaxation phase [21]. Figure 3 (b) shows the recoverable component for sub-threshold and super-threshold operation regime. Larger R is observed for super-threshold operation regime as more hole trapping during stress for higher voltage [21]. However, the R still can be significant in number for sub-threshold operation regime which the minority carriers also contribute to the hole trapping during stress. More R is observed for the higher sub-threshold voltage.

3.3 Physical interpretation of NBTI degradation based on energy distribution of switching oxide trap and interface trap

In this work, we investigate the relationship between energy depths of $\Delta\varphi_s$, at the interface below E_f with applied stress voltage under sub and super-threshold regime. We defined the energy depth of $\Delta\varphi_s$ as shown in Figure 4 (a) where $\Delta\varphi_s$ = Ef (Si/SiO_2 interface) – Ev (Si/SiO_2 interface). The energy depth of $\Delta\varphi_s$ is used in the experimental work as to probe the energy distribution charges in gate dielectric [4]. The larger $\Delta\varphi_s$ is found under sub-threshold voltage regime as compared to super-threshold voltage regime as shown in insert. This indicates that the energy band diagram almost not bend up in the oxide region whereby the larger $\Delta\varphi_s$ reflects the charges associated in the degradation is due to natural precursor charge which energy levels below the silicon valence band [4]. Hence, as discussed in the previous section, the small degradation may be associated with the pre-existing defect within the dielectric.

To further investigate the mechanism behind the minor degradation, we probe the energy distribution of each traps at three different location consists of near to Source, [A], in the middle of the channel, [B], and near to Drain, [C]. By following the earlier work [17], [22] where similar range of energy level is used, Figure 5 (a) – (d) shows the energy distribution of the switching oxide trap and interface trap during sub and super-threshold operation within the specified locations. First impression on the energy distribution of switching oxide trap, S2 and interface trap, S4 based in different locations, tell us that they are randomly distributed within the specified energy levels. However, closer observation indicates that there is interesting information on the energy distribution rhythm

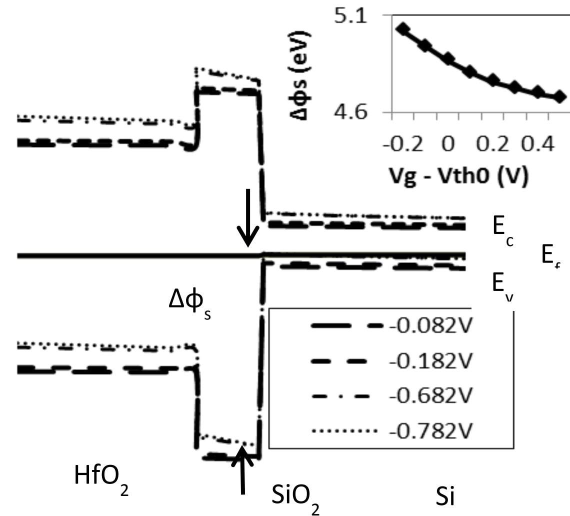

Fig. 4. Energy band diagram showing the energy depth of Δφs. Insert is extracted $\Delta\varphi_s$ with respect to sub and super-threshold regime

for a different location. Middle of the channel, [B] gives significantly different amount of switching oxide trap and interface trap in the specific energy levels during sub and super-threshold regime. In contrast, [A] and [C] region give almost similar amount of switching oxide trap and interface trap during sub and super-threshold regime respectively. The higher amount of switching oxide trap and interface which the traps are located in the middle of the channel is in agreement with relative random telegraph signal (RTS) [30]. Graph in Fig. 6 shows that the number of precursor is reduced when biased in super-threshold as compared to sub-threshold at the middle of the channel. This indicates that the precursor has been transformed into a positively charged switching oxide trap hence fewer precursors exist. More switching oxide trap is perceived as compared to interface trap within the specified energy range which is similar to what has been witnessed in previous discussion. This supports that the bulk defect is dominant contribution in NBTI degradation [13].

4 CONCLUSION

The effects of sub-threshold operation regime in NBTI degradation was investigated for HKMG PMOSFET devices which have less than 2 nm EOT. This sub-threshold operation regime is suitable for ULP applications which require very small supply voltage. The smaller value of V_{DD} (V_g-V_{tho} < 0) shows smaller ΔVth. However the mechanism of the degradation is similar to super-threshold operation regime where the generation of switching oxide trap and interface trap significantly contributed to the device degradation. More switching oxide trap is observed within the specified energy profile as compared to interface trap.

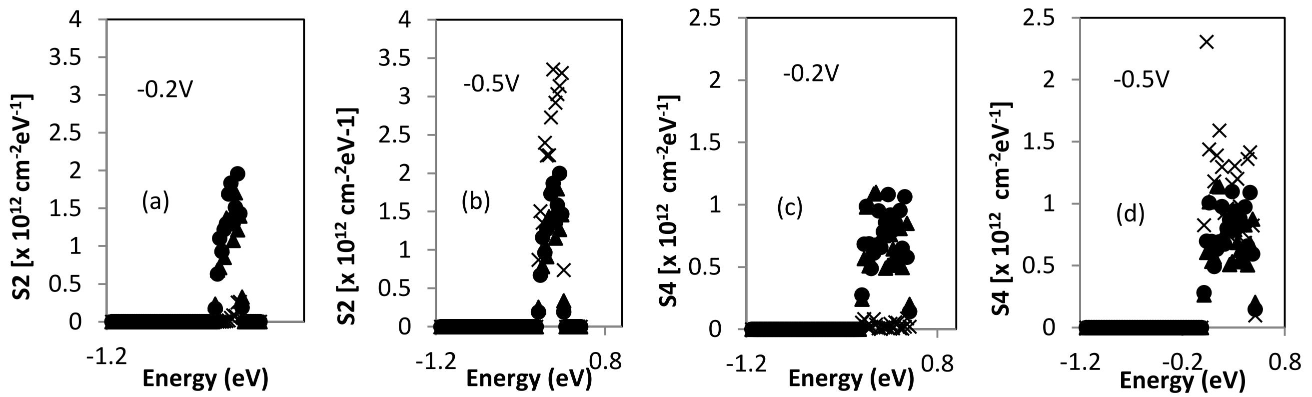

Fig. 5. The energy distribution of the switching oxide trap during (a) sub (b) super-threshold operation and interface during (c) sub (d) super-threshold within the specified locations. Sub: Vg-Vtho = -0.2V and Super: Vg-Vtho = -0.2V

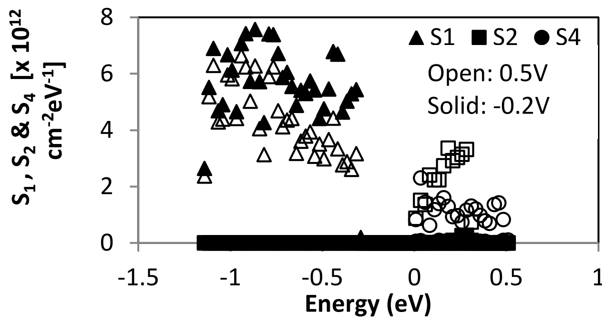

Fig. 6. The energy distribution of the precursor, switching oxide traps and interface traps at the middle of the channel

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