Compact Negative Bias Temperature Instability Model for Nanoscale FinFET Reliability Simulation

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ABSTRACT

A compact Negative Bias Temperature Instability (NBTI) model, which is based on a novel Reaction-Trapping (R-T) theory, is proposed to predict the static and dynamic NBTI degradation in nanoscale FinFET reliability simulation. This R-T theory is on the basis of the hypothesis that threshold voltage variation is induced by H atoms captured by either shallow or deep level traps in the gate oxide. The advantage of the novel NBTI model is demonstrated by comparing with the classical Reaction-Diffusion NBTI model. A good match between the proposed NBTI model and the experimental results is obtained in terms of the temperature dependence and the structure effect of nanoscale FinFETs.

Keywords: Negative Bias Temperature Instability (NBTI), FinFET, nanoscale, R-T theory

1 INTRODUCTION

As one of the most promising candidates for post-CMOS era, nanoscale P-type FinFETs is seriously susceptible to Negative Bias Temperature Instability (NBTI) effect [1,2]. Therefore, an accurate NBTI model is highly desirable to predict the performance degradation of tightly designed FinFET circuit. A classical Reaction-Diffusion (R-D) model [3-5] has been reported in the previous works. According to the R-D theory, the shift of the threshold voltage (ΔVth) and the stress time follows the power law [6-8]. However, this relationship is based on the infinite thickness of the gate oxide, which is not the case in nanoscale FinFETs. Due to the ultra thin gate oxide of FinFET, it is nearly impossible for all the reacted H atoms to diffuse effectively in the gate oxide, as supposed in the R-D theory. Nevertheless, the novel Reaction-Trapping (R-T) theory [9] assumes that H atoms diffused into the gate oxide are trapped in either shallow or deep levels, and the total number of broken Si-H bond is still calculated with the classical R-D theory.

2 MODEL DEVELOPMENT

The schematic view of the bulk FinFETs [10] is shown in Figure 1. The device used here is with the gate length Lg =15nm, Fin height Hfin=25nm and Fin width Wfin =7nm. The gate oxide on the side wall is tox=1.2nm. The top surface of Fin is covered by thick oxide. The NBTI stress voltage Vgstr= -2.5V is applied to gate with drain-source voltage Vds= 0V. Both stress and recovery time range from 0s to 1000s.

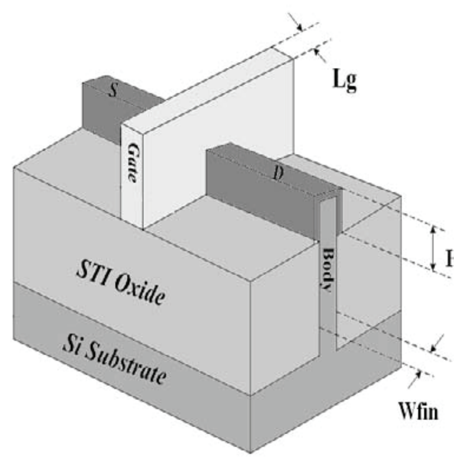

Figure 1: Schematic view of bulk FinFET.

2.1 Static NBTI Model

Stress Process: During the stress process, with the large negative bias applied to the gate, Si-H bonds at the silicon/oxide interface are broken down by holes in the inversion layer break down. H atoms diffuse into the gate oxide and some of them are captured by traps. Si- dangling bonds are left behind, which result in ΔVth. Referring to the charge trapping theory [11,12], the interface state density (Nitstr) generated during the stress process is written as:

$$N_{it}^{str} = N_{it\_\max}^{str}\left[1-\exp\left(-t/\sigma\right)\right] \tag{1}$$

Where t is the stress time, σ is the capture cross section and $N_{it\_\max}^{str}$ is the maximum interface state density obtained from R-D theory [4,13]. The threshold voltage variation during stress process (ΔV_{th}^{str}) is:

$$\Delta V_{th}^{str}(t)=\frac{qN_{it\_\max}^{str}}{C_{ox}}=\frac{qt_{ox}}{\varepsilon_{ox}\varepsilon_0\sqrt{W_{fin}}}\left[\sqrt[\frac{1}{2n}]{K^2\left(\exp\frac{E_{ox}}{E_T}\right)^2 C_{ox}(V_{gstr}-V_{th})}\right]$$
$$\cdot\left(W_{fin}\sqrt{Ct}+\frac{\left(\sqrt{Ct}\right)^2}{4}\right)^{2n}\cdot[1-\exp(-t/\sigma)] \qquad (2)$$

Where n=1/4 is relative to the diffusion species [4], $C=[exp(-E_a/kT)]/T_0$ is the diffusion constant depending on the temperature and diffusing species [14]; T_0 , E_a and E_0 are constants given in [4,15].

Recovery Process: Since the stress voltage is removed during the recovery process, some H atoms trapped in the shallow level escape and diffuse back to repair the Si- dangling bonds at the interface. Others trapped in the deep level are still confined by the defects and corresponding to a partly recovery of ΔV_{th} [6]. To be Consistent with the stress process, ΔV_{th} results from the H de-trapping from the shallow level is written as

$$\Delta V_{th}^{shallow}(t)=\left(\Delta V_{th\_\max}^{str}-\Delta V_{th}^{deep}\right)\exp(-t/\sigma) \qquad (3)$$

Where ΔV_{th}^{deep} is the ΔV_{th} caused by the deep level traps and insensitive to the recovery duration; the term of $\left(\Delta V_{th\_\max}^{str}-\Delta V_{th}^{deep}\right)$ reflects the maximum ΔV_{th} due to shallow level traps. The recovered V_{th} (ΔV_{th}^{rec}) is due to the effect of both deep and shallow level traps.

$$\begin{aligned}\Delta V_{th}^{rec}(t)&=\Delta V_{th}^{deep}+\Delta V_{th}^{shallow}(t)\\&=\Delta V_{th}^{deep}+\left(\Delta V_{th\_\max}^{str}-\Delta V_{th}^{deep}\right)\exp(-t/\sigma)\end{aligned} \qquad (4)$$

This novel R-T theory has been verified in [16] by a Twin Silicon Nanowire MOSFET [17]. The result shows that, NBTI model based on the R-T theory presents an evident advantage to the classical R-D theory.

The temperature dependence of ΔV_{th} due to NBTI stress is shown in Figure 2. Resulting from the experiment, the higher is the temperature, the larger is the ΔV_{th}. This phenomenon indicates that when temperature increases, the inversion carriers reacting with the Si-H bonds suffer more from scattering effect which dramatically degrades the kinetic energy. Therefore, with elevating temperature, less Si- dangling bonds is generated and smaller ΔV_{th} is observed. The result also shows a good match between the R-T model and the experimental result over a large range of temperature.

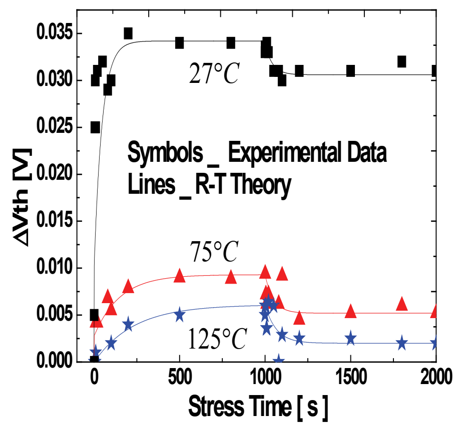

Figure 2: Comparison of NBTI R-T model and measured data at different temperatures.

2.2 Dynamic NBTI Model

In the dynamic NBTI effect, the density of Si-H bond ($N_{Si\text{-}H}$) is assumed to be constant. As a result of deep level trapping, number of available Si-H bond decreases after every stress-recovery cycle. Meanwhile, H atoms trapped in the shallow level diffuse back during every recovery process and induce quick recovery of ΔV_{th}. The dynamic NBTI model in stress (Eq.5) and recovery processes (Eq.6) are derived based on the static NBTI R-T theory:

$$\Delta V_{th(i)}^{str}(t)=\Delta V_{th(i-1)}^{deep}+\frac{qt_{ox}}{\varepsilon_{ox}\varepsilon_0\sqrt{W_{fin}}}\left[\sqrt[\frac{1}{2n}]{\frac{k_f}{2k_r}\left(N_{Si-H}-\sum_{m=0}^{i-1}N_{H(m)}^{deep}\right)C_{ox}(V_{gstr}-V_{th})}\right]$$
$$\cdot\left[W_{fin}\sqrt{Ct}+\frac{\left(\sqrt{Ct}\right)^2}{4}\right]^{2n}\left\{1-\exp\left[-\frac{t-(i-1)\Gamma}{\sigma}\right]\right\}$$
(5)

$$\Delta V_{th(i)}^{rec}(t)=\Delta V_{th(i)}^{deep}+\Delta V_{th(i)}^{shallow}\left(t-[i-1]\Gamma\right) \qquad (6)$$

Where i is the cycle number and Γ is duty time; $\sum_{m=0}^{i-1}N_{H(m)}^{deep}$ is the accumulation density of H trapped in the deep level. Figure 3 shows the simulation result of ΔV_{th} at different stress frequency. The result is consistent with the previous reports [18-20].

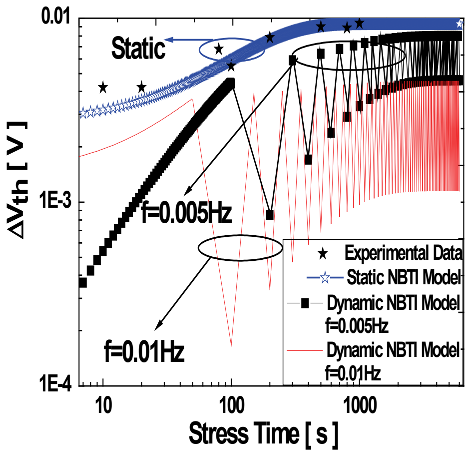

Figure 3: Dynamic NBTI simulation with frequency of f=0.01Hz and f=0.005Hz.

The R-T model is also robust in predicting the ΔV_{th} of nanoscale FinFET under different NBTI stress conditions. As shown in Figure 4, both Fin width and NBTI stress voltage impact the shift of threshold voltage. The simulation result achieves a good agreement with the measured data [1].

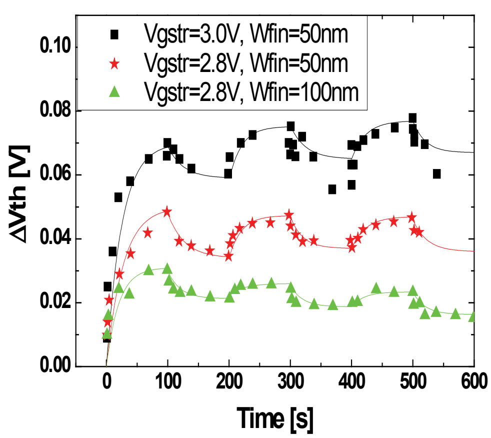

Figure 4: The ΔV_{th} of FinFETs with various Fin widths under different NBTI stress conditions.

3 CONCLUSIONS

This paper proposed a compact NBTI model to predict both static and dynamic NBTI effects in nanoscale FinFET reliability simulation. The NBTI modeling is carried out based on a novel Reaction-Trapping (R-T) theory and the results agree well with the experiments over a large range of temperature. The dynamic NBTI is also simulated with different stress frequency, and verified by comparing with experimental data from FinFETs with different Fin width.

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