

Simulation Study on Dopant Fluctuation Impact on SRG MOSFET Device and Circuit Performance

Hao Wang^{*}, Jin He^{*,**}, Ying Liu^{*}, Caixia Du^{*}, Qingxing He^{*}, Yun Ye^{*}, Wei Zhao^{*}, Wen Wu^{*}, and Wenping Wang^{*}

^{*}Peking University Shenzhen SOC Key Labor., PKU-HKUST Shenzhen-Hong Kong Institution, Shenzhen, China

^{**}Shenzhen Huayue Teracale Chip Electronic Limited Co., Shenzhen, China

ABSTRACT

This paper investigates the impact of random dopant fluctuation on surrounding gate MOSFET, from atomic statistical simulation of device to circuit performance evaluation. The doping profile is generated by an analysis of each lattice atom and then the threshold voltage variation is obtained by device Drift-Diffusion simulation. From it, the circuit performance is evaluation is performed by feeding the result into a surrounding-gate MOSFET model in the circuit simulator. It is shown that a significant fluctuation in threshold voltage is due to volume decreases. The circuit simulation results also reveal that a surrounding gate MOSFET based 6-T SRAM presents a promising resistibility to noise disturbance compared to the traditional bulk MOSFET.

Keywords : surrounding gate MOSFET, random dopant fluctuation, threshold voltage variation, SRAM, static noise margin

1 INTRODUCTION

With the aggressive scaling down of MOSFETs in order to obtain better circuit performance [1,2], the statistical variation in nano-scale transistor is becoming a serious issue [3-5]. Therefore, the variation-tolerant prediction and device design technique are required [6]. The sources of variations on chip can be divided into temporal and spatial components [7-8]. The temporal component relates to the run-time variations [8], such as NBTI effects and body effect in SOI devices. And the spatial component corresponds to the variations in geometric factors, mainly including line edge roughness (LER) [9], layout dependent variations [10], systematic and random variations in film thicknesses [11], and random dopant fluctuation effect [12-17].

In nano-scaled novel structure devices, such as FinFET and surrounding gate MOSFETs, Random Dopant distribution Fluctuations (RDF) becomes more and more significant. Therefore, developing a general method to investigate the impact of random dopant fluctuation effect on characteristics of novel structure devices is necessary.

This paper investigates the influence of RDF on surrounding gate MOSFET on device characteristics and circuit performance. The content is organized as follows: In section II, the approach of simulation, including the problems

and strategies are presented; then, the results and discussions are provided in section III; Finally, a conclusion is drawn in section IV.

2 SIMULATION APPROACH

2.1 Atomic Level Simulation

Threshold voltage is one of the significant parameters of MOSFETs in device modeling and circuit simulation. Accordingly, the threshold voltage is regarded as the representation to reveal the impact of random dopant fluctuation on the device performance.

First, Monte Carlo method [18] is used to generate the dopant atom distribution in the volume of interest. The random dopant placement algorithm, as shown in Figure1, is based on a pseudo lattice to imitate real crystal lattice to ensure a relatively low computational complexity with reasonable accuracy.

As the placement algorithm considered every lattice atom, the resulting dopant atom distribution is able to reflect the fluctuation of total number of the dopant atoms, variation of dopant atom position and effect of discrete doping concentration.

However, the key problem in the device simulation is that the data about atoms cannot be directly used in popular commercial drift-diffusion device simulator. A method to translate atomic information to doping profile is given by Sano et al. [19], which emphasizes the actual effect of a dopant atom. The equivalent charge density corresponding to a single dopant located at the origin is given by

$$\rho(r) = \frac{ek_c^3}{2\pi^2} \frac{\sin(k_c r) - (k_c r) \cos(k_c r)}{(k_c r)^3} \quad (1)$$

Where k_c is the inverse of the screening length, e is elementary charge, r is the distance of grid point to from the single dopant atom.

2.2 Circuit Performance Evaluation

Thousands of devices with variations induced by random dopant fluctuation are simulated in SRAM cell circuit to investigate the impact of RDF on the performance of SRAM cell, such as static noise margin and write noise margin. Since the device simulation launched by general Drift-Diffusion simulator is computationally intensive and the threshold voltage follows Gaussian distribution, randomly generated

doping profiles are simulated 100 times and then fitted into Gaussian distribution. Finally, in order to investigate the influence of RDF on the circuit performance, the random dopant fluctuation effect is added into the compact model of surrounding gate MOSFET [19].

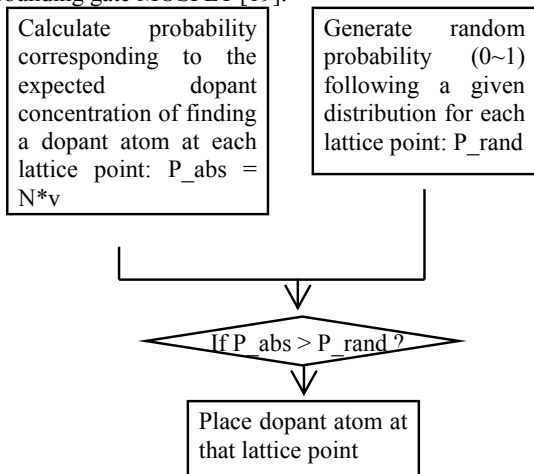


Figure1: Random dopant placement algorithm [8]. In the expression $P_{abs} = N \cdot v$, N is the expected doping concentration with any doping profile, and v is the volume owned by each atom in the pseudo lattice.

3 RESULT AND DISCUSSION

Figure2 shows an example of random dopant atom placement. Both the total number in the channel and the position of dopant atoms lead to aggressive fluctuation of the doping profile. First, the total number variation of dopant atoms reflects the deviation of doping concentration from the expected value. Second, the decreasing number of dopant atoms in nanoscale devices significantly discretizes the doping profile so that some of the grid points in device simulator have a much higher concentration. Finally, which is probably most important, dopant atoms located in different positions have distinct influence on the device performance, as shown in Figure3. The simulation result indicates that dopant atoms, which are located at the central in channel direction and close to surrounding oxide, make greater contribution to the threshold voltage, or in other words, are more effective dopants. Accordingly, characterization of devices can be various, though they may have the equal doping concentration of the channel as a whole.

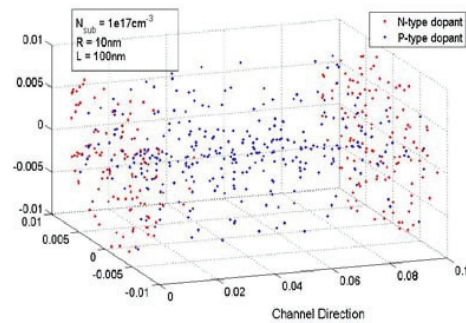


Figure2. An example of random dopant placement in channel region of surrounding gate MOSFET. Red points represent N-type dopant in S/D gradient region; while blue points represent P-type dopant reflect discretized channel doping profile.

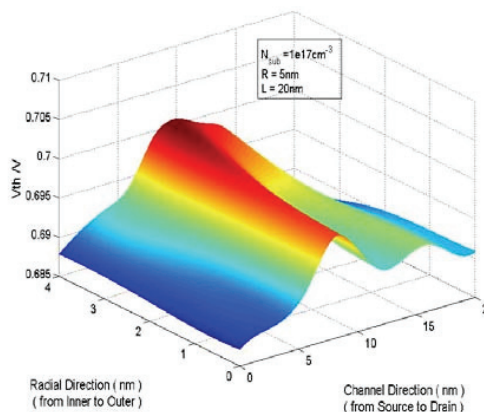


Figure3. Threshold voltage variation due to single acceptor dopant at different locations in channel. X-Y plane depict the position where the single dopant located.

Figure4 is a statistical result of threshold voltage variation in surrounding gate MOSFET. Since it is reported that fluctuation of threshold voltage follows Gaussian distribution statistically, we fit the data into Gaussian distribution and obtain a standard deviation of 53.1mV.

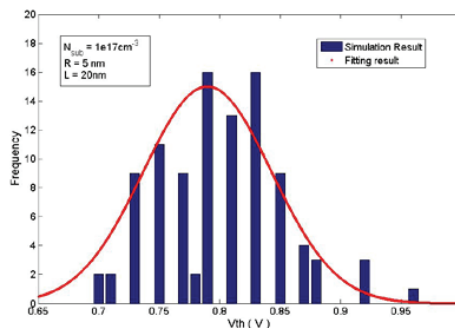


Figure4. Statistical variation in threshold voltage of surrounding gate MOSFET for random dopant fluctuation in

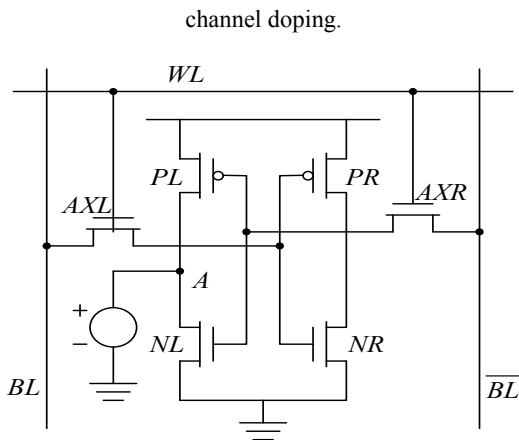


Figure5. 6T-SRAM cell based on surrounding gate MOSFET. BL and WL are bit line and word line. PL, PR, NL, NR, AXL and AXR represent Pull-up, Pull-down and Access transistors, respectively.

Figure5 is a schematic diagram of 6-T SRAM cell based on surrounding gate MOSFET. According to the previous result, we bring the random dopant fluctuation effect as a factor of threshold voltage into our compact model. As a result, we can reveal the impact of device parameter mismatch on the circuit stability. Figure6 and Figure7 show the statistical distribution of static noise margin of SRAM cell during hold time and write operation, respectively. The results indicate that, in spite of the aggressive fluctuation of threshold voltage, the SRAM cells made up of surrounding gate MOSFET do not amplify the variation. That is, they are not that sensitive to random dopant fluctuation.

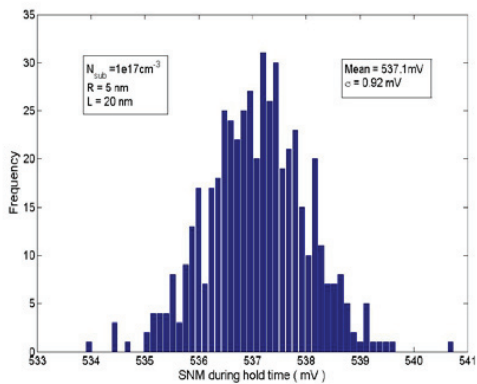


Figure6. Statistical variation in static noise margin of SRAM cell during hold time.

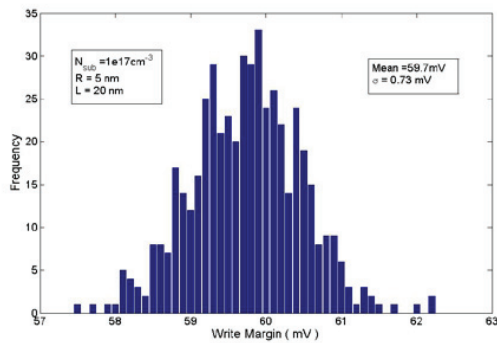


Figure7. Statistical variation in write margin of SRAM cell for random dopant fluctuation.

To further investigate the stability of SRAM cell, we also analyze the cell current during read and write operation. An N-curve is obtained by exerting a sweep voltage to the node A and measuring the current flowing into the node. I_{CRIT_RD} and I_{CRIT_WT} , which is defined as the peak current in N-curve for read and lowest current in N-curve for write respectively (Figure8), are also cell stability margin parameters [20]. Figure9 and Figure10 show the statistical study of I_{CRIT_RD} and I_{CRIT_WT} . As known in the analysis of static noise margin, the result also suggests an effective resistibility of surrounding gate MOSFET against device parameter variation and mismatch.

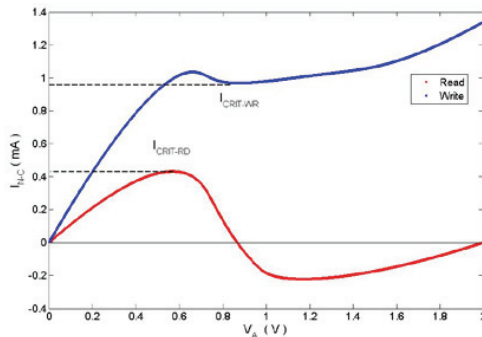


Figure8. N-curve for read and write and definition of critical current.

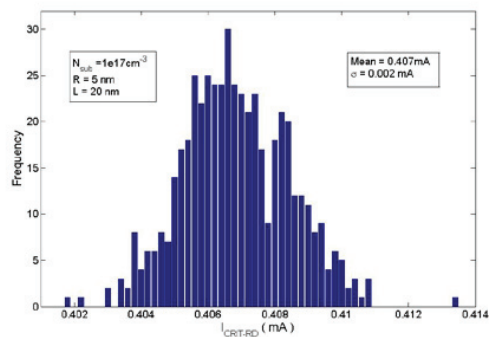


Figure9. Statistical variation in critical current for read due to random dopant fluctuation.

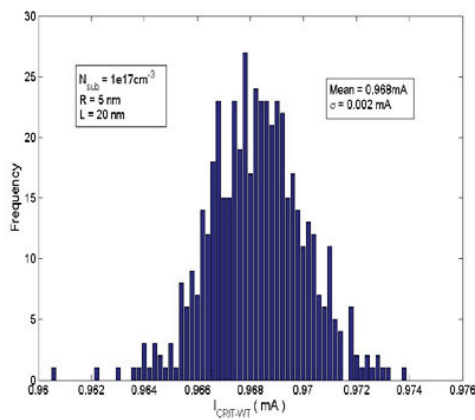


Figure10. Statistical variation in critical current for write due to random dopant fluctuation.

4 CONCLUSIONS

This paper provides a general method to study the impact of random dopant fluctuation on the device and circuit performances. A statistical simulation is presented to investigate the random dopant fluctuation effect on the threshold voltage variation of surrounding gate MOSFET and further on the SRAM stability. The results show an obvious variation of threshold voltage due to the limited channel volume. The circuit level simulation indicates that surrounding gate MOSFET can be a promising substitute for its resistibility to device parameter variation and mismatch due to the random dopant fluctuation.

ACKNOWLEDGEMENT

This work is supported by the Key Project of National natural Science Funds of China (61036004), the National natural Science Funds of China (61204043, 61274096), the Fundamental Research Project of Shenzhen Science & Technology Foundation (JC201005280670A), the Guangdong Natural Science Foundation (S2012010010533), the Shenzhen Science & Technology Foundation (CXB201105100089A), and the Fundamental Research Project of Shenzhen Science & Technology Foundation (JC201105180786A).

REFERENCES

[1] F.-L. Yang, D.-H. Lee, H.-Y. Chen, C.-Y. Chang, S.-D. Liu, C.-C. Huang, T.-X. Chung, H.-W. et al., VLSI Symp. Tech. Dig., pp. 196-197, 2004
 [2] F.-L. Yang, J.-R. Hwang, and Y. Li, in Proc. IEEE CICC, pp. 691-694, 2006
 [3] A. Asenov, A. R. Brown, J. H. Davies, S. Kaya, and G. Slavcheva, IEEE Trans. Electron Devices, vol. 50, no. 9, pp.

1837-1852, Sep. 2003.
 [4] S. Borkar, IEEE Micro, vol. 25, pp. 10-16, 2005.
 [5] S. Nassif, IEEE International Solid-State Circuits Conference, pp. 368-369, 2000
 [6] Leland Chang, David M. Fried, Jack Hergenrother, Jeffrey W. Sleight, et al., VLSI Symp. Tech. Dig., pp. 128-129, 2005
 [7] Nassif, S., Bernstein, K., Frank, D.J., Gattiker, A., Haensch, W., Ji, B.L., Nowak, E., Pearson, D., Rohrer, N.J., IEEE International Electron Devices Meeting, pp. 569-571, 2007
 [8] Varadarajan Vidya, University of California, Berkeley, PhD dissertation, pp. 70-74, 2007
 [9] Yu, S., Zhao, Y., Zeng, L., Du, G., Kang, J., Han, R., Liu, X., IEEE Trans. Electron Devices, vol. 56, no. 6, pp. 1211-1219, Jun. 2009.
 [10] L.-T. Pang and B. Nikolic, VLSI Symp. Tech. Dig., pp. 69-70, 2006
 [11] A. Asenov, A. R. Brown, J. H. Davies, S. Kaya, and G. Slavcheva, IEEE Trans. Electron Devices, vol. 50, no. 9, pp. 1837-1852, Sep. 2003.
 [12] Tomohisa Mizuno, Jun-ichi Okamura, Akira Toriumi, IEEE Trans. Electron Devices, vol. 41, no. 11, pp. 2216-2221, Nov. 1994
 [13] T. Ezaki, T. Ikezawa, and M. Hane, IEEE International Electron Devices Meeting, pp. 311-314, 2002
 [14] Yiming Li, Shao-Ming Yu, Jiunn-Ren Hwang, and Fu-Liang Yang, IEEE Trans. Electron Devices, vol. 55, no. 6, pp. 1449-1455, Jun. 2008
 [15] Jeng-Nan Lin, Kuo-Chih Chan, Chin-Yu Chen, Meng-Hsueh Chiang, Electron Devices and Solid-State Circuits, pp. 577-580, Dec. 2007
 [16] Meng-Hsueh Chiang, Jeng-Nan Lin, Keunwoo Kim, Ching-Te Chuang, IEEE Trans. Electron Devices, vol. 54, no. 8, pp. 2055-2060, Aug. 2007
 [17] Asen Asenov, IEEE Trans. Electron Devices, vol. 45, no. 12, pp. 2505-2513 Dec. 1998
 [18] D. J. Frank, Y. Taur, M. Ieong, and H. S. Wong, Symp. VLSI Tech. Dig., pp. 169-170, 1999
 [19] N. Sano, K. Matsuzawa, M. Mukai, and N. Nakayama, IEEE International Electron Devices Meeting, pp. 275-278, 2000
 [20] Jie Yang, Jin He, Feng Liu, Lining Zhang, Feilong Liu, Xing Zhang, Mansun Chan, IEEE Trans. Electron Devices, vol. 55, no. 11, pp. 2898-2906 Nov. 2008
 [21] Qiang Chen, Balasubramanian, S., Thuruthiyil, C., Gupta, M., Wason, V., et al., IEEE Solid-State and Integrated-Circuit Technology, pp. 448-451, 2008