An Analytic Potential Based Model for Gate-All-Around Nanowire Tunnel-FETs

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ABSTRACT

In this paper, an analytic potential based current model of the gate-all-around (GAA) silicon nanowire tunnel-FETs (NW-TFETs) is proposed based on the surface potential solutions at the channel direction and considering band to band tunneling (BTBT) efficiency. The 3-D Poisson's equation is solved to obtain the surface potential distribution in the partition regions along the channel direction for NW-TFET device and then a tunneling current model using Kane's expression is developed. The validity of the developed model is proved by the good agreement between the model predictions and TCAD simulation results.

***Keywords*:** Gate-All-Around (GAA); nanowire tunnel-FETs (NW-TFETs); band to band tunneling (BTBT); analytic model.

1 INTRODUCTION

Tunnel-FETs (TFET) has been got great attention in the semiconductor academic and industry fields in recent years for the superior performance in sub-threshold region. Compared with the conventional MOSFETs, TFET is competitive and chosen due to its high ON-OFF current ratio, below 60 mV/dec sub-threshold swing (SS) and low leakage power consumption [1-4]. However, TFETs have a small amount of band to band tunneling (BTBT) efficiency in the large band gap of silicon body leading to a low ON-current. To obtain the high ON-current and small SS, the GAA NW-TFETs is considered as an efficient device candidate. NW-TFET process technology and fabrication measures have been matured recently and many research papers have been published [4-6]. However, the compact model of NW-TFET for circuit performance prediction and simulation has made a few progresses. Most works only focus on NW-TFET empirical model development [5,9]. So far, there is no a complete analytical model of GAA NW-TFET for device scientists and circuit designers to test and simulation such a device based circuit performance.

In this paper, an analytical model of GAA silicon NW-TFETs has been developed based on the three-dimensional (3-D) potential solution and the Kane's expression. For observing the validity of the model and the different parameters impact on the device performance, we have also compared the analytical model prediction with the TCAD SenTaurus simulation results of the device to verify the model validity.

2 STRUCTURE AND MODEL

2.1 Structure of GAA NW-TFET

The Figure1 shows the structure of GAA TFET with silicon nanowire body. Figure1 (a) indicates 3-D structure of the n-channel GAA NW-TFET. Figure1 (b) represents the cross-section of the device with n-channel. In this paper, n-TFET is considered so the doping profile along the axis direction with the p^+ doping in source, n^+ doping in channel and drain. Band-to-band tunneling (BTBT) happens in the P/N junction at the source/channel region. Based on the drift-diffusion (DD) theory, the electrons are moved toward the drain thus the device can be divided into three regions: the depletion region Ⅰ, the tunneling region Ⅱ and the surplus channel region Ⅲ.

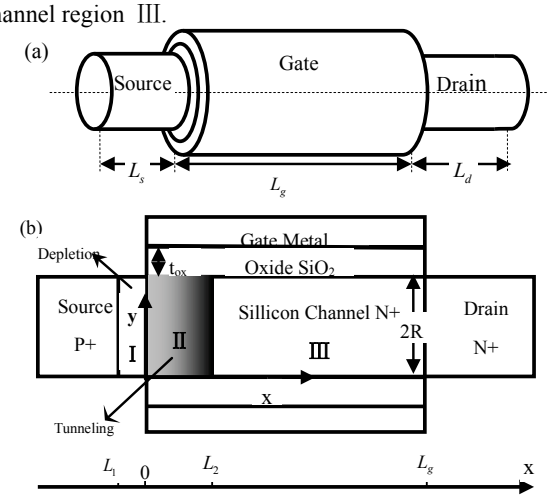

Figure 1: (a) 3-D structure of the n-channel GAA Silicon NW-TFET (b) Cross-section of the device and its division into a depletion region Ⅰ, a tunneling region Ⅱ and a conventional GAA MOSFET region Ⅲ.

Energy bands with electron and hole quasi-Fermi energies along the axis direction from the device simulator TCAD SenTaurus are demonstrated in Figure2. As shown, inversion

electrons transported to the region Ⅲ make a steep drain voltage drop in the reverse biased tunneling junction (region Ⅰ&Ⅱ) and it also makes that the potential profile is almost flat in the region Ⅲ because of the tunneling current. This suggests the surface potential of GAA NW-TFETs along the channel direction can be solved separately in the divided regions.

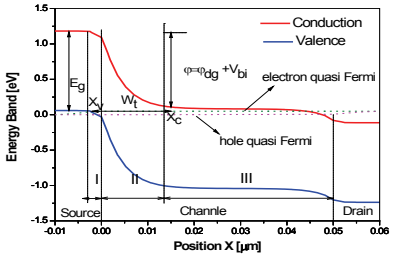

Figure 2: Energy band diagram with electron and hole quasi-Fermi energies along the axis direction from TCAD SenTaurus device simulation.

2.2 Potential Distribution Model

Only the depletion charge is considered at the sub-threshold region as discussed above, thus the Poisson's equation can be written as follows

$$\frac{1}{r}\frac{\partial}{\partial r}(r\frac{\partial\varphi(r,x)}{\partial r})+\frac{\partial^2\varphi(r,x)}{\partial x^2}=\frac{qN_i}{\varepsilon_{Si}} \tag{1}$$

where $\varphi(r,x)$ is the 2-D potential N_i is the different doping densities in partition regions. Since the potential is parabolic at the radius direction, it can be solved utilizing the 2-D polynomial approximation [8]:

$$\varphi(r,x)=\varphi_c(x)+\frac{C_{ox}(V_{gs}-V_{fb}-\varphi_s(x))}{2\varepsilon_{Si}R}r^2 \tag{2}$$

where $\varphi_c(x)$ and $\varphi_s(x)$ are the centre and surface potential relatively at the channel direction, and the relationship between them is:

$$\varphi_s(x)=\varphi_c(x)+\frac{2C_{ox}R(V_{gs}-V_{fb}-\varphi_s(x))}{\varepsilon_{Si}} \tag{3}$$

In this paper, it is assumed that the GAA NW-TFETs can be described by a modified Poisson's equation generating a characteristic length scale λ for the surface potential variation [7] as

$$\frac{\partial^2\varphi_s(x)}{\partial x^2}+\frac{\varphi_s(x)}{\lambda^2}=\eta \tag{4}$$

where $\eta=qN_i/\varepsilon_{Si}-(V_{gs}-V_{fb})/\lambda^2$ and $\lambda=\varepsilon_{Si}R/2C_{ox}$ is the characteristic length of GAA MOSFET structure. The general solution of (4) is

$$\varphi_s(x)=C_A\exp(\frac{x}{\lambda})+C_B\exp(-\frac{x}{\lambda})-\lambda^2\eta \tag{5}$$

In region Ⅰ ($-L_1\le x<0$), it is assumed the region is full depleted and an equivalent gate oxide thickness is $t_{ox}'=\pi t_{ox}/2$ for the gate fringing field [7,10]. Using the Taylor expansions, the equation is simplified:

$$\varphi_{s1}(x)\approx A_1(1+\frac{x^2}{2\lambda_1})-\lambda_1^2\eta_1 \tag{6}$$

where $\lambda_1=\sqrt{\varepsilon_{Si}R^2\ln(1+\pi t_{ox}/2R)/2\varepsilon_{ox}}$ is the characteristic length of region Ⅰ for the fringing GAA MOSFET structure and $\eta_1=qN_s/\varepsilon_{Si}-(V_{gs}-V_{fbs})/\lambda_1^2$.

The boundary conditions at the position $x=-L_1$ are: the surface potential is the silicon intrinsic voltage; the electric field is zero. Combining boundary conditions, the solution of surface potential in region Ⅰ is expressed as

$$\varphi_{s1}(x)=A_1(x+L_1)^2-V_{bi} \tag{7}$$

where $A_1=\frac{qN_{seff}}{2\varepsilon_{Si}}$, $N_{seff}=N_s-\frac{2\varepsilon_{ox}}{q}\cdot\frac{V_{gs}-V_{fbs}}{R^2\ln(1+\pi t_{ox}/2R)}$, $V_{fbs}=W_{fg}-W_{fs}$ is the flat-band voltage, W_{fg} and W_{fs} are the work functions. In (11), the value of L_1 is unknown.

In region Ⅱ ($0\le x<L_2$), the solution of (4) can be approximated as

$$\varphi_{s2}(x)=B_1\exp(\frac{x}{\lambda_2})+B_2\exp(-\frac{x}{\lambda_2})+V_{gs}-V_{fbs} \tag{8}$$

where $\lambda_2=\sqrt{\varepsilon_{Si}R^2\ln(1+t_{ox}/R)/2\varepsilon_{ox}}$ is the characteristic length of the region Ⅱ for the conventional GAA MOSFET structure. Using the boundary conditions at the position $x=-L_2$, the surface potential of the region Ⅱ can be solved as:

$$\varphi_{s2}(x)=(V_{gs}-V_{fbs})-[V_{gs}-V_{fbs}-(V_{bi}+\varphi_{dg})]\cdot\cosh[(x-L_2)/\lambda_2] \tag{9}$$

where the length L_2 is vague too. The following work is to solve the values of L_1 and L_2 using the boundary conditions between the region Ⅰ and Ⅱ: the surface potential and electric field are continuous.

Eventually, the compact solutions of the potential model are completed by the values of L_1 and L_2 as follows.

$$L_1=\sqrt{2\varepsilon_{Si}[\varphi_s(0)+V_{bi}]/qN_{seff}} \tag{10}$$

$$L_2=\lambda_2\cdot\cosh^{-1}(-\frac{V_{gs}-V_{fbs}}{V_{gs}-V_{fbs}-V_{bi}-\varphi_{dg}}) \tag{11}$$

$$\varphi_s(0)=(V_{gs}-V_{fbs}+\zeta)-\sqrt{(V_{gs}-V_{fbs}-V_{bi}-\varphi_{dg})^2+2(V_{gs}-V_{fbs})\zeta+\zeta^2+2V_{bi}\zeta} \tag{12}$$

where $\varphi_s(0)$ stands for the surface potential at $x=0$, $\zeta=qN_{seff}\lambda_2^2/\varepsilon_{Si}$. By bringing L_1 and L_2 into (7) and (9),

the compact 3-D analytical model of the potential distribution for the GAA silicon NW-TFETs is developed.

2.3 Analytic Current Model

Usually the BTBT is described using an introducing generation term in the drift and diffusion (DD) equation. When the BTBT current is dominating, the total current can be calculated by summarizing the charge generated in the device:

$$I_{ds} = q\int GdV = q\cdot\pi R^2\int Gdx \tag{13}$$

where G is the generation rate of carriers per unit volume per unit time and dV is an elementary volume of the device.

As is shown in Figure2, BTBT has different paths between the source/body junction, so the tunneling width $W_t = x_c - x_v$ must has a minimum value. The carrier generation rate due to BTBT has a peak value $G_{\max}$ along the tunnel path which has the minimum tunnel distance $W_{t,\min}$ because of the largest tunneling probability [12]. The minimum tunneling width can be obtained by

$$\begin{cases} \varphi_{s2}(x_c) = \phi_t \\ \varphi_{s1}(x_v) = \phi_t - E_g/q \\ dW_t/d\phi_t = 0 \end{cases} \tag{14}$$

where ϕ_t is the potential on the conduction band when the tunneling width is minimum, E_g is the band gap and it is assumed that the position x_v is in region Ⅰ and x_c is in region Ⅱ. From (18), the minimum tunneling width is

$$W_{t,\min} = L_2 + \lambda_2\cosh^{-1}\left(\frac{V_{gs}-V_{fbs}-\phi_t}{V_{gs}-V_{fbb}-\varphi_{dg}}\right) - \sqrt{\frac{\phi_t - E_g/q + V_{bi}}{A_1}} + L_1 \tag{15}$$

$$\phi_t = (V_{gs}-V_{fbs}) + 2A_1\lambda_2^2 - \sqrt{(V_{gs}-V_{fbb}-\varphi_{dg})^2 + (2A_1\lambda_2^2)^2 + 4A_1\lambda_2^2(V_{gs}-V_{fbs}-E_g/q+V_{bi})} \tag{16}$$

With the Kane's model [14], the generation rate is calculated by

$$G(E) = A\frac{E^D}{E_g^{1/2}}\exp\left(-\frac{BE_g^{3/2}}{|E|}\right) \tag{17}$$

where A and B are the parameters of Kane's model depending on the effective mass of valence and conduction bands and D takes a value of 2 [15].

When maximum electric filed across the tunneling junction is approximated as $|E| = E_g/(qW_{t,\min})$, the maximum carrier generation rate is obtained

$$G_{\max} = A\frac{E_g^{3/2}}{q^2}\frac{1}{W_{t,\min}^2}\exp\left(-\frac{W_{t,\min}}{\lambda_D}\right) \tag{18}$$

in which $\lambda_D = 1/(BqE_g^{1/2})$ is the tunneling decay length.

From Kane's model discussed above, it is observed the generation rate is an exponential function depending on the linear tunneling width, so it can assume that the electron generation rate satisfies the following function

$$G(x) = G_{\max}\exp\left(-\frac{|x-x_{c,\min}|}{\lambda_D}\right) \tag{19}$$

As a consequence, the equation (13) is easily computed

$$\int_{-\infty}^{+\infty} G(x)dx = \int_{-\infty}^{+\infty} G_{\max}\exp\left(-\frac{|x-x_{c,\min}|}{\lambda_D}\right)dx = 2\lambda_D G_{\max} \tag{20}$$

Finally using a current correction factor F_{fermi} produced from the Landauer's formula to make sure that the tunneling current is zero when the drain voltage is zero [13].

$$F_{fermi} = 1 - 2\frac{1}{1+\exp(qV_{ds}/\xi_n kT)} \tag{21}$$

where ξ_n is acquired from experiences. Thus the tunneling current model is given by

$$I_{ds} = 2q\cdot\pi R^2\lambda_D G_{\max}F_{fermi} \tag{22}$$

3 RESULT AND DISCUSSION

The analytical model is validated by comparing the model prediction results with the TCAD simulations.

Figure3 shows the surface potential profiles $\varphi_s(x)$ along the channel direction at different gate and drain voltages. In figure3 (a) it is evident that with the reduction of gate voltage, the length of depletion region L_1 becomes smaller and the length of tunneling region L_2 becomes larger. It is observed that in Figure3 (b) with the decrease of drain voltages, the length of tunneling region L_2 becomes smaller, leading to a significant increase in the tunneling probability which can remarkably enhance the drain current.

The transfer characteristics of $I_{ds}-V_{gs}$ in a log scale are presented in Figure4 (a) and the output characteristics of $I_{ds}-V_{ds}$ in a linear scale are shown in Figure4 (b). Good agreements between the developed model and device simulations are achieved in all the regions.

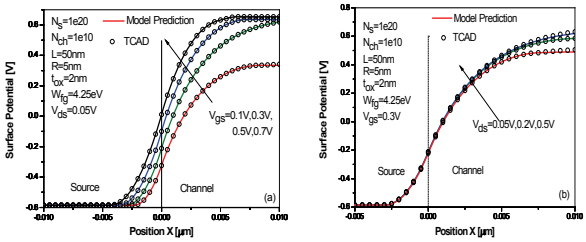

Figure 3: The surface potential profile φ_s along the channel direction in a GAA NW-TFET (a) with different gate voltages V_{gs} and the same drain voltage: V_{ds}=0.05V (b)with different drain voltages V_{ds} and the same gate voltage: V_{gs}=0.3V

Figure5 (a) indicates the dependence of minimum tunneling width $W_{t,\min}$ on gate voltage V_{gs}. With gate voltage increased the minimum tunneling width has a reduction

although a small gate bias is needed for the tunneling to happen. It clearly certifies the reduction of tunneling distances depending on decreasing V_{gs} observed in Figure3 (a).The dependences of off-state current I_{off} and sub-threshold swing (SS) on the drain voltage V_{ds} are shown in Figure5 (b). SS is much smaller than the traditional MOSFET limit 60mV/dec and both I_{off} and SS increase most linearly.

$$SS = \frac{dV_{gs}}{d\log(I_{ds})} \quad (35)$$

Figure 4:

The reason is that in GAA NW-TFETs with larger drain voltage, the tunneling width is also increased which reduces the BTBT electron generation rate and the tunneling current.

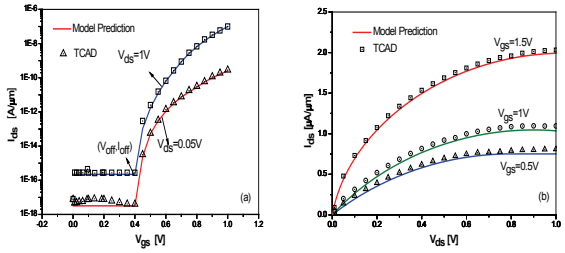

Figure 5: (a) The transfer characteristics of $I_{ds} - V_{gs}$ in a log scale with different drain voltages, (b) The output characteristics of $I_{ds} - V_{ds}$ in a linear scale with different gate voltages for a GAA-TFET device.

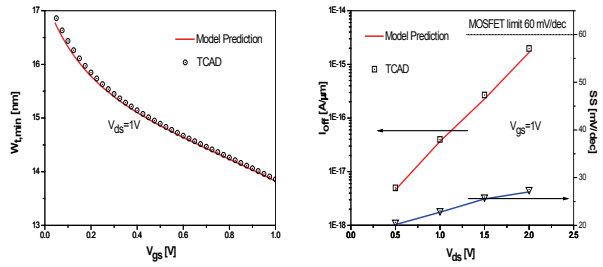

Figure 6: The dependences of (a) minimum tunneling width $W_{t,\min}$ on the gate voltage V_{gs} (b) off-state current I_{off} and sub-threshold swing SS on the drain voltage V_{ds}.

4 CONCLUSION

An analytical current model based on the surface potential solution for the GAA silicon NW-TFETs device has been developed in this paper. The model predictions are validated by using the TCAD results, and the good agreements between the model calculation and the TCAD simulations are widely found. It can be expected this potential based current model can be also extended to study the charge model and some transport properties for the GAA NW-TFETs if more parasitic effects are considered.

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