NQS Modeling of Independent DG MOSFET by Relaxation Time Approximation Approach

ABSTRACT

In this paper, we investigate the applicability of the Relaxation Time Approximation (RTA) based approach for the NQS modeling of independent double gate (IDG) MOSFET, which is a non-trivial exercise due to the anomalous inter-gate transcapacitance frequency response. We model the NQS effect in an IDG MOSFET by employing the RTA based approach along with the novel piecewise linearization methodology and validate the model against the TCAD simulation for different bias conditions. Proposed model predicts the NQS behavior accurately for any amount of gate oxide thickness asymmetry for a frequency range $2f_t$ in saturation and $10f_t$ in linear region (where ft is the cut-off frequency) and successfully reproduce the anomalous frequency dependency of the inter-gate transcapacitances. The model is also successfully implemented in a professional circuit simulator through Verilog-A interface and good convergence is observed during different standard circuit simulation.

***Index Terms*—Compact modeling,Piecewise linearization, Non Quasi Static (NQS) effect, Relaxation time approximation, Double Gate (DG) MOSFET**

I. INTRODUCTION

INDEPENDENT Double GATE (IDG) metal-oxide-semiconductor field- effect transistors (MOSFETs) has attracted much attention as a replacement to bulk MOSFET for future semiconductor industry due to its ability to modulate the threshold voltage and transconductance dynamically [1]. IDG Configuration owing to its enhanced functionality can be used for many novel circuit applications [2]- [4]. Though we have some models [5] [6] [7] proposed for IDG Configuration but these models were for the configuration where the back gate oxide thickness is much higher than the front gate oxide thickness so that always front gate is the dominant gate controlling the functionality of device and the other gate is used just for controlling the threshold voltage. The model [5] was developed for a particular set of device manufactured at LETI, CEA. But in real scenario as the device dimensions are scaling down, the oxide thickness will also get scaled down accordingly and the assumption that front gate will always be the dominant gate will not hold true. Therefore, our model is not based on any such assumption and holds true for any amount of asymmetry in oxide thickness. Our model is developed in such a way that no matter which gate is the dominant gate it is able to predict the device behaviour accurately.

With advancement in CMOS applications for RF design, we need a compact model for high frequency RF applications. In order to model the device at high frequency, we need to model the non-quasi static effects in MOSFETs. The modelling of non-quasi static effects in MOSFETs can be done by two approach: Relaxation Time Approximation (RTA) and Continuity Equation (CE). Recently we have proposed a continuity equation based NQS model for independent double gate MOSFET [8]. These models are physical based and therefore, very accurate but they are computationally expensive and therefore, in this work we examine the applicability of RTA based modelling for IDG MOSFETs. RTA based modelling involves empirical parameters which needs to be calibrated and therefore, is less accurate at higher frequencies. However, RTA based model is very simple, promises faster convergence and is easy to implement in a circuit simulator [9].

We show here that with some judicial assumptions, it is possible to apply RTA technique for accurate modelling of the IDG MOSFET. Though, we have used the same phenomenological equations as used in [9] for modelling the drain and total inversion charge, but the same equation cannot be used for modelling the terminal charges across gate. So in order to model the gate terminal charges we have used piecewise linearization technique [10]. IDG MOSFET shows a very anomalous frequency dependency of inter-gate transcapacitances. It is expected that with increase in frequency transcapacitances should decrease but in IDG MOSFET, it is observed that the inter-gate transcapacitance increases with increase with frequency. Our model is able to predict this anomalous behaviour of inter-gate transcapacitance very accurately. Proposed model is verified against TCAD simulations and successfully implemented in a professional circuit simulator through Verilog-A interface.

II. MODEL DEVELOPMENT

The conventions used in this paper are: $t_{ox1(2)}$ is the oxide thickness of first(second) gate, t_{si} is the thickness of the silicon body, $C_{ox1(2)}$ is the oxide capacitance per unit area of first(second)-gate defined as $\epsilon_{ox}/t_{ox1(2)}$, ϵ_{si}, ϵ_{ox} are the permittivities of Si and SiO_2 respectively, q is the elementary charge, β is the inverse thermal voltage, n_i is the intrinsic carrier density, $B = 2qn_i/\beta\epsilon_{si}$, L is the channel length, $\psi_{1(2)}$ are the Si/SiO_2 surface potentials at first(second) gate, V is the electron quasi-Fermi potential (channel potential) and μ is the effective mobility. The effective gate voltage is defined as $V_{g1(2)} = V_{g1(2)_{applied}} - \delta\phi_{1(2)}$, where $V_{g1(2)_{applied}}$ is the voltage applied at gate terminals and $\delta\phi_{1(2)}$ is the work function difference of the gate material. The inversion charge density at any point along the channel is denoted by Q_i, which is sum of two components Q_{i1} and Q_{i2} expressed as $Q_{i1(2)} = C_{ox1(2)}(V_{g1(2)} - \psi_{1(2)})$. The terminal charges at

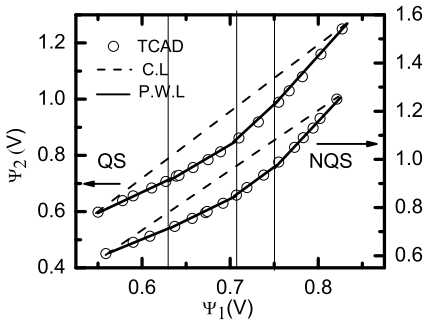

Figure 1. Relationship between ψ_1 and ψ_2 depicting piecewise linearisation assumption. V_{gs1} is swept from 1 V to 1.5 V at ramp rate of 10 V/ns. V_{ds} is kept at 1.5 V and V_{gs2} at 0.7 V. C.L stands for conventional linearization. P.W.L stands for piecewise linearization.

first gate, second gate, source and drain are denoted as Q_{G1}, Q_{G2}, Q_S and Q_D respectively. In all the discussion that follows, any variable with subscript 's' refers to its values at source end and with subscript 'd' refers to its value at drain end.

In order to model NQS effect in MOSFETs with RTA approach we model the NQS terminal charges from the QS terminal charge using the the following phenomenological equation [9] [12] [13]

$$\frac{dQ_{T,nqs}}{dt} = -\frac{Q_{T,nqs} - Q_{T,qs}}{\tau} \tag{1}$$

where Q_T represents the terminal charges and T represents the terminal. τ is known as 'relaxation time' which has two components: drift and diffusion and semi-empirically modeled as [13]

$$\tau = \left[\left[\frac{L^2 k_{diff}\beta}{\mu}\right]^{-1} + \left[-\frac{Q_I k_{drift}}{I_d}\right]^{-1}\right]^{-1} \tag{2}$$

where, I_d is the DC drain current.

It is worth noting that k_{diff} and k_{drift} are model parameters, which are not a part of QS model, and thus requires additional measurement for their calibration. Initially for bulk MOSFET [12] [13], RTA was applied to all terminals. However, recently it is argued [9] that RTA should only be applied to the drain (Q_D) and the total inversion charge (Q_I) in order to obtain superior accuracy especially at $V_d = 0$ condition. In this work we have followed the same argument. For developing NQS model for IDG MOSFET with RTA approach we need to compute $Q_{G1,nqs}$ and $Q_{G2,nqs}$ individually. For this purpose we have developed following methodology:

Step 1: Using the 'piecewise linearization concept' [10] we divide the channel into 'N' segments and compute the QS terminal charges. It is established in [10] that ψ_1 and ψ_2 holds a linear relationship inside any segment in QS condition. In NQS condition also as shown in Fig. 1 it is observed from TCAD simulations that ψ_1 and ψ_2 holds a linear relationship inside each segment. So, the linearisation co-efficients of surface potentials for each segment under

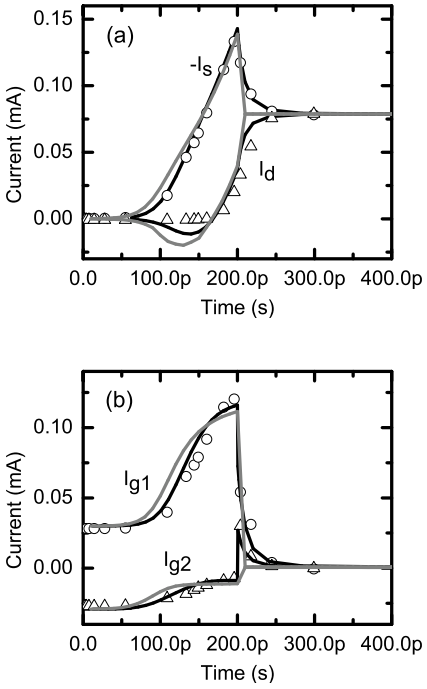

Figure 2. (a) Drain (I_d) and source (I_s) ; (b) gate terminal currents ($I_{g1} and I_{g2}$) predicted by proposed model and the TCAD simulation. A step voltage from 0 to 1V is applied to gate1 with a rise time of 200 ps and V_{ds} is kept at 1V. Black Line represents proposed NQS model and Gray line represent QS model.

NQS condition remains almost same as the QS condition.

Step 2: We then apply the RTA (1) on $Q_{D,qs}$ and $Q^j_{I,qs}$ to obtain $Q_{D,nqs}$ and $Q^j_{I,nqs}$, where $Q^j_{I,qs}$ is the total inversion charge for the j^{th} segment.

Under NQS condition, in each segment ψ_2 can be linearised w.r.t. ψ_1 as

$$\psi_2 = \lambda^j_1 \psi_1 + \gamma^j_1 \tag{3}$$

where,

$$\lambda^j_1 = \frac{\psi^{y^{j-1}}_{2,qs} - \psi^{y^j}_{2,qs}}{\psi^{y^{j-1}}_{1,qs} - \psi^{y^j}_{1,qs}} \tag{4}$$

$$\gamma^j_1 = \psi^{y^{j-1}}_2 - \lambda^j_1 \psi^{y^{j-1}}_1 \tag{5}$$

Here, y^{j-1} and y^j represents the left-most and right-most coordinates of the particular segment and ψ^{y^j} denotes surface potential values at y^j. Now for any j^{th} segment,

$$Q^j_{I,nqs} = -W. \int_{y^{j-1}}^{y^j} (C_{ox1}(V_{g1} - \psi_1))\, dy -$$

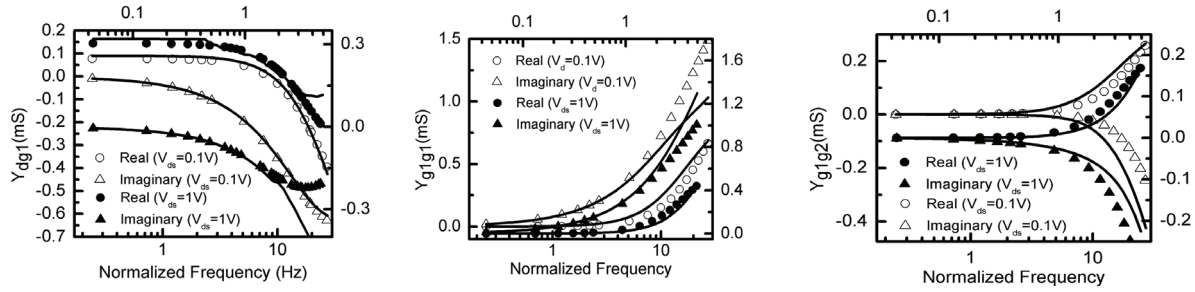

Figure 3. Small signal characteristics: (a) Y_{dg1}. (b) Y_{dg2}. (c) Y_{g1g1}. (d) Y_{g1g2}. (e) Y_{g2g1}. (f) Y_{g2g2}. (g) Y_{dd}. (h) Y_{g1d}. (i) Y_{g2d}. Solid Symbol represent saturation region ($V_d = 1V$) and Open symbol represent linear region ($V_d = 0.1V$). V_{gs1} is kept at 1V and V_{gs2} is kept at 0.5V. Real part is represented by circle symbol and Imaginary part is represented by triangle symbol. Line represents proposed model and Symbols represents TCAD results.

$$W \int_{y^{j-1}}^{y^j} (C_{ox2}(V_{g2} - \psi_2))\, dy \tag{6}$$

Applying the linearization (3) we obtain

$$Q^j_{I,nqs} = -W. \int_{y^{j-1}}^{y^j} (C_{ox1}(V_{g1} - \psi_1))\, dy -$$

$$W \int_{y^{j-1}}^{y^j} \left(C_{ox2}(V_{g2} - \lambda^j_1 \psi_1 - \gamma^j_1)\right) dy \tag{7}$$

Evaluating this we obtain,

$$Q^j_{I,nqs} = -WC_{ox1}V_{g1}.(y_j - y_{j-1}) - WC_{ox2}V_{g2}.(y_j - y_{j-1})$$

$$+W \int_{y^{j-1}}^{y^j} \left(C_{ox1}\psi^j_1\right) dy + W \int_{y^{j-1}}^{y^j} \left(C_{ox2}(\lambda_{1j}\psi^i_1 + \gamma_{1j})\right) dy \tag{8}$$

$$\frac{Q^j_{I,nqs}}{C_{ox1}W(y_j - y_{j-1})} + V_{g1} + \left(\frac{C_{ox2}}{C_{ox1}}V_{g2}\right) - \left(\gamma_{1j}\frac{C_{ox2}}{C_{ox1}}\right)$$

$$= \frac{1}{(y_j - y_{i-1})} \int_{y^{j-1}}^{y^i} \psi^j_1 dy + \frac{C_{ox2}}{C_{ox1}} \frac{\lambda_{1j}}{(y_j - y_{j-1})} \int_{y^{j-1}}^{y^j} \psi^j_1 dy \tag{9}$$

Now introducing $\overline{\psi_1} = \frac{1}{L_j}\int_{y_{j-1}}^{y_j} \psi_1(y)dy$ where $L_j = y_j - y_{j-1}$and doing some further simplification we finally get

$$\overline{\psi_1} = \frac{\left\{\frac{Q^j_{I,nqs}}{C_{ox1}WL_j} + V_{g1} + \left(\frac{C_{ox2}}{C_{ox1}}V_{g2}\right) - \left(\gamma^j_1 \frac{C_{ox2}}{C_{ox1}}\right)\right\}}{\left(1 + \frac{C_{ox2}}{C_{ox1}}\lambda^j_1\right)} \tag{10}$$

Step 3: The NQS gate terminal charges for each segment now can be computed as

$$Q^j_{G1,nqs} = C_{ox1}WL_j(V_{g1} - \overline{\psi_1}) \tag{11}$$

Table I
EXECUTION TIME

Circuits	QS time (s)	NQS time (s)	Ratio ($\frac{\text{NQS}}{\text{QS}}$)
Ripple Adder	6.79	9.18	1.35
8-bit counter	3.97	9.47	2.38
75-stage ring oscillator	31.69	68.22	2.13

$$Q^j_{G2,nqs} = -Q^j_{G1,nqs} - Q^j_{I,nqs} \tag{12}$$

After evaluating the respective terminal charges for each segment the total terminal charge of the device can be found by the summation of charges across all these segments. The accuracy of the proposed model has been verified against TCAD simulation in the next section.

III. RESULTS AND DISCUSSIONS

We have implemented the RTA based models for IDG devices in a professional circuit simulator through its Verilog-A interface [14]. For IDG device, we require $N+1$ number of additional nodes, where N is the number of channel segments used in the 'piecewise linearization technique'. In this work we have used $N = 4$ with the same break-points proposed in [10]. All the results for the RTA models shown in this manuscript is obtained from the circuit simulator [14].

We have validated our model against the 2-D TCAD simulation results [15] for devices having gate oxide thickness asymmetry: t_{ox1} = 1nm, t_{ox2} = 1.5nm, t_{si} = 10nm, L = 1um, W = 1um . The cut-off frequency (f_t) is calculated as $f_t = \frac{g_m}{2\pi C_{g1g1}}$ and are found to be 2.27 GHz at $V_{gs} = V_{ds} = 1$V and 0.41 GHz at $V_{gs} = 1; V_{ds} = 0.1$V (here g_m is the gate transconductance and C_{g1g1} is gate1-gate1 capacitance). The channel is kept undoped and source-drain doping is taken as 10^{20} cm^{-3}. We use constant mobility of $300cm^2/V - s$ both in TCAD simulation and proposed model. We use $k_{diff} \simeq 0.0999$ and $k_{drift} \simeq 0.079995$ for this configuration.

Fig. 2 shows the transient behaviour of the terminal current for IDG MOSFET while a ramp voltage with rise time of 200 ps from 0 V to 1 V is applied at gate terminal. In order to ensure NQS condition the rise time is chosen to be smaller than transit time (440ps) of the carriers . It is observed that currents across Source, Gate1 and Gate2

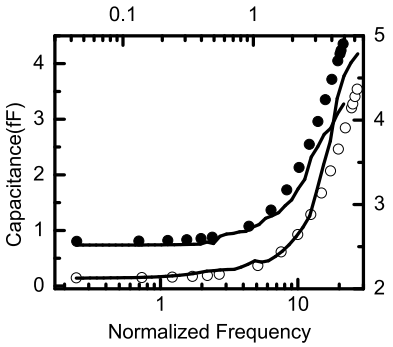

Figure 4. C_{g1g2} predicted by proposed model and TCAD in both linear and saturation region. V_{gs1} is kept at 1V and V_{gs2} is kept at 0.5V. Y at V_{ds}=1V is plotted against top x-axis which is normalized to 2.27 GHz and Y at V_{ds}=0.1V is plotted against bottom x-axis which is normalized to 0.41 GHZ.

matches exactly with TCAD simulation while Drain current shows small deviation. But still, RTA based model predicts the terminal currents more accurately as compared to QS model when high ramp rate voltage is applied across gate terminal. Fig. 3 shows some of the independent Y parameter characteristics predicted from RTA based NQS model. Y parameter characteristics in both linear and saturation region is verified against TCAD simulation. We have calibrated the k_{diff} and k_{drift} parameters against Y_{dg1} values. The RTA based NQS model is found to predict the device behaviour quite accurately at least for a frequency range of $2f_t$ in saturation region and $10f_t$ in linear region which is used for most practical applications. The most interesting NQS feature of IDG MOSFET is the frequency response of its inter-gate capacitance (C_{g2g1} or C_{g1g2}) as shown in Fig. 4. It is well known that transcapacitances of MOSFETs decrease with increase in frequency. However, we found that the inter-gate transcapacitance of IDG MOSFET increases with frequency and proposed model is in good agreement with the TCAD data. It is observed that all the other 14 transcapacitances decrease with increasing frequency, while C_{g2g1} or C_{g1g2} increases with frequency for any bias conditions. In independent gate configuration, terminal charge across gate1 is dominantly affected by gate1 bias and the terminal charge across gate2 is dominantly affected by gate2 bias. Therefore, with increase in bias frequency across one gate, the rate of change of terminal charges across source, drain and the respective gate decreases as the charges across these terminals are not able to respond fastly to the changing frequency. However, as the charge across second gate does not depend directly on the first gate bias and also in order to maintain charge neutralization in the device, the rate of change of terminal charge across second gate increases and therefore, inter-gate capacitance increases. Table 1 shows the execution time observed from implementation of different standard circuits. It is observed that the model shows good convergence for all the circuits implemented.

IV. Conclusion

We propose a new set of RTA based NQS model for IDG by taking into account the fact that any gate can be the dominant gate. It is shown that the proposed model is predicting both large and small signal device characteristics very accurately for any amount of gate oxide thickness asymmetry. The model is also able to predict the anomalous frequency dependence of inter-gate transcapacitance and therefore, can be used for most of the practical applications. Proposed models have been verified against TCAD simulation. The model has been implemented in a professional circuit simulator and found to show good convergence.

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