SOI-Multi-FinFET: Impact of Fins Number multiplicity on Corner Effect

A.N. MOULAI KHATIR, A. GUEN-BOUAZZA , B. BOUAZZA

Abstract — SOI-Multifin-FET shows excellent transistor characteristics, ideal sub-threshold swing, low drain induced barrier lowering (DIBL) without pocket implantation and negligible body bias dependency. In this work, we analyzed this combination by a three-dimensional numerical device simulator to investigate the influence of *fins* number on corner effect by analyzing its electrical characteristics and potential distribution in the oxide and the silicon in the section perpendicular to the flow of the current for SOI-single-fin FET, three-fin and five-fin, and we provide a comparison with a Tri-gate SOI Multi-FinFET structure.

Keywords — SOI, FinFET, Corner effect, Dual-gate, tri-gate, Multi-Fin FET.

I. Introduction

THE current drive in a multi-gate-FET is essentially equal to the sum of the currents flowing along all the interfaces covered by the gate electrode. It is, therefore, equal to the current in a single-gate device multiplied by the equivalent number of gates (a square cross section is assumed) if carriers have the same mobility at each interfaces.

For instance, the current drive of a double-gate device is double that of a single-gate transistor of equivalent gate length and width. In triple-gate and vertical double-gate structures all individual fins have the same thickness and width. As a result the current drive is fixed to a single, discrete value, for a given gate length.

To drive larger currents multi-fin devices are used. The current drive of a multi-fin MOSFET is equal to the current of an individual fin multiplied by the numbers of fins (also sometimes referred to as "fingers" or "legs").

We will compare the current drive of a single-gate, planar MOSFET with that of a multi-fin multigate-FET having the same gate area, $W \times L$ (Fig.1). We suppose that the planar FET is made on (100) silicon and that the surface mobility is μ_{top}. Let us also assume the multigate-FET is made on (100) silicon and that the top surface mobility is μ_{top}. The sidewall interface mobility may be different from the top mobility, depending on the sidewall crystal orientation, usually (100) or (110), and is noted μ_{side} [1].

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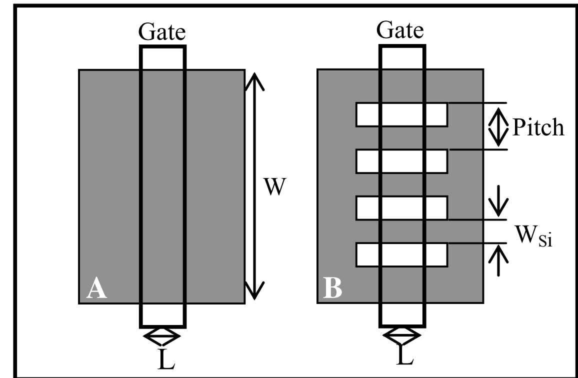

Figure.1: A. Single-gate, planar MOSFET Layout; B. Multi-fin multigate FET layout.

Fig.2 show the measured I_d-V_d characteristics for a three-gate SOI-Multi-FinFET structure with (a) single-Fin and (b) five-Fins (b) by TCAD Silvaco simulator for a 20 nm thick, 40 nm high Silicon fin, 25 nm for channel length and 2 nm for the gate oxide thickness with several gate voltages 1.2, 1.5, 1.8, and 2V.

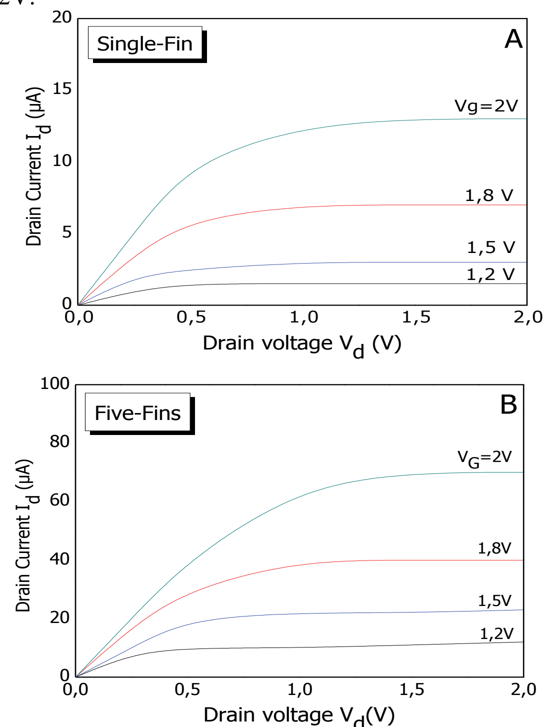

Figure 2: Measured I_d-V_d characteristics for a three-gate SOI-Multi-FinFET structure with a (a) single-Fin; (b) five-Fins.

It is apparent that 5 times of the drain current is accurately obtained in the five-Fin device compared with that of in the single-Fin device at a fixed gate voltage and drain voltage.

Considering a pitch P for the fins, the current in the multigate device is given by:

$$I_D = I_{D0}\frac{\theta\mu_{top}W_{fin} + 2\mu_{side}t_{Si}}{\mu_{top}P} \quad (1)$$

Where I_{Do} is the current in the single-gate, planar device, W_{fin} is the width of each individual fin, t_{si} is the silicon film thickness (Fig.3); $\theta=1$ in a triple-gate device where conduction occurs long three interfaces, and θ=0 in a FinFET where channels are formed at the sidewall interface only [2]

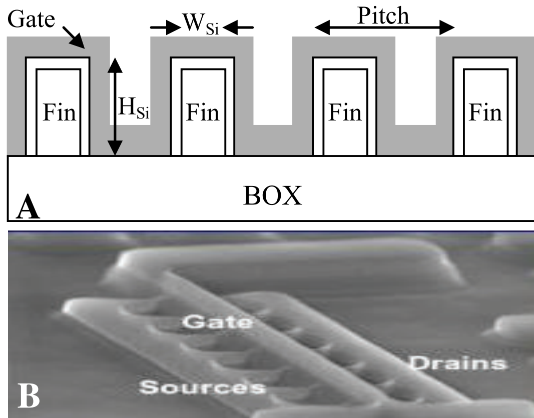

Figure 3: (a) Cross-section of a Multifin-FET with four-Fins, (b) SEM Picture of the fins.

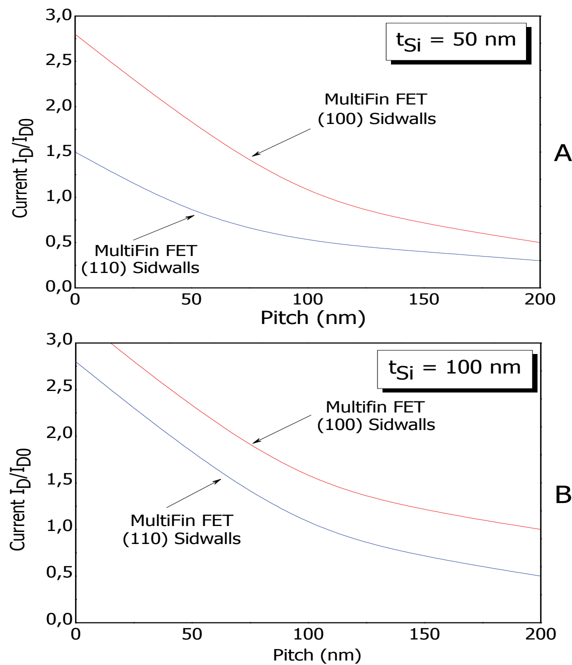

Figure 3: Normalized current drive of a triple-gate SOI-FinFET vs. pitch. W_{fin}= pitch/2; The (100)-interface electron mobility is 300 cm^2/Vs and the (110)-interface mobility is 150 cm^2/Vs.
a) t_{si} =50nm; b) t_{si}=100nm.

Fig.3 shows the current drive in a multi-fin, tri-gate SOI-FinFET as a function of the fin pitch, P, assuming $W_{fin}=P/2$. The fin height is either 50nm or 100 nm. The drain current is normalized to that of a single-gate planar device occupying the same silicon real estate. This figure shows that a tri-gate SOI multi-fin FET can deliver significantly more current with a small enough fin pitch can be achieved. It also shows the impact of device orientation ((100) or (110) sidewalls) on current drive. The current drive can be increased by increasing the fin height, t_{si}, but the use of tall fins often raises difficulties during device processing.

II. CORNER EFFECTS

Devices with a triple, quadruple, Π or Ω gate structure present a non planar silicon/gate oxide interface with corners. It has been known for long that premature inversion can form in at the corners of SOI structures because of charge-sharing effects between two adjacent gates. In particular, one can observe the presence of two different threshold voltages (one in the corners and at the top or sidewall Si-SiO2 interfaces), as well as a kink in the sub-threshold $I_D(V_G)$ characteristics [3].

The presence of corners can degrade the sub-threshold characteristics of a device. Avoiding that problem is the reason why there is a hard mask at the top of SOI-FinFETs. To complicate the matter, the radius of curvature of the corners has a significant impact on the device electrical characteristics and can decide whether or not a different threshold voltage will be measured at the corners and at the planar interfaces of the device.

In classical single-gate SOI MOSFETs, corner effects are purely parasitical. They are not part of intrinsic device operation and they can usually be eliminated by increasing the doping concentration in the corners. In a multigate device, on the other hand, the corners are part of the intrinsic transistor structure. Therefore, it is worth understanding the relationship and interaction between currents in the corner currents and currents in the planar surfaces of the device [4].

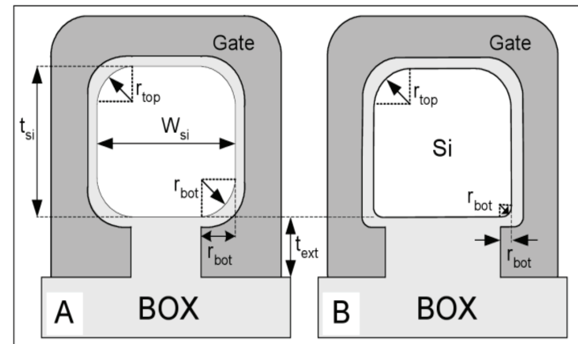

Figure 4: Ω-gate device cross section.
A: $r_{top} = r_{bot}$; B: $r_{top} \neq r_{bot}$

To illustrate the corner effect, let us use the Ω-gate device shown in Fig.4. The thickness and width of the device are tsi and W_{fin}, and the radius of curvature of the top and the bottom corners is noted r_{top} and r_{bot}, respectively. The gate oxide thickness is 2 nm, and t_{si}=W_{fin}=30 nm. Because the gate material is N+ poly-silicon, high doping concentrations have to be used to achieve useful threshold voltage values (N-channel device).

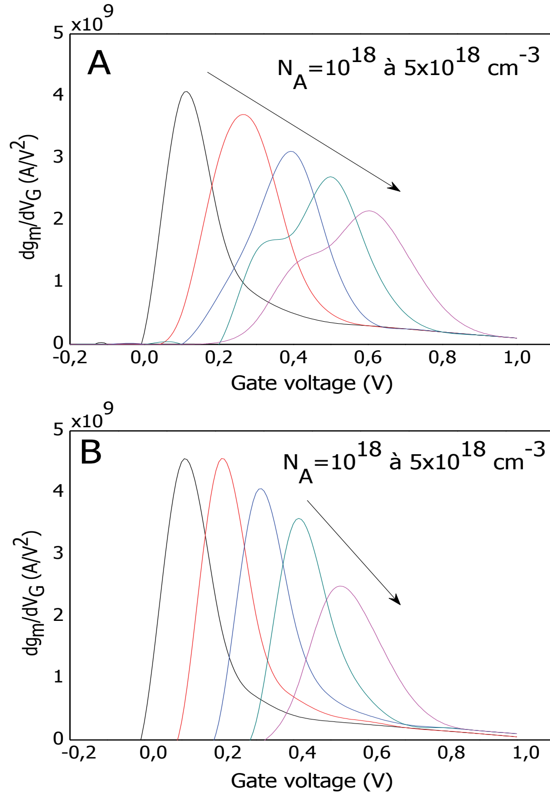

Figure 5: dg_m/dV_G in the Ω-gate device.
A: $r_{top} = r_{bot} = 1nm$; B: $r_{top} = r_{bot} = 5nm$

Fig.5 presents the simulated dg_m/dV_G characteristics of the device at $V_{DS}=0.1V$ for different doping concentrations and a top and bottom corner radius of curvature of either 1 or 5 nm. The dg_m/dV_G characteristics have been used by several authors to identify the different threshold voltage(s) single- and double-gate SOI devices [5-6]. The humps of the dg_m/dV_G curve correspond to the formation of channels in the device (i.e. they correspond to threshold voltages).

When the corner radius of curvature is equal to 1nm the devices with the lowest doping concentrations exhibit a single hump, indicating that both corners and edges build up channels at the same time. The devices with the more heavily doped channels have two humps. The first of these two humps corresponds to inversion in the top corners, and the second one to top and sidewall channel formation.

When the corner radius of curvature is 5 nm, a single peak is observed for all doping concentrations, which indicates that premature corner inversion has been eliminated. In that case all devices reach a sub-threshold swing of 60 mV/decade over a significant range of their sub-threshold current. The corner effect can thus be eliminated by using either a low doping concentration in the channel, or corners with a large enough radius of curvature [7-8]. The general manufacturing trend being to use undoped channels in conjuction with a midgap metal gate, the corner effect is not expected to pose any problem to the use of MuGFET technology [9-10].

III. SIMULATION AND RESULTS:

We first optimize a single-finFET which then will be used as a base transistor for a multi-fin structure [11].

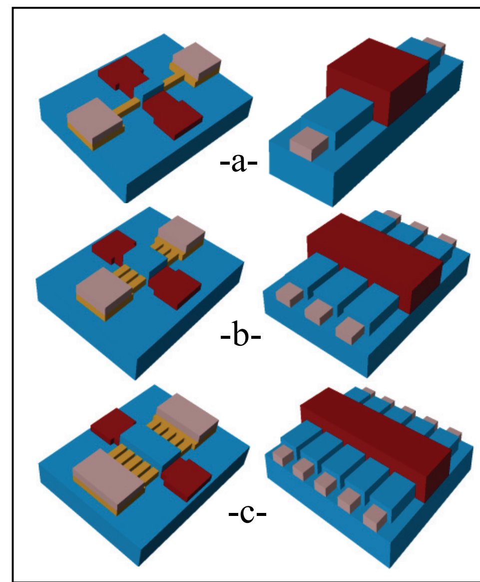

Figure.6: 3D Structure of SOI-Multi-FinFET
a) Single-fin; b)Triple-fins; c) Five-fins.

The bulk is lightly doped 10^{18} cm^{-3} to avoid the dopant fluctuation.

With extensive calibrated TCAD Silvaco simulations [12], we present results for a comparison of the potential in the oxide and the silicon in the section perpendicular to the flow of the current for various numbers of *fins* from n=1fin to 3 fins and finally 5 fins in the case of dual-gate SOI-Multifin FET and we will compare these results with the case of tri-gate SOI-Multifin FET as shown in (fig.7.a.b.c). In the case of SOI-Single-FinFET, the potential distribution shows that the potential barrier between the source and the drain is higher, and that the barrier is the highest in the middle of the channel which should push the electron flow from source to drain to the corners of the fin. Further, electric field from the substrate electrode penetrates into the channel decreasing the potential in the fin. This increases the source to-drain potential barrier in every part of the channel. It can be seen

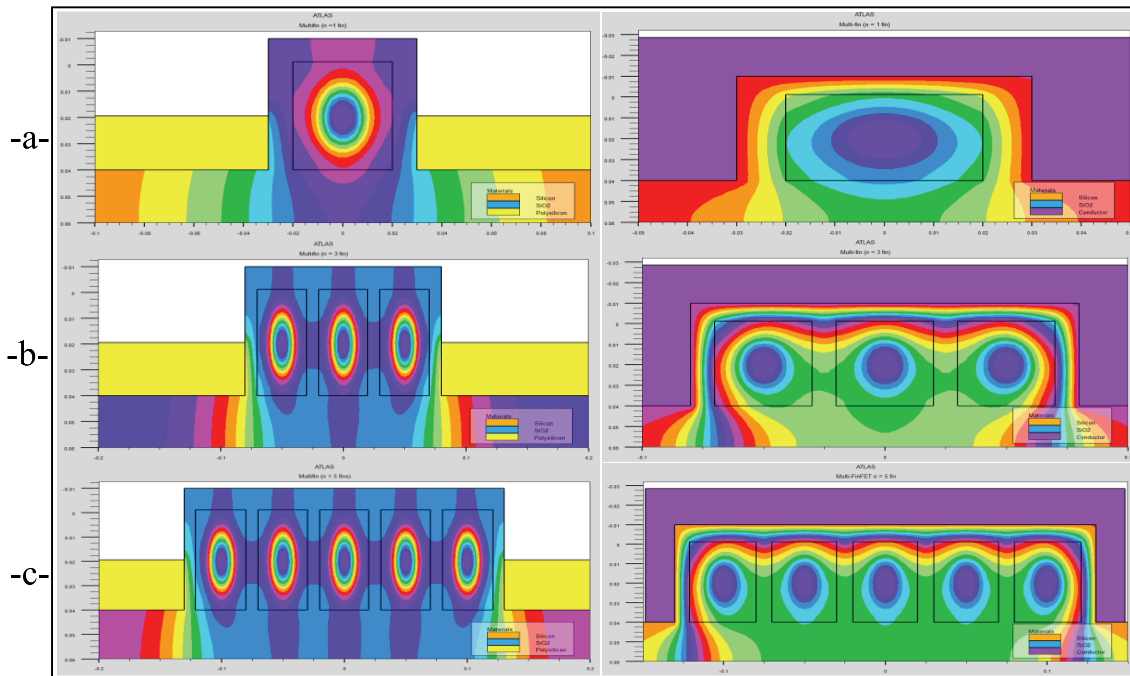

Figure 7: Potential in the oxide and the silicon in the y-z section for the Dual-gate and tri-ga Multifin-FET (Vgs=0.5V) -a-Single fin -b- Three fins - c-Five fins

that the barrier rises from top to the bottom of the channel and it is the highest in lower part of the channel, around the bottom of the gate. Higher barrier at the bottom and in the middle will force the electron flow to the top of the fin, or to be more precise, to the upper corners of the fin. For both Dual and Tri-gate SOI-Single FinFET, it can be seen that the current flow is pushed to four corners (4-corner effect), this means that if we will increase the number of fins, we will multiply these four corners effects by this new number, which will result an on-state drain current *n* times higher than single fin where *n* is the new fin number.

Although Dual and Tri-Gate SOI-Multi-FinFETs have a completely identical doping in the active area, the performance of the tri-gate transistor is better than the one of the double gate transistor, because the Tri-gate has a slightly higher on-current, but simultaneously a much lower leakage current compared to the Dual-Gate, because the upper part of the fin also contributes to the total current of the open double gate transistor.

A slight enhancement of the current in the corners of the fin in the open transistors is observed for both transistors considered.

IV. Conclusion

Although SOI-FinFETs have aforementioned advantages, they also bring some other disadvantages, such as corner effect in relation to the multiple-gate structure. In contrast, the corner effect improves the performance of the FinFETs since the on-current is enhanced at the corners and the leakage current is suppressed. Since the corners effect is located at each fin, with increasing the fin number the influence of the corner effect became stronger and the leakage currents is more higher in shallow trench isolated CMOS transistors. Due to positive influence of the corner effect, the triple gate wrap around design of the SOI-Multi-FinFET appears to be more advantageous in comparison to the double gate design

Acknowledgment

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