Nanomagnet Logic - From Concept to Prototype

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ABSTRACT

Nanomagnet Logic (NML) systems comprise several subsystems including nanomagnets, clock lines, input and output devices, and layers for concentrating the clocking and coupling fields. This paper summarizes progress made at Notre Dame toward a practical, completely integrated NML CMOS-compatible system.

Keywords: Nanomagnet Logic, Boolean logic, NML

1 INTRODUCTION

Nanomagnet Logic (NML) is a paradigm for performing digital logic functionality that uses the magnetization of single-domain nanomagnets to encode logical values [1]. NML uses in-plane magnetic coupling between nanomagnets of roughly 60 nm × 90 nm × 20 nm to compute and transfer digital information. Figure 1 shows the components of the planned NML system comprising the magnets on the surface of a "clock" line that is clad on three sides by a magnetic yolk (much like word and bit lines in magnetic random access memory (MRAM)), an input device, output device, and (not shown) field-concentrating enhanced permeability dielectric (EPD) layer on the surface. Briefly, the magnetization is set in one of

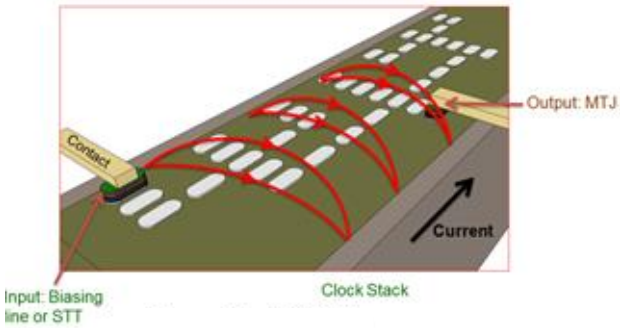

Fig. 1. Complete NML system.

two possible directions (corresponding to each binary logic value) along the easy (long) axis of an input magnet. The resulting field couples to the adjacent array of magnets, which under the control of the field set by the underlying clock line, settles into a final ground state that reflects the result of the computation. Logical functions, including "wires" of magnets for transferring data, logical AND, OR and majority gates, and fanout for variously shaped nanomagnets have already been demonstrated [2]. NML promises to be a low-power [3] alternative or adjunct to CMOS, but only if the magnets can be parallel pipelined with the least amount of power dissipation in the clock lines.

Several hurdles toward a completely integrated NML system remain, but are yielding to current development efforts. This paper summarizes progress in each of the critical areas, namely input, clocked control of data flow, output, and most importantly, reduction of system power.

2 CLOCK LINES

A full NML system consists of a set of pipeline stages, each controlled by a clock line [2], which is a copper conductor whose purpose is to reset, or null, the magnetization states. In our case, the clock lines are buried in the substrate, and the nanomagnets are fabricated on the surface. The field due to the current in the clock line passes through the magnets on the surface. The magnets are arranged so that the field re-evaluates the nanomagnets by bringing them into the metastable, high energy, null state. The clock line size, arrangement, and excitation current are design parameters that can be altered to achieve the desired clocking field with the lowest possible power consumption for a particular NML circuit.

The clock lines are fabricated using a copper damascene process, similar to that which has been used to make copper interconnects since the 1990's [4]. First, the clock line patterns are etched, and an insulating SiO_2 layer is grown on the wafer by thermal oxidation. Then, a CoFe cladding layer is sputter deposited. The thickness of this cladding layer can vary from 10 to 50 nm depending on the spacing of the clock lines and required clocking field. An additional SiO_2 layer is deposited by plasma enhanced chemical vapor deposition to insulate the CoFe cladding layer from the subsequent Cu seed layer to avoid corrosion during Cu electroplating. After the Cu seed layer is sputtered, the bulk Cu is deposited by electroplating. The wafer is then polished by chemical mechanical polishing (CMP). The Cu overburden is removed using an aggressive slurry at a high material removal rate. The insulating SiO_2 layers and CoFe cladding layer are then removed with a slurry having a low pH and a small particle size, both of which aid in smoothing the clock line surface. Fabrication is completed by applying spin-on hydrogen silsesquioxane (HSQ) on the entire sample to aid in planarization and adhesion, and the resultant clock lines have a surface roughness of less than 2 nm. A cross-sectional SEM image of the clock lines

currently being used in experiments, cut by focused ion beam, is shown in Fig. 2. This clock line can provide ample nulling field, and is the base on which to build a realizable NML circuit with a field-coupled input and magnetoelectric output.

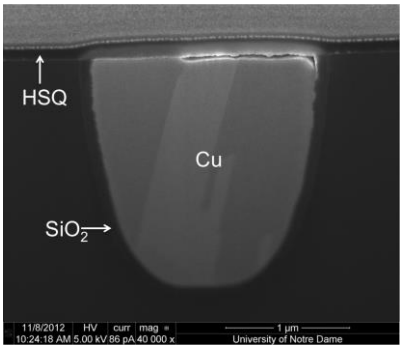

Fig. 2. Electron micrograph of clock line cut by focused ion beam. The shading in the copper line is due to grain boundaries.

3 FIELD-COUPLED INPUTS

An NML system requires electronic input for two reasons: to enable arbitrary control over each input nanomagnet without affecting the rest of the system, and to facilitate interfacing between CMOS and NML. To this end, we have developed a field-MRAM-inspired field-coupled input scheme [5,6]. This scheme relies on the control of the state of individual magnets through the interaction of two orthogonal fields. In NML, all nanomagnets reside on top of a clock line such that the current controlled global clock field aligns the magnetization of all nanomagnets, including the inputs, along the hard axis.

To enable field-coupled input control, a bias line is placed on top of each input nanomagnet to provide a small bias field along the easy-axis direction. The bias field tilts the energy landscape of the underlying nanomagnet, thus creating a bias-dependent preferred direction. With the application of synchronized, overlapping clock and bias fields, the input nanomagnet settles in the direction set by the applied bias field. This scheme offers ease of fabrication and the ability to control thicker input nanomagnets (20-30 nm). Such a magnetoelectric input could lead to the realization of a hybrid CMOS-NML system. Figure 3a shows the schematic of an NML system where the clock line and bias lines are integrated with a slant-based [7] OR gate. Each input to the OR gate is provided with a dedicated bias line, allowing the device to be tested for all possible input combinations. Figure 3b shows the fabricated structure showing clock lines, logic elements and bias lines on top of input magnets. The dimensions, as well as the shape, of the nanomagnetic logic elements are chosen according to micromagnetic simulations in order to reduce the possibility of erroneous output states. The fabricated devices were tested by applying overlapping current pulses through the clock line and bias lines. The SEM and magnetic force microscopy (MFM) images in Fig. 3c show the magnetization of the output magnets of two OR gates for all input combinations. It is evident that the devices under test settled into the correct output states for all inputs for both devices.

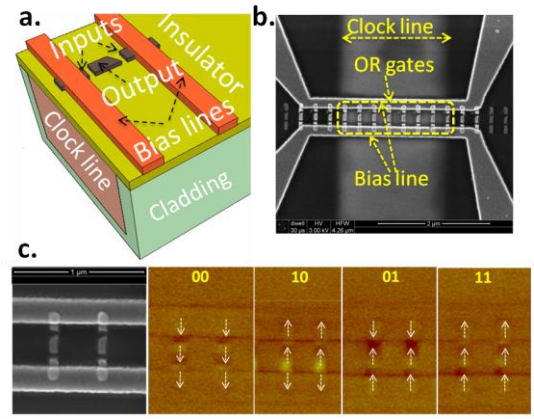

Fig. 3. Field-coupled input scheme. a) Schematic showing a slant-based OR gate with integrated clock line and bias lines. b) SEM image of a fabricated structure. The clock line runs vertically in the background. NML elements are fabricated on top of the clock line. Two bias lines run across several input magnets, allowing simultaneous testing of multiple gates. c) SEM and MFM showing the devices under test for all four input combinations.

4 NML OUTPUT

Magnetic tunnel junctions (MTJ) and giant magnetoresistance (GMR) based nanoscale spin valves can be used as outputs for NML [2]. Free layers of these spin valves are required to be free from any parasitic biasing in order to ensure proper NML operation [8]. Such biasing in free layers arises from the magneto-static and orange-peel [9] coupling between the fixed and free layer. The inherent roughness of NML clock lines can aggravate such parasitic biasing. Although the magnetoresistance (MR) ratio of a GMR stack is lower compared to that of an MTJ, the thicker metallic spacer layer of a GMR stack can reduce the unwanted coupling, and make GMR-based spin valves more attractive as an NML output. To this end, we have developed and incorporated an $Ir_{22}Mn_{78}/Co_{70}Fe_{30}/Cu/Co_{70}Fe_{30}$-based GMR structure over a planarized NML clock line.

A UHV DC magnetron sputtering system was used to prepare the stacks on native oxide over a (100) Si substrate. Exchange bias (EB) was introduced to the fixed layer by field cooling the stack from 230 deg. C to room temperature in 1 hour under a field of 400 mT and high vacuum. Magnetic and electrical characterization of the stacks were performed using a vibrating sample magnetometer (VSM)

and a probe station customized to perform R-H measurement. The stack was optimized in terms of process pressure, seed layer and Cu spacer layer thickness. The thickness of the IrMn layer and CoFe fixed layers were kept constant at 10 nm and 3 nm, respectively. By lowering the process pressure from $3x10^{-3}$ mbar to $2x10^{-3}$ mbar, we increased the EB field from 50 mT to 120 mT for a 5 nm Cu seed layer. Energetic atoms at low pressure are capable of forming larger grains in the films, which increases the EB. We observed that a Cu seed layer on top of the Ta buffer layer introduces higher EB (120 mT) than a Ru seed layer (65 mT) of the same thickness. XRD study of the films confirms that the Cu seed layer enhances the (111) texture in IrMn, resulting in a higher EB field. Reduction of the Cu seed layer thickness from 5 to 2 nm increases the current-in-plane (CIP) MR ratio from 1.25% to 4.5%, but reduces the bias field to 75 mT. Thinner Cu spacer layer improves the MR ratio. However, we did not reduce the thickness below 3 nm to avoid any RKKY type coupling between the fixed and the free layers. Finally we integrated the optimized GMR structure over a Si substrate with planarized NML clock lines.

Figure 4 shows a STEM image of the stack over an NML clock line and magnified HRTEM image of the same in the inset. Figure 5 shows M-H and R-H curves of the integrated GMR stack. We observed an EB field of 75 mT and CIP MR ratio of 3.35% for the integrated stack. A marginally reduced MR of the integrated stack can be attributed to the higher roughness of the planarization oxide on the clock structure than that of the native oxide. Fabrication of nanoscale output devices from the integrated stack is in progress.

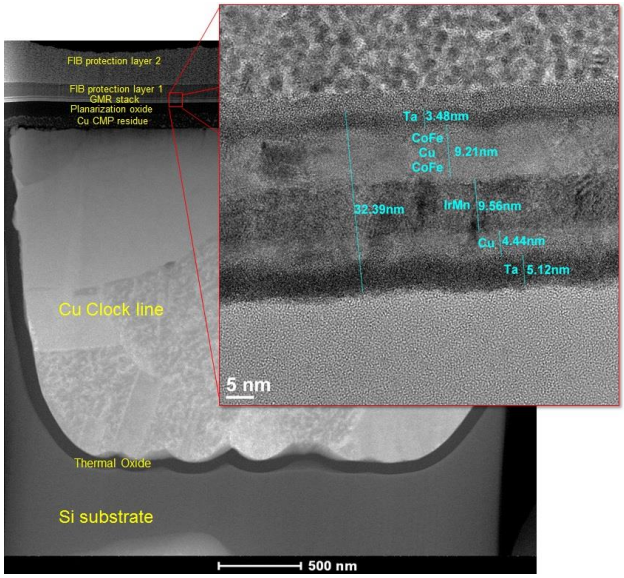

Fig. 4. Cross sectional STEM image of a Ta (5 nm) / Cu (5 nm)/ $Ir_{22}Mn_{78}$ (10 nm) / $Co_{70}Fe_{30}$ (3 nm) / Cu (3 nm) / $Co_{70}Fe_{30}$ (3 nm) / Ta (5 nm) GMR stack over NML clock line and magnified HRTEM image of the stack in the inset.

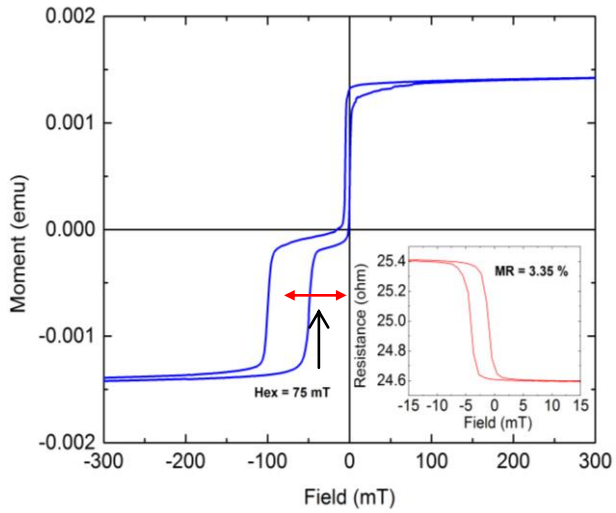

Fig. 5. M-H and R-H (inset) curve of the optimized GMR stack over planarized oxide on the clock

5 POWER REDUCTION IN NML

Central to NML operation, hard-axis fields are required to place the magnets into a metastable state for re-evaluation, a process referred to as "nulling" or "clocking." The energy to produce the clock field is the most significant component of the entire power budget of NML circuits, and our goal is to reduce this energy. We employ two methods to do so.

5.1 Intermagnet space reduction

Placing nanomagnets closer together increases intermagnet field coupling, which reduces the required clock field and lowers the overal energy requirement as the square of the clock field strength, which is proportional to current in the clock line. By utilizing double e-beam exposure technology [10] we were able to reduce the

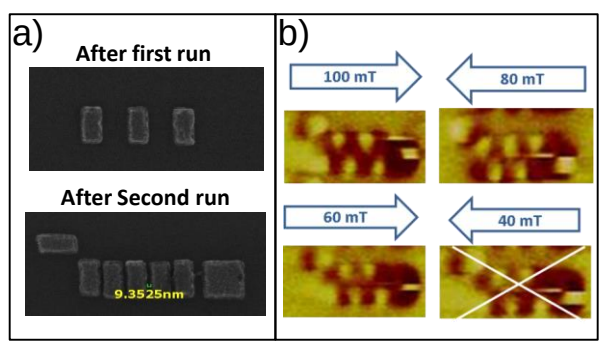

Fig. 6. a) SEM image of nanomagnets after first and second run of fabrication, resulting in a 5-magnet-long dataline with sub-10-nm spacing. b) MFM image of the dataline after application of different clock-fields. The minimum clock-field was 60 mT.

intermagnet spacing from 30 nm to 10 nm. Such reduction of spacing reduced the clock field from 125 mT to 60 mT, a 52% reduction, which translates to a 77% reduction in power. Figure 6 summarizes the results.

5.2 Enhanced Permeability Dielectrics

We can furthur reduce the clock field by utilizing enhanced permeability dielectrics (EPD). During clocking, some flux lines pass through the nanomagnets, while others leak into air; if we can redirect these leaked flux lines so that they also cut through the nanomagnets, then the clocking efficiency can be improved through the requirement of lower nulling fields. This can be done by covering the nanomagnets with EPDs [11], which in our case is an MgO dielectric matrix with embedded CoFe particles.

Figure 7 is a schematic of the cross section of the layers. Using e-beam lithography, reactive etching, e-beam evaporation and lift-off, a sample of nanomagnets embedded in EPDs can be made.

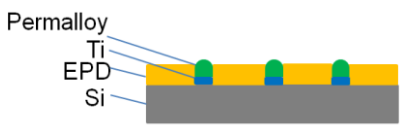

Fig. 7. Schematic of the sample structure.

The sample was tested for its nulling clock field with transverse magnetization metrology (TMM) [12], which measures the Y component of magnetization (M_y) when the field is applied along the X axis.

Figure 8 shows an M_y vs. H_x curve measured by TMM, with insets showing schematics of magnetization states at different fields. Starting from H_x = 0, each nanomagnet points up, so there is a large M_y component. As H_x increases in the rightward direction, it biases the magnetization of the nanomagnets to the left, so M_y decreases. When H_x = 89 mT, M_y = 0, indicating that all the magnetization is fully saturated in the X-axis direction. This is the case when all the nanomagnets are set along the hard axis during the NML clocking process, so the nulling clock field of this sample is 89 mT. As H_x approaches zero, each nanomagnet has an equal opportunity to turn up or down randomly, so the overall magnetization averages to zero. This is why from State B to State C, M_y is a constant and zero. When H_x increases in the leftward direction, it biases the nanomagnets to the left, and M_y remains zero.

Previously, we tested a sample with nanomagnets (60 nm × 120 nm × 20 nm) solely for their nulling clock field, and the results showed that the field is 160 mT [12]. As shown in the above experiment, when nanomagnets are embedded in EPDs, this field reduces to 89 mT, which is a 44% reduction in clock field, translating to a potential 70% reduction in power dissipation in NML.

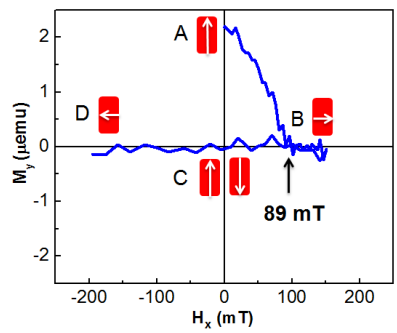

Fig. 8. M_y vs. H_x (TMM) curve of the sample.

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