

# Single-crystalline 3C-SiC thin-film on large Si substrate for photonic applications

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## ABSTRACT

This paper presents an unique low-temperature chemical vapor deposition process developed at Griffith University that enables the hetero-epitaxial growth of uniform single-crystalline cubic silicon carbide thin-film on very large silicon substrate. This technology, combined with the unique properties of silicon carbide, opens new opportunities for photonic applications on silicon.

**Keywords:** LPCVD, hetero-epitaxy, Silicon carbide, SiC-on-Si, photonic, GaN-LEDs

## 1 INTRODUCTION

### 1.1 SiC: Properties and applications

Silicon carbide (SiC) for many years has driven a strong interest from various fields of engineering. Initially used as an abrasive material and as a very hard ceramic for mechanical applications, research on SiC is now mainly focused on its unique properties as a semiconductor material and for micro-systems [1]. Its high radiation and chemical tolerance, high thermal conductivity (between Copper and Diamond), high hardness and Young's modulus mean that SiC is an ideal material for microelectromechanical systems (MEMs) technology, especially in the case of applications in harsh environments such as in the outer space or in nuclear plants [2]. SiC is also a material of choice for power electronics thanks to its high electron saturation velocity ( $\sim 2 \cdot 10^7$  cm/s) and high critical electric field ( $> 2$  MV/cm) opening the route to efficient power devices working at high temperatures, high voltages and with ultra-fast switching speed [3].

Less is known regarding the promising potential of SiC for optical-based applications. Because of its wide band gap ( $\sim 3$  eV), SiC has been largely investigated in the past for the fabrication of visible light sources. Despite its indirect band-gap strongly limiting its efficiency as a light emitter, SiC was used for the first light emitting diode (LED) demonstration in 1907 and then commercial blue LEDs were made of SiC until the development of the more efficient gallium nitride (GaN) LEDs technology at the end of the 20<sup>th</sup> century [3]. Nowadays, SiC is still an important material for optoelectronics as the lack of GaN substrates combined with the low lattice mismatch of SiC with GaN ( $\sim 3\%$ ) and AlN ( $\sim 1\%$ ) has motivated its use as a substrate

for the hetero-epitaxial growth of high-power GaN-LEDs and GaN laser diodes. Finally, recent years have seen a growing interest for SiC-based photonic applications. As a wide band-gap semiconductor, SiC is transparent over the visible and infrared wavelengths which is of importance for photonic applications based on low-loss waveguides and ultrahigh quality factor cavities in this spectrum range [4]. Such photonic structures could also be used to enhance the performance of GaN-LED grown on SiC. Furthermore, two photons absorption which impairs Si and gallium arsenide (GaAs) photonic devices working in the telecommunication range does not occur in SiC, opening the development of efficient SiC photonic structures for harmonic generation, parametric down conversion and Raman amplification [5]. It is also worth mentioning the recent discovery of atom-like single defect centres in SiC with long coherence time at room temperature which could lead to the development of single-photon sources and quantum devices [6].

### 1.2 Hetero-epitaxy of SiC on Si

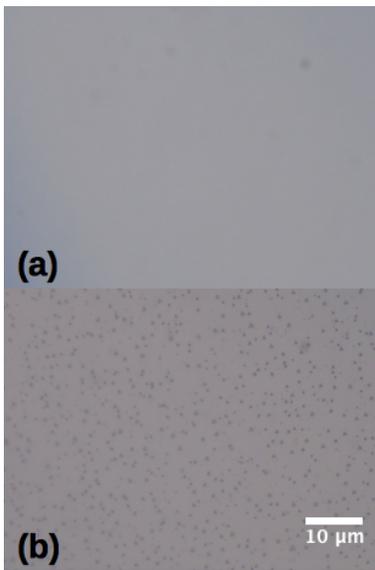
The development of SiC-based applications has been hampered by the high cost and limited size of SiC substrates. To date, 150mm SiC wafers are available but in limited production scale and cost a few thousand dollars [7]. As an alternative approach, growth of SiC on large Si substrate has been investigated since the last fifty years [8]. Silicon wafers can be produced in very large size, up to 300mm, with very good quality and a relatively low price of typically a few hundred dollars thanks to a large economy of scale. Consequently, hetero-epitaxy of SiC on Si can provide low cost single-crystal SiC template on very large wafers. Integration of SiC on Si wafers also brings several important advantages. First, this would enable a better compatibility with CMOS factory plant, leading to substantial cost saving in investment and device processing. Also, Si is much easier to process than SiC, meaning that standard Si processing, such as substrate removal, can be easily adapted and new functionalities can be integrated by using the Si properties, especially for MEMs applications.

However, SiC-on-Si approach comes with a limitation as only the cubic crystal structure, also called 3C-SiC, can be grown on Si. This is due to the limitation on the maximum growth temperature imposed by the relatively low melting point of Si, at 1420°C. Fortunately, 3C-SiC has similar properties to the standard hexagonal-form SiC

## 2 SIC-ON-SI GROWTH AT GRIFFITH UNIVERSITY

Hetero-epitaxy of the SiC films is achieved in a hot-wall vertical low-pressure chemical vapor deposition (LPCVD) reactor, jointly developed between Griffith University and SPTS Technologies [11]. This unique reactor was designed to accommodate up to  $50 \times 300\text{mm}$ -diameter Si wafers per run. Contrary to the standard concurrent supply epitaxy (CSE), where both silicon source gas and carbon source gas are provided simultaneously, an alternating supply epitaxy (ASE) was used, meaning that Si and C atoms were supplied in alternative pulses. In a previous work ASE was found to provide a better thickness uniformity, a lower density of defects and a better morphology than the CSE growth [12].

The growth procedure used here is similar to the one described by Wang *et al.* [12] and is as followed. After standard cleaning, Si wafers are loaded into the chamber via an atmospheric nitrogen purged loadlock that avoids contamination of the reactor on wafer loading and unloading. The load lock not only minimizes unwanted contaminations but also significantly reduces the overall process time. After wafer loading, the reactor temperature is ramped from  $500^\circ\text{C}$  to  $1000^\circ\text{C}$ , and a low flow of  $\text{SiH}_4$  (1.5sccm) is sent into the chamber with the dual purpose of removing any native oxide on the Si and then add a thin epitaxial Si layer on the substrate surface. After 30minutes, the  $\text{SiH}_4$  flow is stopped and the chamber is cooled down to  $750^\circ\text{C}$  for the following carbonisation step. First, a flow of  $\text{C}_3\text{H}_6$  (10sccm) at a pressure of 2Pa is introduced to convert the Si substrate surface into SiC from  $750^\circ\text{C}$  to  $900^\circ\text{C}$ , followed by ramping the temperature from  $900^\circ\text{C}$  to  $950^\circ\text{C}$  with continuous flowing of  $\text{H}_2$  and  $\text{C}_3\text{H}_6$  at a pressure of 40Pa. Optimization of the carbonisation process was found to be crucial to prevent the formation of Si voids. This is demonstrated on Figs. 1 where two microscope images of samples having undergone respectively an optimised carbonisation and a non-optimised carbonisation are shown. One can easily notice the large Si-voids obtained with the non-optimised process (Fig. 1(b)), while no such defects are visible when the optimized carbonisation process is used



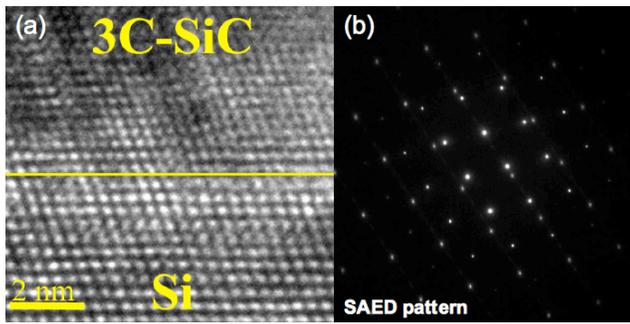
Figures 1 - Optical images of Si samples following an optimised carbonisation step (a) and a non-optimised carbonisation step (b).

polytypes, such as 6H-SiC and 4H-SiC, commonly used for SiC-based device fabrication. Another drawback in the hetero-epitaxy of SiC on Si is the large lattice mismatch of  $\sim 20\%$  between Si and SiC, as well as the  $\sim 8\%$  thermal expansion mismatch, resulting in stacking faults and other extended defects in the grown SiC layer. The growth of SiC on Si also induces defects in the silicon side at the interface, such as voids and pits going down deep into the Si substrate, because of the out-diffusion of Si from the substrate and its incorporation into the SiC growth process.

The presence of these extended defects is a serious limitation for device development, and therefore important research works have been initiated with the purpose to reduce their density and their size. The two-step approach, first introduced by Nishino & *al.* [9], has been so far the most successful progress in the reduction of the defect densities. This two-step approach consists of creating a buffer layer by carbonisation of the silicon surface, then followed by the 3C-SiC growth. The buffer layer, also called “carbonisation layer” is formed by reaction of the silicon surface with a carbon-base gas and is composed of polycrystalline 3C-SiC. The purpose of this buffer layer is to accommodate the lattice mismatch between the Si substrate and the single-crystalline 3C-SiC layer, allowing to grow thicker films with a much lower density of defects. However, this two-step approach does not prevent the formation of Si voids beneath the interface [10]. We present here a further progress in the hetero-epitaxy growth of 3C-SiC on Si. A low temperature deposition combined with an alternating gas supply approach was used to successfully suppress the formation of Si voids and achieve SiC growth with very high thickness uniformity and low surface roughness on very large Si wafers. We also demonstrate the potential of these high-quality SiC thin-films for photonic and MEMs applications.



Figure 2 – Optical image of a 51nm-thick 3C-SiC layer grown on a 300mm Si(100) wafer.



Figures 3 – (a) Cross-sectional HRTEM image of a 3C-SiC/Si(111) interface observed along the [110] direction of electron incidence and (b) its corresponding SAED pattern.

(Fig. 1(a)). After the carbonisation step, the bulk epitaxial growth of 3C-SiC is performed, cycle by cycle, with alternate supply of SiH<sub>4</sub> and C<sub>3</sub>H<sub>6</sub>. Each cycle consists of the following four steps: 1) the supply of SiH<sub>4</sub> with a flow rate in the range from 0.3sccm to 2.5sccm; 2) Pump out; 3) The supply of C<sub>3</sub>H<sub>6</sub> (from 0.8sccm to 10sccm) and finally; 4) Pump out. This process provides a typical 3C-SiC growth rate of 0.8nm/cycle in our LPCVD reactor.

Fig. 2 shows an optical image of a typical 300mm Si wafer with a thin 3C-SiC layer deposited with the process described above. No defects are visible by naked eye and light interferences induced by the transparent 3C-SiC coating show a uniform color, indicating its high thickness uniformity. In this particular case, the average 3C-SiC thickness was 51nm with a standard deviation of 0.3nm over the whole wafer. Our results show a thickness non-uniformity of ~1% or less for 3C-SiC thicknesses up to several micrometers. This high precision thickness control and uniformity is needed for production of high quality optical devices. Figs. 3 show a cross-section image obtained by high-resolution transmission electron microscopy (HRTEM) of a 3C-SiC/Si(111) interface and its corresponding selected area electron diffraction (SAED) pattern. The HRTEM image shows a smooth interface with no etch pits, indicating the high quality of the hetero-epitaxial growth. The SAED pattern confirms the single-crystalline form of the grown 3C-SiC film. These results are also confirmed by XRD scan (not shown here). Surface morphology and roughness of the 3S-SiC films were also

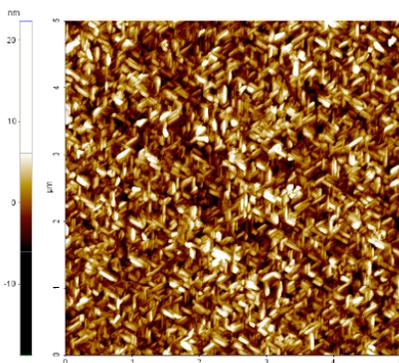


Figure 4 – AFM image for a 330nm-thick 3C-SiC film grown on Si(111) substrate. Scanned area is 5μm×5μm.

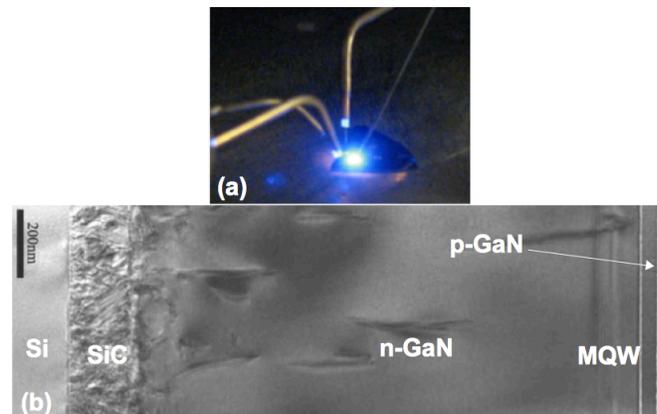
investigated by atomic force microscopy (AFM) and a representative image is shown in Fig. 4. Typical root mean square roughness of 3nm is found for films of few hundred nm thick. The roughness was found to slightly increase with increasing film thickness.

Those results show that low-temperature LPCVD combined with an ASE approach can provide high quality 3C-SiC thin films on Si with excellent thickness uniformity on very large wafer size. It is also worth noting that similar results can be obtained on both Si(100) and Si(111) substrates.

### 3 INTEGRATION OF GAN-LEDS ON SI USING SIC TEMPLATE

The low lattice-mismatch of SiC with GaN has enabled the commercial development of high-power GaN-LEDs on SiC substrate. As SiC has a much smaller lattice mismatch with GaN (~3%) than Si (~17%), use of SiC template to grow GaN-LEDs on Si wafer is a very attractive approach. The large size of the Si wafer and their relatively low price would reduce the retail price of the GaN-LEDs which is still hampering their acceptance in the general public. MOCVD growth of thick crack-free GaN layer has already been demonstrated on 3C-SiC template on Si [14], and more recently, we have successfully grown a GaN-LED structure on SiC-on-Si [15]. Fig. 5(a) shows an optical image of the blue electroluminescence from the LED structure and cross-sectional TEM image of the LED structure on SiC-on-Si is displayed on Fig. 5(b). While growth optimization is still an ongoing work, these results demonstrate the high potential of SiC-on-Si for low-cost production of efficient GaN-LEDs.

To demonstrate further the advantages of using 3C-SiC for GaN-LEDs on Si, we used 3C-SiC to fabricate a distributed Bragg reflector (DBR). Such SiC-based DBR mirror could be used as a high-reflectance growth template for GaN-LEDs on Si, and would be a cheaper alternative compared to the standard substrate transfer to a higher



Figures 5 – (a) Optical image of the EL of a GaN-LED grown on SiC-on-Si and (b) a cross-sectional TEM image of the same structure.

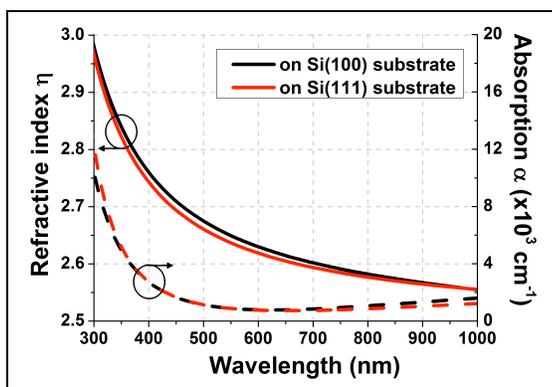


Figure 6 – Optical constants of ~1µm-thick 3C-SiC layer grown on Si(100) and Si(111) substrates respectively.

reflectance substrate [17]. The DBR template can act as a reflective mirror for the GaN-LED light emission, reducing the optical loss in the non-transparent Si substrate and therefore increasing the LED efficiency. In order to optimise the DBR design, optical properties of as-grown 3C-SiC layers on Si were first investigated by spectroscopic ellipsometry (J.A Woolman VUV-VASE GenII). Optical constants, extracted from the experimental data, are plotted in the Fig. 6 and show quasi-identical results on both Si(100) and Si(111) substrates. A refractive index of 2.7 can be deduced at 450nm, which is in good agreement with reported values for bulk 3C-SiC [18], showing de-facto the good quality of these 3C-SiC thin-films on Si. Low residual absorption is still visible above the indirect band-gap, most likely due to growth imperfections. Then single-crystal 3C-SiC/AlN/3C-SiC layers were hetero-epitaxied on a 100mm Si(111) wafer, forming a 1.5 pair DBR designed to provide high reflectance in the blue region. Fig. 7 shows a typical reflectance spectrum from this DBR with a maximum reflectance of 52.5% obtained at 444nm, and a minimum full width half maximum of 115nm. Higher reflectance can be obtained by increasing the number of pair.

#### 4 CONCLUSIONS

This paper presents a new deposition tool to achieve the hetero-epitaxy of single-crystal 3C-SiC on Si by using LPCVD growth at low-temperature with an alternative supply epitaxy approach. This new growth technique does not induce any extended defects, neither voids, into the Si substrate, and provides good quality 3C-SiC thin-films with very high thickness uniformity on up to 300mm Si wafers. Growth of a GaN-LED structure on Si was demonstrated by using the 3C-SiC thin-film as a growth template and a 3C-SiC based DBR on Si was also successfully fabricated which shown high reflectance in the blue spectrum. Single-crystal 3C-SiC thin-film on Si is also of great interest for MEMs application as well as to integrate enhanced photonic structure on Si.

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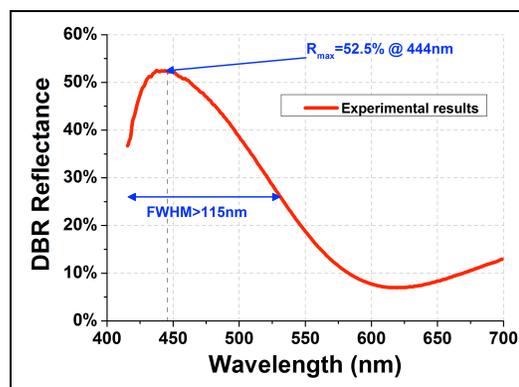


Figure 7 – Reflectance spectrum of a SiC-based DBR on a 100mm Si(111) substrate.

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