Wafer-scale Integration of In-situ Grown Horizontal Carbon Nanotube Membranes: a Platform to Study Electrical Properties

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ABSTRACT

This work deals with the wafer-scale fabrication of a basic building block for electronic devices. It consists in horizontal supported or suspended membranes made of a dense carbon nanotube (CNT) array connected between two metallic top electrodes. An integration yield of similar CNT membranes higher than 90 % is achieved on a 100 mm wafer thanks to a robust process flow based on in-situ CNT growth by a chemical vapor deposition (CVD) process. The wafer constitutes a platform to optimize the membrane electrical performances by tuning post-growth processes. A state of the art value of 3.6 $m\Omega.cm^{-1}$ is obtained for the membrane equivalent resistivity and a negligeable contact resistance is achieved for Pd/Au top electrodes. An insulating Diamond Like Carbon (DLC) layer appears as an innovative good material to encapsulate the CNTs.

Keywords: horizontal carbon nanotubes, wafer-scale integration, in-situ growth, electrical properties, encapsulation.

1 INTRODUCTION

Dense arrays of horizontal CNTs connected between two metallic electrodes, either supported on a silicon dioxide layer or suspended, constitute a basic building block to achieve CNT-based electronic devices such as sensors [1, 2], interconnect lines [3, 4] or micro-electromechanical systems [5]. Despite the recognized potential of CNTs, their adoption as alternative materials is postponed mainly due to integration issues at wafer-scale. A reliable integration scheme totally compatible with full wafer processing was previously proposed by our team to manufacture multi-criteria resistive and resonating gas sensors [1, 2]. It was based on in-situ CNT growth by catalytic CVD and used conventional silicon technologies of the microelectronic industry. Resistive sensors were thus fabricated via the successful integration of supported horizontal few-walled CNT membranes on 100 mm wafers [2].

Here, a buffered hydrofluoric (BHF) acid solution followed by critical point drying is assessed to suspend the membranes. Moreover, the elaboration of a huge number of similar CNT membranes by CVD at the wafer-scale constitutes a real asset to study how post-growth processes can affect the CNT electrical performances and to optimize the critical steps required for device fabrication. Different processes and materials were investigated for the top electrode elaboration and for the membrane encapsulation by an insulating material. The latter is of particular interest for interconnect applications [6] and 3D integration of CNT based devices. The impact of BHF treatment was also studied.

2 FABRICATION OF CNT-BASED DEVICES

The process flow previously developed by our team and presented in Fig. 1 was used to fabricate the electrical devices made of supported or suspended horizontal CNT membranes.

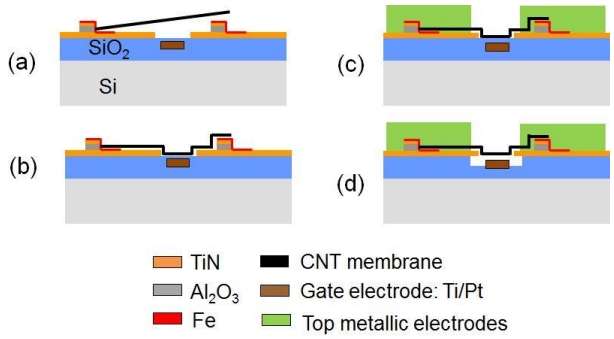

Figure 1: Process flow for fabrication of devices made of suspended or supported CNT membranes.

A line-shaped catalyst support was optimized to activate the growth of pre-inclined CNT membranes. It consisted of a TiN / Al_2O_3 / TiN stack, on which a 1 nm thick iron (Fe) catalyst layer was deposited by e-beam evaporation (45° tilt angle) and localized via a lift-off process combined with optical lithography. The CNT growth was performed at 580°C in a mixture of acetylene (3%), hydrogen (30%) and helium (67%) at a pressure of 0.4 mbar (Fig. 1a). The growth occurred selectively from Al_2O_3 surfaces only, due to Fe diffusion into the TiN layers. The highly thin Fe layer gave rise to nano-particles with a sufficiently high density to compel the CNTs to grow

parallel to each other and perpendicularly to the Al_2O_3 side-walls (Fig. 2a2). A very good integration yield at wafer-scale higher than 90 % was demonstrated. Transmission electron microscopy revealed a CNT average diameter of 4.6 nm with values ranging between 2.7 to 6.3 nm. The number of graphitic walls per CNT was between 1 and 5 walls with a vast majority of double-walled CNTs.

The horizontal supported membranes were obtained by flattening the pre-inclined membranes onto the substrate thanks to a wet treatment in isopropanol, without impairing the high integration yield (Fig. 1b, 2b1 and 2b2). Scanning electron microscopy (SEM) images are consistent with a density of few 10^{12} CNTs.cm^{-2}.

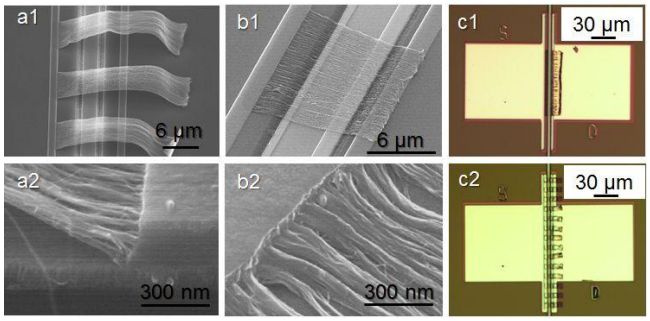

Figure 2: SEM images of devices (a1, a2) after CNT growth, (b1, b2) after CNT flattening; (c1, c2) optical microscopy images of devices made of supported membranes with Cr/Al top electrodes.

The fabrication of the top electrodes (Fig. 1c) was then performed on individual dies cleaved from the same wafer. The aim was to investigate different metallization processes and materials on similar membranes grown simultaneously in the same run. The top metallization was performed by combining optical lithography and a lift-off process previously developped by our team to realize side-bonded contacts on CNT lines [3]. A mild oxygen descum plasma was systematically carried out at 80W for 20s prior metal deposition in order to remove residues on the CNTs in the areas where the photo-resist was opened. Different metal stacks were investigated: Cr/Al and Pd/Au deposited at normal incidence by e-beam evaporation and Ti/Au deposited by sputtering. The first 20 nm thick layer ensures the electrical contact with the CNTs and promotes the adherence of the 200 nm thick top layer, which should withstand the post-processes investigated here. Different membrane designs were evaluated: devices made of a 84 µm wide single continuous membrane (fig. 2c1) and devices made of a dashed membrane (fig. 2c2). The second group consisted of several membranes in parallel: 7 membranes with widths of 12 µm or 14 membranes with widths of 6 µm, as defined on the lithography mask. All the devices should thus correspond to about the same number of CNTs in parallel. Different gap between the top electrodes were also designed (3 to 9 µm).

The thickness of the membranes anchored by the top electrodes was estimated to about 40 ± 10 nm by intermittent contact atomic force microscopy.

An annealing treatment previously developed [2] was carried out on one die at 400°C under H_2 for 10 min to improve the membrane electrical behavior.

Various insulating encapsulation materials were deposited on the whole surface of several dies with supported membranes to study their impact on CNT electrical performances. For Cr/Al electrode devices, two kinds of SiO_2 layers were investigated: a 22 nm thick coating deposited by CVD in O_3 atmosphere and a 25 nm thick coating deposited by plasma enhanced CVD (PECVD) in O_2 atmosphere. A 15 nm thick Al_2O_3 layer deposited by Atomic Layer Deposition (ALD) was also tried on similar devices. Finally, a DLC layer with an estimated thickness of 8 nm was deposited by a PECVD process on devices with Ti/Au electrodes.

Just after the top electrode fabrication, one die with Pd/Au electrodes underwent a wet treatment in BHF solution followed by critical point drying with CO_2. This step should lead to the release of the membrane through selective etching of the under-lying SiO_2 while preventing surface tension effect (Fig. 1d). This process was 100% efficient for CNT membrane widths ≤ 6 µm and suspended membranes up to 5 µm long were successfully demonstrated (Fig. 3). The process however still requires optimization for the other designs.

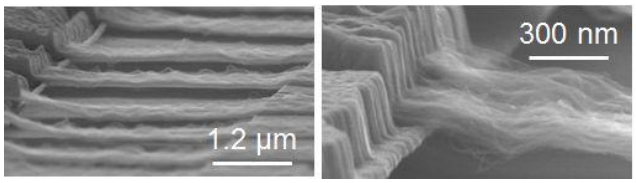

Figure 3: SEM images of devices made of suspended CNT membranes with Pd/Au top electrodes.

3 CNT MEMBRANE ELECTRICAL PERFORMANCES

Two point probe direct current electrical characterizations were performed. The current versus voltage (I-V) characteristic was plotted for each device by applying a ± 1V voltage sweep between the 2 top electrodes. The I-V curves generally showed a linear behavior representative of an ohmic contact, from which the overall device resistance was extracted (Fig. 4). The contribution of the electrical probes was measured and substracted to the overall resistance to obtain the CNT membrane resistance, $R_{membrane}$.. The electrode resistances were neglected.

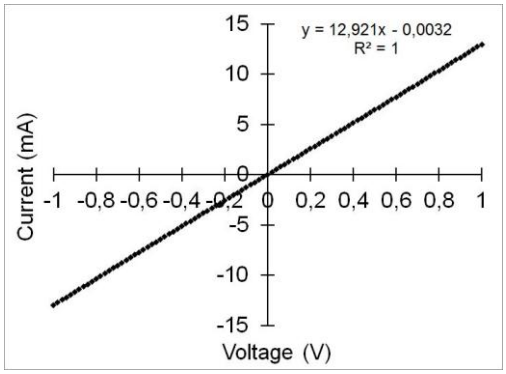

Figure 4: Typical I-V plot for a Pd/Au top contacted device corresponding to an overall resistance of 77Ω.

For each die corresponding to a given fabrication process, this resistance was plotted as a function of the length of CNTs bridging the electrodes (L). These values were measured manually by optical microscopy. The curves could be fitted with linear regressions (Fig. 5) consistent with the electrical behavior of N CNTs in parallel according to equation 1:

$$R_{membrane} = \frac{r}{N} = \frac{rc}{N} + \frac{rs}{N} \times L = Rc + Rs \times L \qquad (1)$$

where r is the resistance of individual CNTs, rc and Rc the respective contact resistances of individual CNTs and of the membrane, rs and Rs the respective scattering resistance of individual CNTs and of the membrane. The experimental uncertainty on Rs (which is representative of the CNT cristalline quality) was estimated at about ± 0.5 Ω.µm^{-1} and a high uncertainty level of about ± 5 Ω was estimated for the zero length intercept Rc. Finally, an equivalent resistivity (ρ_{eq}) of a 40 nm thick bulk membrane could be calculated from the Rs values, using average membrane widths measured on the devices. This value is thus over-estimated compared to the real resistivity of the CNT membrane since CNTs do not fill the whole membrane volume and top metallization certainly do not connect all the CNTs in the membrane [3].

Fig. 5 and table 1 display the results obtained on supported membranes for different processes of fabrication of the top electrodes. The same process corresponding to Cr/Al electrodes repeated on 3 dies (07, 08 and 10) led to comparable results, showing the good process reproducibility and also the good membrane homogeneity at the wafer scale. This can be explained by the huge number of CNTs in parallel in each membrane, resulting in similar overall electrical behavior. The best contacts were achieved with Cr or Pd. Suprinsingly, the scattering resistance depends on the nature of the top electrodes, even though the CNT membranes are basically identical. This feature demonstrates that a variable number of CNTs is electrically contacted depending on the metal deposition process used: Ti/Au contact deposited by sputtering instead of evaporation yields the best resistivity (3 mΩ.cm^{-1}). However, Pd/Au stack appeared as the best compromise since this process led simultaneously to a negligeable contact resistance and a low membrane resistivity of 3.6 mΩ.cm^{-1}, which is comparable to the state-of- the-art values [7]. Post-annealing treatments are generally used to improve the contact resistance [2]. Here, a good contact quality seems to be achieved thanks to the mild O_2 descum plasma performed before metal deposition. A further annealing step was not necessarily beneficial as the contact resistance notably increased. However, the resistivity was improved, probably due to a cleaning of the CNTs in the area located between the electrodes (removal of photo-resist residues).

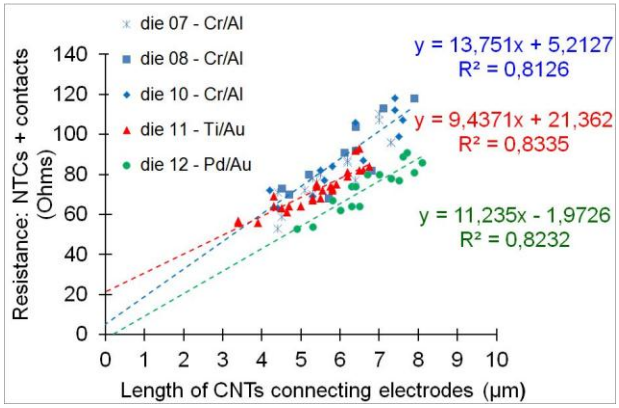

Figure 5: $R_{membrane}$=f(L) plots for devices on several dies corresponding to different top electrode metals.

Die	Electrodes	Rc (Ω)	Rs (Ω.µm^{-1})	ρ_{eq} (mΩ.cm^{-1})
07	Cr/Al	Negligible	14.1	4.4 – 4.6
07	Cr/Al + annealing	18	10.6	3.3 – 3.5
08	Cr/Al	4.1	14.0	4.4 – 4.6
10	Cr/Al	5.2	13.8	4.3 – 4.4
11	Ti/Au	21	9.44	3.0 – 3.1
12	Pd/Au	Negligible	11.2	3.6 – 3.7

Table 1: Scattering resistances (Rs), contact resistances (Rc) and equivalent resistivities (ρ_{eq}) of CNT membranes for dies with different top electrodes.

Table 2 and Fig. 6 and 7 show the results obtained after the different encapsulation processes. Except for SiO_2 deposited by CVD, the pristine electrical performances (Rs values) are generally degraded to some extent, whereas the contact resistances remained comparable. This behaviour can be correlated with a modification of the CNT structure in contact with an insulating material. The DLC layer appeared as an interesting encapsulation material since the resistivity degradation was limited (Fig. 6).

Die	Encapsulation	Rc (Ω)	Rs ($\Omega.\mu m^{-1}$)	ρ_{eq} ($m\Omega.cm^{-1}$)
07	PECVD SiO_2	8.3	26.7	8.3 – 8.8
08	ALD Al_2O_3	Not representative	21.5	6.8 – 7.1
10	CVD SiO_2	Negligible	10.6	3.3 – 3.4
11	PECVD DLC	20	13.4	4.3 – 4.4

Table 2: Scattering resistances (Rs), contact resistances (Rc) and equivalent resistivities (ρ_{eq}) of CNT membranes for dies with different encapsulation processes.

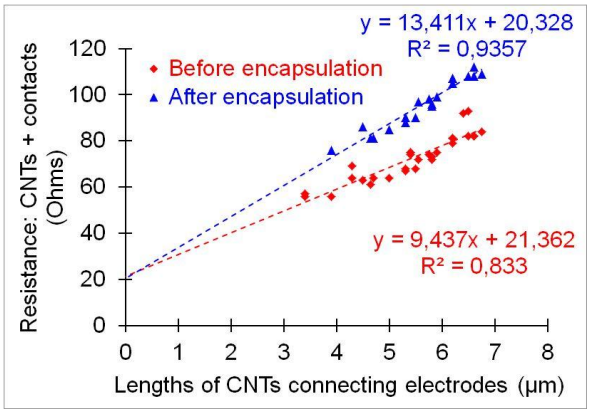

Figure 6: $R_{membrane}$=f(L) plots for devices with Ti/Au electrodes before and after encapsulation by DLC.

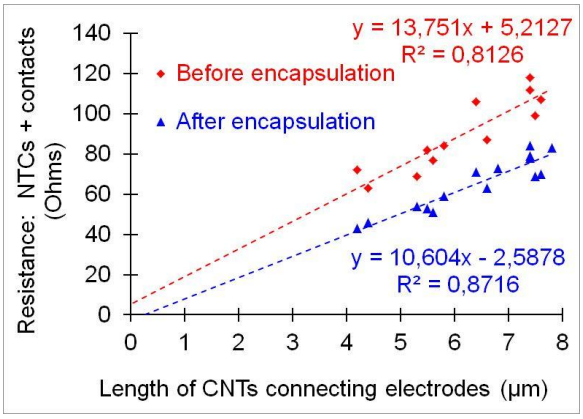

Figure 7: $R_{membrane}$=f(L) plots from devices with Cr/Al electrodes before and after encapsulation by CVD SiO_2.

A surprising result was obtained for CVD SiO_2: the scattering resistance notably decreased. This improvement could be explained by a cleaning of the CNT surface from organic contaminants brought by the photo-resist spread on CNTs during fabrication of the top electrodes. This could be activated thanks to the peculiar O_3 atmosphere used during the CVD process.

Finally, as illustrated on Fig. 8, the BHF treatment to suspend the membranes did not induce notable modifications of the electrical performances.

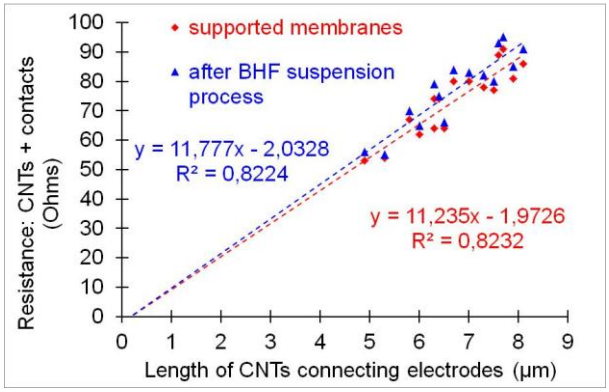

Figure 8: $R_{membrane}$=f(L) plots for devices on die 12 with Pd/Au electrodes before and after the BHF treatment.

4 CONCLUSIONS

A highly robust process flow previously developed by our team allowed the integration on 100 mm wafers of supported 40 nm thick horizontal membranes made of dense few-walled CNTs. The integration yield higher than 90% corresponds to the best result ever reported. The huge number of CNTs simultaneously in-situ grown by CVD led to a very good membrane homogeneity at wafer scale. The membrane suspension was demonstrated for specific device designs. The electrical performances of CNT membranes contacted by top electrodes appeared to be strongly dependent on post-growth processes. Pd/Au stack evaporated on top of the membranes led to negligeable contact resistances and an equivalent membrane resistivity of 3.6 $m\Omega.cm^{-1}$, i.e. comparable to state of the art values. DLC was shown to be an innovative insulating material to encapsulate the CNTs with a limited degradation of the electrical performances. Finally, post-growth wet processes can induce an organic contamination of the CNT surface: cleaning processes need to be optimized to recover the pristine CNT properties.

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