Charge Amplification of a Graphene-Integrated-CMOS (GIC) RF Detector

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ABSTRACT

We demonstrate an approach to characterize the charge amplification of mono-layered graphene as an integral part of a *Complementary Metal Oxide Semiconductor Device (CMOS)* under RF radiation. The understanding of the mechanisms of charge amplification involved in GIC devices is of fundamental and technological importance to the advancement of nanotechnology as the scientific community struggles to use graphene as an electronic device material. This proceeding underlines important findings in an effort to develop a state-of-the-art graphene integrated CMOS RF detector. We have verified that under 500 MHz RF radiation, charge carriers on a device integrated with graphene will effectively interact with an applied electric field and graphene electronic properties can be measured indirectly through capacitive coupling between surfaces.

Keywords: graphene, CMOS devices, RF detection

1 INTRODUCTION

Graphene is a single-atom thick layer of carbon atoms arranged in a honeycomb crystal lattice with a carbon-carbon bond length of 0.142 nm [1]. With a densely packed single planar sheet of sp^2-bonded carbon atoms, graphene provides a strong and robust material that is capable of providing a potential barrier to separate electronic devices from chemical excitation and harsh environments while remaining electrically conductive. Graphene is also unique in that it is a semi-metal with zero bandgap [1], [2]. The E-k relation illustrates that the conduction and valence bands meet at the K points of the Brillouin zone and result in the existence of fermions with zero effective mass and carrier mobilities reported to be greater than any other material (>100,000 cm^2/V s at room temperature) [3]. Graphene also possesses one of the highest thermal conductivities of any known material (~50 W/(cm·K)) [4] which makes it particularly attractive for electronic applications.

Impact ionization and Auger recombination have been theorized to dominate relaxation dynamics in graphene and can be exploited to obtain carrier multiplication [5]. Impact ionization is the process by which kinetic energies of energetic electrons can be passed to bound electrons and result in the generation of electron-hole pairs. Auger recombination is the process by which electron-hole pairs are created when electrons fill empty energy states and release their energy to neighbor electrons. In either case, a single absorbed photon can excite an electron-hole pair to start each process and under a high electric field can induce avalanche breakdown. Graphene's zero bandgap will aid in efficient e-e scattering due to energy and momentum conservation [5]. However, the lack of an existing bandgap has limited the development of graphene integrated devices due to the inability to correctly switch on and off an electronic device such as in steady state MOSFETs.

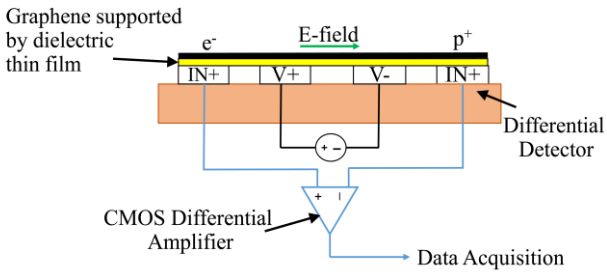

Figure 1: Device Visualization. Location of graphene and metals rails on GIC Differential Detector.

Our research aims to develop a better understanding of graphene's electrical properties and how to manipulate those properties to incorporate mono-layer graphene into low frequency detectors that do not require an off-state. Radio frequency devices are unique in the manner that devices can be operated in an on-state, and RF signals that are to be amplified are superimposed onto a dc gate to source voltage [6]. Our hope is that the combination of a high electron mobility and carrier multiplication will allow our device to detect low-energy RF radiation.

2 METHODOLGY

Graphene was isolated using a physical exfoliation process and mechanically transferred to a silicon-based *CMOS test integrated circuit* (CTIC). The *Graphene-Integrated-CMOS* (GIC) device consist of various differential amplifiers configured for low-powered operation and corresponding metal sense rails to detect small changes in an underlying applied electrical field as a direct result of the generation and recombination of electron-hole carriers when exposed to RF radiation. We hope to verify that under low energy RF radiation, charge carriers above a graphene surface will effectively interact with the applied electric field potential and can be monitored by small changes in potential energy detected by a CMOS differential amplifier. It is hoped that the response will be significant compared to a device without graphene integration.

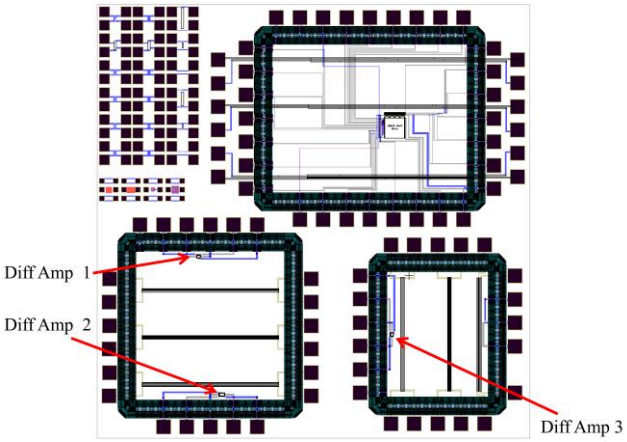

Figure 2: 5 mm x 5 mm CMOS Test Integrated Circuit with location of differential amplifiers 1, 2, and 3 along with corresponding metal rails.

3 FABRICATION OF A CMOS TEST IC

Figure 2 illustrates the transistor layout of the 5mm x 5mm CMOS test integrated circuit (IC). The IC was designed in Tanner Tools Layout editor and fabricated using a MOSIS TSMC (Metal Oxide Silicon Implementation Service Taiwan Semiconductor Manufacturing Company) 0.25 micron process.

3.1 ULP Differential Amplifiers

An Ultra-Low Power (ULP) Simulation Program with Integrated Circuit Emphasis (SPICE) model was used and provided by the Space and Naval Warfare Systems Command (SPAWAR) to implement into the design architecture. The test IC was proportioned into four quadrants, however, the top two quadrants are ignored as these quadrants are not applicable for this proceeding. The bottom two quadrants contain differential amplifiers (DA1, DA2, and DA3) for graphene measurements. In addition, each quadrant is enclosed in an electrostatic discharge padframe to protect the device components from electromagnetic interference (EMI). All three differential amplifiers were specifically designed to minimize power consumption and maintain a reasonable gain of 20 dB with a low supply. These goals were set to fully explore the capabilities of the ULP Model. The measurement area was kept small to reduce parasitics and produce a high signal-to-noise ratio. Furthermore, the differential pairs within each differential amplifier were matched utilizing an interdigitation technique [7] that allowed for an improved CMRR and accuracy of on-chip experiments that require accurate detection of small signal changes (in mV range).
Within each bottom quadrant are located three sets of metal rails in which graphene is overlaid. The outer two rails are coupled to the input stage of the differential amplifier under test and are responsible for voltage detection as charge carriers accumulate over the graphene surface as a direct result to an applied electric field potential across the inner rails. The spacing between rails is varied among each set, however, only the results of the middle set are reported in this proceeding. The longest rail dimension of the middle set measures 1.58 millimeters, width of 10 microns, and a spacing of 2 microns.

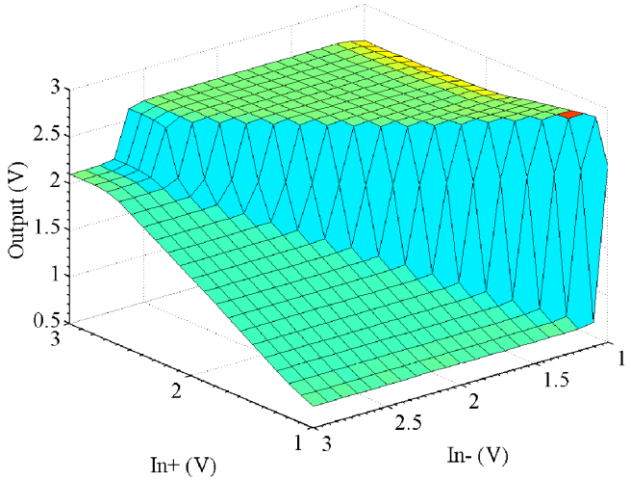

Figure 3: Output voltage characteristics of a DC sweep from 1-3V of DA1. (In blue) Output voltage range in which to operate the device during graphene measurements.

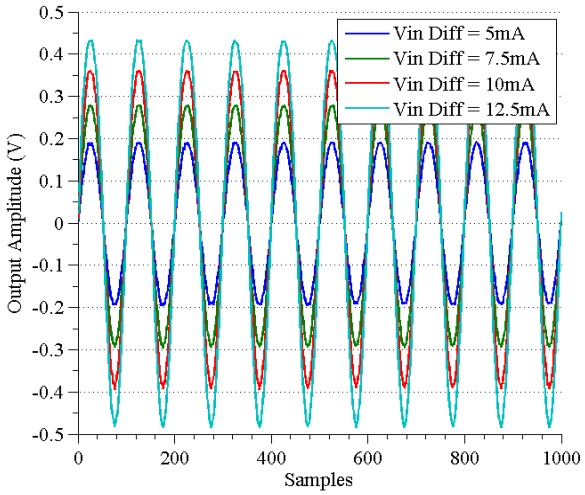

Figure 4: Output voltage characteristics of an AC sweep on DA1.

Parameter	Mean	Std	Unit
A_d	18.8 19.6 18.2	0.6 0.4 0.7	V/V
A_{cm},V_{off}=1.4, 1.7,1.7	1.1 1.0 0.9	0.1 0.2 .01	V/V

Table 1: Specification Summary of Differential Amplifier Operation.

3.2 CMOS Test IC Functionality

A DC sweep with an input range of 1-3V (V_{dd}=3V) was applied to the input terminals of each differential amplifier to determine the input offset voltage, output offset voltage, and dynamic range. Figure 3 illustrates the acceptable output range on DA1. It was noted to achieve correct operation, a 10 Kohm resistor was placed in series with the supply for current limiting between 20-33 micro amps. With an acceptable input offset voltage in mind, an AC signal was passed to the positive and negative input terminals to compute the nominal output range and compute a gain factor. A maximum gain of 20 dB, Table 1, was determined for small input voltages, Figure 4.

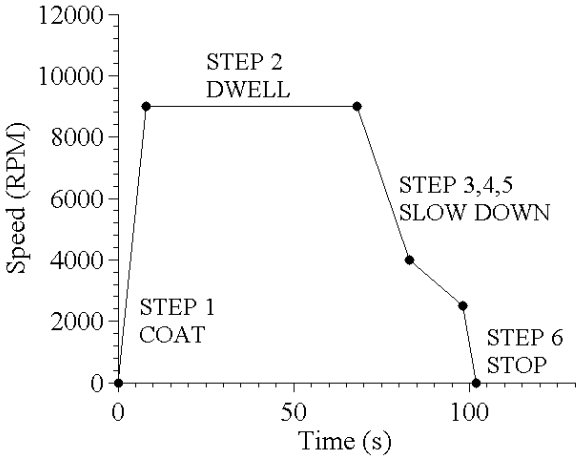

Figure 5: Spin coat recipe, G3 Spin Coat Series, Model G3P-8 to deposit 10 micron thick PDMS membrane on graphene grown on copper.

4 DIRECT EXFOLIATION OF GRAPHENE/PDMS STRUCTURE

Mono-layered graphene was transferred on-chip utilizing polydimethylsiloxane (PDMS) and a modified physical exfoliation process that minimizes damage to the graphene surface. Typical graphene transfer processes etch any metal catalyst beforehand and move graphene via thermal transfer tapes. However, these methods are not repeatable and have the potential to damage a graphene structure by applying unnecessary strain on the graphene surface, therefore, destroying graphene's desirable electronic properties. Our method utilizes the strength of the metal catalyst and robustness of the PDMS stamp to transfer and etch the metal catalyst on-chip and reduce the possibility of damage to the graphene structure.

To prepare the graphene structure for transfer, a solution of 10:1 PDMS base to curing agent is prepared at room temperature and mixed thoroughly for 5 minutes. A 10 micron thick PDMS membrane is deposited on a sample of

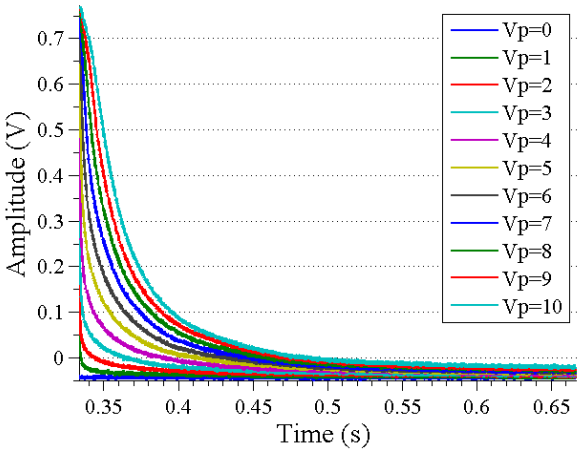

Figure 6: GIC differential response to an applied electric field potential by underlying electric field rails from 0-10V.

graphene grown on copper via chemical vapor deposition using the spin coat recipe in Figure 5. The PDMS/graphene/Cu (PGC) sample is then cured in a heat oven at 60 degrees Celsius for 45 minutes and cut to size by mechanical methods. Light pressure is applied via a 3-D printed micromanipulator stage integrated with a small strip of thermal transfer tape to grab and transfer the graphene structure to the device target area with the copper side facing up. The thermal transfer tape is released under 100 degrees Celsius and the copper film is etched in a solution of 20:1 deionized water (DI) water and Ammonium Persulfate. When the copper film is no longer visible, the device is rinsed with DI water and dried in an oven to remove any remaining water particles.

5 RESULTS AND DISCUSSION

For experimental comparison both a non-graphene intergrated-CMOS (NGIC) and a graphene-integrated-CMOS device (GIC) were placed in an ideal faraday environment and tested under the same conditions. An electric field was supplied via the two inner rails by a balanced 0-10V potential that was centered on an input voltage offset of 1.7V. Potential changes caused by the interaction with electron-hole pairs above the graphene surface was measured through capacitive coupling with the two outer metal rails that are tied to the input gates of DA1.

5.1 Charge Amplification of a grapehene

To get an understanding of how charge carriers interact with an underlying electric field and provide a reference for RF experiments, Figure 6, illustrates a 0-10V electric field potential varied on and input voltage offset of 1.7V. It is clearly noted that when the electric field potential is switched on and then off, the differential response resembles that of a typical resistor-capacitor network, which is expected due the

dielectric separation of 10 microns between metal surfaces. More importantly, it is determined that the induced electric field does contribute to a separation of charge carriers above the graphene surface as Figure 6 illustrates a detected potential difference across the positive and negative input terminals of the CMOS differential amplifier. The voltage response as the electric field potential is increased may be indicative of an increase in charge density due to charge carrier multiplication generated from the methods described in the introduction section and can be correlated to a simple relationship amongst charge and voltage for a simple capacitive network.

5.2 Charge Amplification of graphene under 500 MHz RF radiation

An omnidirectional RF propagation pattern of output power 10dB was exposed to both the GIC and NGIC device via a fixed monopole antenna and associated ground plane. Figure 7 illustrates a comparison of both devices to a fixed electric field potential of 10V under 500 MHz RF radiation. A frequency of 500 MHz was chosen only due the limited size of the testing area and test equipment. According to Figure 7, the sensitivity of the GIC device is ~40x greater than that of the NGIC device. It is believed that energy absorbed by RF photons generate an excess of electron-hole pairs on the graphene surface that can contribute to additional charge amplification by means of impact ionization and auger processes. The increase in charge density can further be correlated to an increase in voltage response, as illustrated in Figure 7.

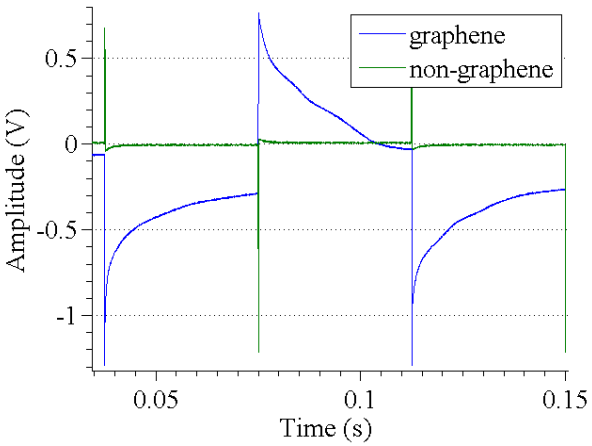

Figure 7: Differential response comparison of graphene and non-graphene integrated devices with an applied electric potential of 10V and 500 MHz RF radiation exposure.

Some noticeable differences between the output responses of the RF exposed GIC device and result from Figure 6 without exposure are the decay characteristics in Figure 7, illustrate a decay that is not smooth. For example, Figure 7 illustrates a decay curve with significant "bumps." The origin of these "bumps" is unknown at this time, but could be indicative of graphene defects or further interaction with RF radiation. It may be that as charge carriers recombine auger type processes dominate over impact ionization and result in a slight increase in voltage response. The origins of this phenomena is still an area of interest in which further implementations of our device will need to be explored.

6 CONCLUSION

The operation and implementation of 0.25 micron MOSIS TMSC CMOS architecture with monolayer graphene was demonstrated. RF Platforms in which size is limited, will greatly benefit from the improved sensitivity and compact size of the proposed GIC device. Results illustrate that charge carriers on a device integrated with graphene will effectively interact with an externally applied RF radiation pattern and can be carefully manipulated by an underlying electric field potential to indirectly measure potential changes through capacitive coupling between graphene and metal surfaces. Using CMOS architecture will allow for low power operation, amplification of graphene measurements, and easy integration with CMOS technology. Future implementations of our device will fully explore the capabilities of the proposed GIC device under varying RF power and frequencies. Utilizing such methods will push the potential of GIC devices to everyday use.

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