GIDL Current and Pass-Gate Body Potential Modeling in 22nm HKMG PD-SOI CMOS

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ABSTRACT

In a floating PD (partially depleted) SOI (silicon-on-insulator) transistor, the internal DC body potential is determined by the various body current components, mainly including diode current, gate-to-body oxide tunneling current (Igb), impact ionization current (II) and gate-induced drain leakage (GIDL) current. In logic circuits, the transistor is usually operated at off condition, linear condition or pass-gate condition. In this paper, we develop a new parameter extraction methodology for GIDL current to accurately model the pass-gate body potential in high K metal gate (HKMG) PD-SOI transistors. We also present the stability simulation result for 6-transistor (6T) static random-access memory (SRAM) cell to represent the +/- 50 mV pass-gate body potential uncertainty in the 22nm HKMG PD-SOI.

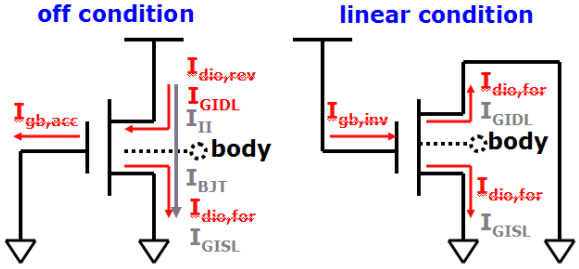
Keywords: gate-induced drain leakage current, pass gate, high K metal gate, silicon-on-insulator

1 INTRODUCTION

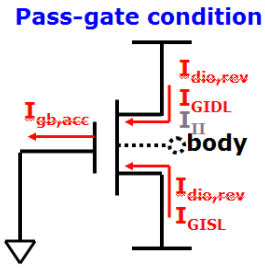
CMOS process technology scaling down to the 22nm technology node and beyond prompts remarkable process-induced variations in transistor performance [1]. SRAM is a critical component in system-on-chip (SOC) circuits. The SRAM cell usually consists of the minimum sized transistors and introduces big challenges during achieving higher density, lower power assumption and improved yield [2]. In PD-SOI transistor, the internal body potential during read and write operation directly influence SRAM stability margins. Modeling of body potential variation impact on SRAM write and read stability margins is very essential to accurately predict the circuit performance and yield.

In logic application, the transistor is usually operated at off condition, linear condition or pass-gate condition, as shown in Figure 1. At off condition, the body potential is determined by the balance between accumulation Igb current, forward diode current, reverse diode and GIDL current. At linear condition, the body potential is determined by the balance between inversion Igb current and forward diode current. At pass gate condition, the body potential is determined by the balance between accumulation Igb current, reverse diode current and GIDL (GISL) current.

In this paper, we analyze the DC body potential as function of both gate and drain voltages for 22nm HKMG PD-SOI technology. We further investigate how the different body current components affect the DC body potential at different biasing regions, especially in off condition, linear condition and pass-gate condition. It was found, with regard to NMOS, GIDL current has dominant impact on floating body potential at very negative V_{gs} and very high V_{ds}. We propose a new GIDL parameter extraction methodology and implement it into 22nm HKMG PD-SOI 6T SRAM stability margin simulation.



(a) off condition and linear condition



(b) pass-gate condition

Figure 1: Key current components to determine the DC body potential in logic application

2 DATA COLLECTION

Conventionally, the GIDL current parameters are extracted from Id-Vg characteristics at high V_{ds} and negative V_{gs} (for NFET). However, from 45nm PD-SOI technology and beyond, high gate leakage dominates drain current in accumulation region and makes it difficult to decouple the GIDL current and gate leakage contributions [3]. In this work, a different measurement setup is used to evaluate GIDL current effects and extract its model parameters.

Figure 2 illustrates the H-type body-contact FET layout used in the measurement. The nominal Vdd is 0.9V. In

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Figure 3, the gate terminal is swept from –1.3V to 1.3V at different drain voltages fixed at 0.05V, 0.3V, 0.6V and 0.9V. The source terminal is grounded. The body terminal voltage is sensed. During the measurement, long integration time is used to ensure reliable data. With this test setup, DC body potential is measured as a function of both gate voltage V_{gs} and drain voltage V_{ds}.

As shown in Figure 4, the measured 22nm HKMG PD-SOI moderate VT NFET raw data show a considerable distribution across the wafer. We used SAS program to remove the outliers and generate the median data for GIDL parameter extraction.

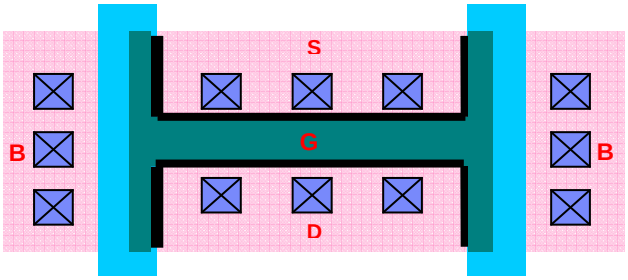

Figure 2: H-type body-contact device layout

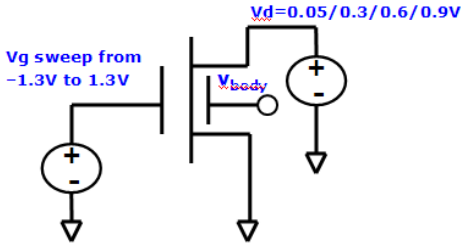

Figure 3: Testing setup for PD-SOI DC body potential

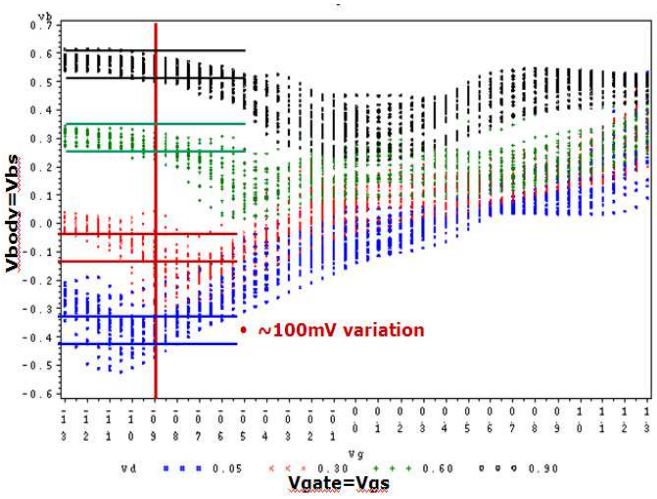

Figure 4: Body potential distribution (raw data) for 22nm HKMG PD-SOI moderate VT NFET

3 GIDL CURRENT MODEL PARAMETER EXTRACTION

The dependence of GIDL current as function of drain-source voltage V_{ds}, effective gate-source voltage V_{gse} and drain-body bias V_{db} is given as [4]:

$$I_{GIDL} = AGIDL \cdot W_{diod} \cdot N_f \cdot \frac{V_{ds} - V_{gse} - EGIDL + V_{fbsd}}{epsratio \cdot T_{oxe}} \cdot \exp\left(- \frac{epsratio \cdot T_{oxe} \cdot BGIDL}{V_{ds} - V_{gse} - EGIDL + V_{fdsd}} \right) \cdot \frac{V_{db}^3}{CGIDL + V_{db}^3} \quad (1)$$

where AGIDL, BGIDL, CGIDL and EGIDL are model parameters. W_{diod} is the effective body-drain width, N_f is finger number, $epsratio$ is dielectric constant ratio between silicon and oxide, T_{oxe} is effective oxide thickness. The flat-band voltage is defined as $V_{fbsd} = \frac{k_B T}{q} \ln\left(\frac{N_{gate}}{10^{20}} \right)$, where N_{gate} is poly gate doping concentration, k_B is Boltzmann constant, T is Kelvin temperature, constant q is electrical charge of an electron.

From eqn. (1), GIDL current can have large impact on body potential at very negative V_{gs} and very high V_{ds} (for NFET). In this work, we evaluate different body current components contribution on body potential at different V_{gs} and V_{ds}. A certain body potential range is utilized to extract GIDL parameters.

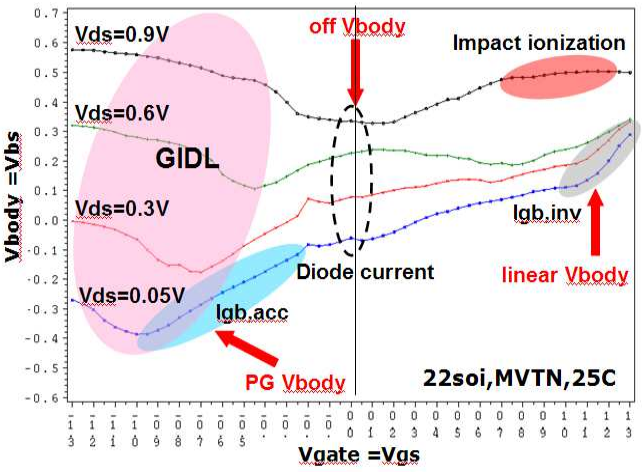

Figure 5: Body potential (median data) as a function of gate and drain biases for 22nm HKMG PD-SOI moderate VT NFET

Although the DC body potential is determined by the various body current components interactively, each body current is a different function of V_{gs} and V_{ds}. Figure 5 is the measured median DC body potential of 22nm HKMG PD-SOI moderate VT NFET as function of gate voltage V_{gs} and drain voltage V_{ds}. The impacts from GIDL current, diode current, Igb current and impact ionization current have been highlighted intuitively. The correlation between body current components and body potential varies with technologies.

In general, we can divide Figure 5 into six operating regions. (1) At off condition (V_{gs} =0V, V_{ds} =0.9V), the DC body potential is week function of V_{gs} and is mainly determined by diode current. (2) At V_{gs} =0V and V_{ds} =0V, both diode current and Igb current play roles. (3) At linear condition (V_{gs} =0.9V, V_{ds} =0.05V), the body potential rolls up by the inversion Igb current. (4) At V_{gs} =0.9V and V_{ds} =0.9V, the body potential is strongly impacted by impact ionization current and self-heating effect. (5) At pass-gate condition (V_{gs} =-0.9V, V_{ds} =0V), the body potential is mainly determined by accumulation Igb current and GIDL current. (6) At V_{gs} =-0.9V and V_{ds} =0.9V, the body potential rolls up by the large GIDL current.

In logic application, although the device is usually not biased at the above mentioned region (6), the strong sensitivity of body potential to GIDL current indicates an effective approach to extract GIDL parameters. We hence propose to use pass-gate body potential data (V_{gs} <0V) to extract the GIDL current parameters, as illustrated in Figure 6. Diode current and Igb current parameters have been extracted respectively prior to GIDL current parameter extraction. Genetic Algorithm [5] is used during parameter extraction. Figure 7 shows the body potential as-fit model result for 22nm HKMG PD-SOI moderate VT NFET.

4 6T SRAM CELL STABILITY SIMULATION RESULT

Figure 8 shows the commonly used 6-transistor SRAM cell architecture. It consists of two cross-coupled inverters (two pull-up PMOS transistors and two pull-down NMOS transistors) and two pass-gate (PG) NMOS transistors to control the access during read and write operations. As long as the word-line (WL) is low, the PG transistors are turned off and the SRAM retains the stored value. (1) **Read operation**: when the WL is high, these two PG transistors are turned on, and the two inverters drive the stored data into bit-lines (BL and BLC). (2) **Write operation**: when the WL is high, these two PG transistors are turned on, and the stored value in the two inverters are literally overwritten by the pre-charged BL and BLC value.

One important aspect to the SRAM design is the process variation that may be tolerated and have the cell still be writeable (Write Margin, WRM), and the process variation that may be tolerated and have the cell remain stable when it is read (Access Disturb Margin, ADM). In PD-SOI CMOS technology, the body potential variation has direct impact on SRAM read and write noise margin. Therefore the uncertainty in the body potential model drives significant uncertainties in the SRAM WRM and ADM simulation. The two pass-gate NMOS are key cells, hence particularly for SRAM, the GIDL current and pass-gate body potential modeling have significant impact on the performance of SRAM circuits.

In this experiment, we simulate the 6TSRAM WRM and ADM as functions of process-induced variability of pass-gate body potential. We define the BSIMSOI model GIDL parameter ***agidl*** and accumulation Igb parameter ***alphagb2*** variation range to represent the +/- 50 mV pass-gate body potential uncertainty in the 22nm HKMG PD-SOI, as shown in Figure 4. Figure 9 and Figure 10 are the simulated ADM and WRM uncertainty for a 22nm SRAM 6T cell for various values of ***agidl*** and ***alphagb2*** parameters. A +/- 50 mV pass-gate body potential uncertainty yields ~0.37 sigma ADM uncertainties and ~0.68 sigma WRM uncertainties at high Vdd (=1.0V), where GIDL current plays an important role on SRAM stability. From Figure 4, in pass-gate condition, GIDL current's impact is negligible when Vdd is below 0.9V. This yields WRM uncertainties insensitive to ***agidl*** parameter at lower Vdd (=0.8V), as shown in Figure 11. There is similar observation for ADM uncertainty at Vdd=0.8V. While still a significant uncertainty, this advance in model accuracy is needed to facilitate meaningful SRAM margin simulations at this technology node.

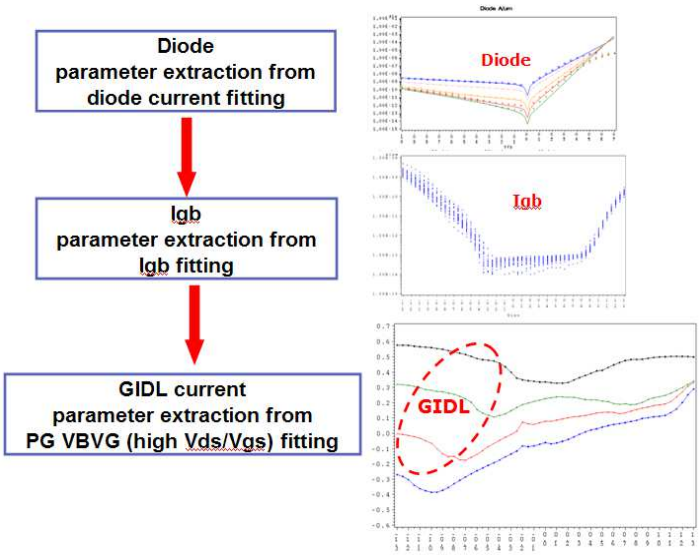

Figure 6: Proposed GIDL parameter extraction methodology

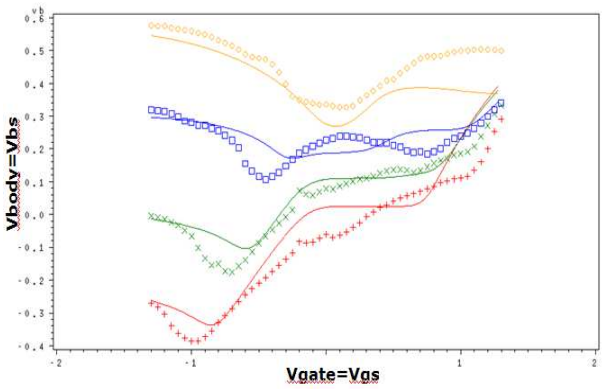

Figure 7: Body potential (median data) and as-fit model for 22nm HKMG PD-SOI moderate VT NFET

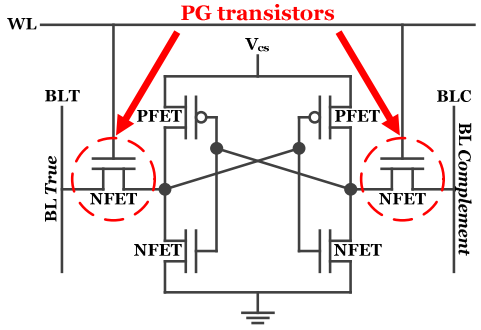

Figure 8: 6-transistor (6T) SRAM cell diagram

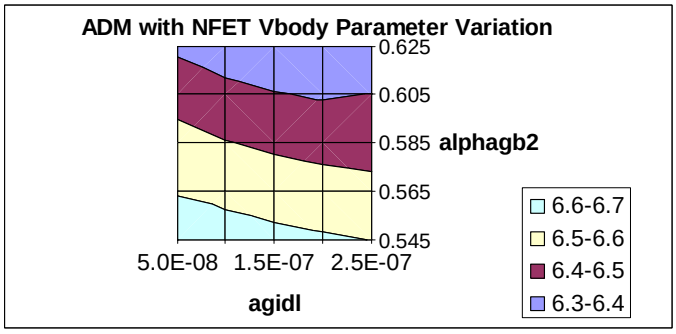

Figure 9: 6T SRAM cell ADM simulation result at Vdd=1.0V, 105C, TT

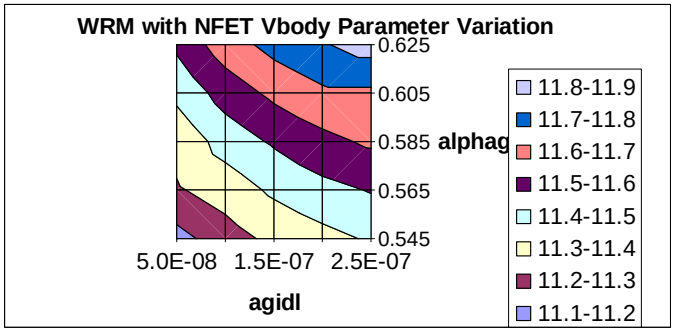

Figure 10: 6T SRAM cell WRM simulation result at Vdd=1.0V, -10C, TT

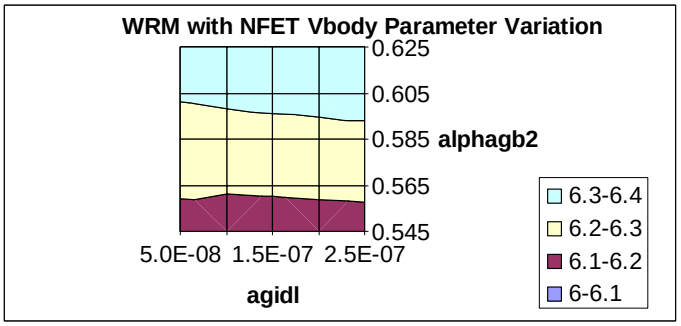

Figure 11: 6T SRAM cell WRM simulation result at Vdd=0.8V, -10C, TT

5 CONCLUSION

We have investigated 22nm HKMG PD-SOI DC body potential at off, linear and pass-gate conditions. We have presented a new GIDL current parameter extraction methodology from a certain DC body potential biasing range, where its strong sensitivity to GIDL current exists. Accurate body current and body potential models have been developed for 22nm HKMG PD-SOI 6-transistor SRAM cell simulation and design. We also present the stability simulation result for this 6T SRAM cell to represent the +/- 50 mV pass-gate body potential uncertainty in the 22nm HKMG PD-SOI.

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