Numerical Study on Gate-All-Around Tunneling FET with SiO2 Core and Si Shell Structure

Xiangyu Zhang*, Aixi Zhang**, Jinhe Mei*, Lining Zhang**, Hongyu He*, Jin He**, and Mansun Chan*

*Peking University Shenzhen SOC Key Laboratory, PKU-HKUST Shenzhen-Hong Kong Institution, Shenzhen, China

** School of Electronics Engineering and Computer Sciences, Peking University, Beijing 1008781, China

ABSTRACT

This work presents a gate-all-around tunneling FET based on SiO_2 core and Si shell structure (GAA-SOI-TFET) and demonstrates its performance characteristics via the numerical simulation method. The 3-D T-CAD numerical simulations demonstrate that this new device has steep subthreshold swing (<60mV/dec), suppressed drain-induced barrier lowering, and enhanced I_{on}/I_{off} ratio up to 10^9 orders of magnitude. It is worth noting that I_{on} begins to increase when SiO_2 core radius exceeds a specified value (~4nm) while influence of gate oxide thickness on the device performance being an important factor.

Keywords: gate-all-around (GAA), nanowire, core-shell, tunnling field-effect transistor (TFET), band-to-band tunneling, quantum confinement effect

1 INTRODUCTION

Following ITRS demonstrated international semiconductor technology development trend, the next generation integrated circuit technology will rapidly comes into 22 nm node. Under such a high integration density and small size background, reducing circuit operation power consumption has become a major concern. Tunneling field effect transistors (TFETs) have been a competitive candidate in future integrated circuits due to their potential use in low power logic circuit, analog circuits [2] and a subthreshold-slope below the limit of 60mV/decade. However, TFETs drive current is smaller than conventional MOSFETs. Gate-all-around (GAA) TFETs [3-6] with best electrostatic control have been proposed. However, even in this scheme, the need of the channel radius decrease to relieve short channel effect (SCE) is still aggressive.

In this paper, a novel GAA TFET with SiO_2 core-Si shell (GAA-SOI-TFET) with the structure as shown in Figure1 is proposed to further improve TFETs performance. The numerical simulation work demonstrates the new device provides the better channel electrostatic control and relaxing requirement of shrinking of channel thickness. Through the introduction of SiO_2 core, channel region is similar to the silicon on the isolation substrate (SOI), thus, the device shows the advantages of both SOI and ultra-thin-body when SiO_2 core radius exceeds about 4nm. Using 3D-CAD tool, a series of numerical simulation experiments demonstrate that it is indeed possible to achieve less than 60mV/dec subthreshold swing, high I_{on}/I_{off} ratio, increased I_{on} and suppressed DIBL in this new GAA-SOI-TFET.

2 DEVICE STRUCTURE AND SIMULATION

A 3-D schematic view, a cross section along the channel and a cross section vertical to the channel of the GAA-SOI-TFETs are shown in Figure1.(a)~(c). A gate-all-around TFET (GAA-TFET) with the same parameters is used as a reference for comparison in Figure1. (d)~(f). Her only N type devices are discussed. There is a tunnel junction at the source side of the channel.

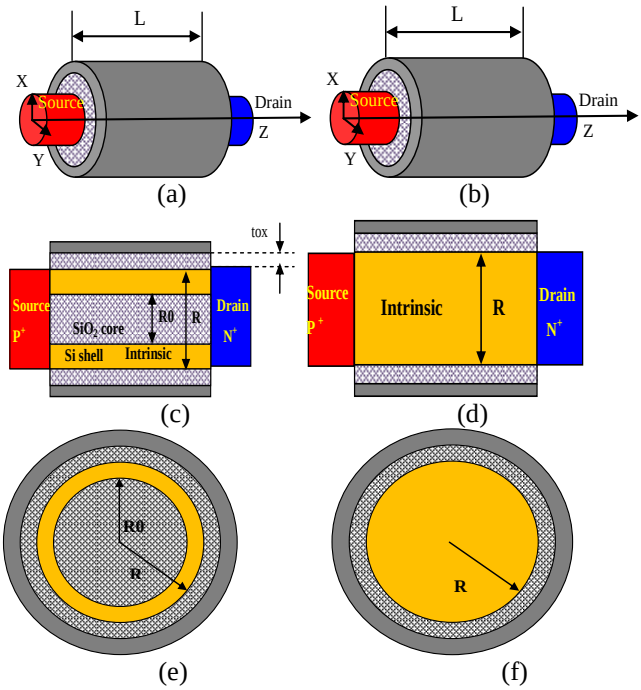

Figure1: A three-dimensional schematic view (a), cross section along the *z*-axis (b) and cross section perpendicular to the *z*-axis (c) of the GAA-SOI-TFET. (d), (e) and (f) are the corresponding picture of GAA-TFET.

The detailed parameters of both GAA-SOI-TFETs and GAA-TFETs used in the simulation are shown in Table I. The SiO_2 core radius (R0), channel doping concentration (Nc), gate oxide thickness (t_{ox}), and gate length (L) can be varied in the simulations. The GAA-SOI-TFET with R0=0

nm is named as the GAA-TFET, which is consistent with the common GAA device concept. The shell region is the conductive channel with a constant radius (R=10nm).

In the simulation, the non-local tunneling model is applied at the source/channel and drain/channel junction. In order to consider the quantum conferment effect, the modified local-density approximation (MLDA) model is used for electrons and the effects of doping concentration in the mobility mode are included. The Shockley-Read-Hall (SRH) generation and recombination model are also included. For simplicity, gate leakage model are neglected.

	GAA-SOI-TFET	GAA-TFET
Source doping (cm-3)	$10^{20}(P+^{+})$	$10^{20}(P+)$
Channel doping(Nc)(cm-3)	Intrinsic	Intrinsic
Drain doping (cm-3)	$10^{20}(N^{+})$	$10^{20}(N^{+})$
Gate oxide thickness (tox)(nm)	2	2
SiO2 core radius(R0)(nm)	0-8	0
Silicon shell radius(R)(nm）	10	10
Length of Sou/Dra (Lsd) (nm)	25	25
Length of Gate(L) (nm)	40	40

Table 1: parameters of GAA-SOI-TFET and GAA-TFET

3 RESULTS AND DISCUSSION

The characteristics of the GAA-SOI-TFET are investigated and compared with a compatible GAA-TFET. The influences of the key parameters are analyzed in this section.

3.1 Performance Characteristics of GAA-SOI-TFET

Figure2 (a) shows the transfer characteristic comparison between the representative GAA-SOI-TFET and the GAA-TFET. For low V_{gs}, the channel is in the weak inversion region. The tunneling probability is low and the reverse biased p-i-n diode characteristics play a major role. Thus the band-to-band tunneling current is low and current is nearly a constant. As V_{gs} increases, channel gradually comes into the strong inversion region, the tunneling probability increases and current rises [7].

As Si shell radius is very small, the entire channel is in the inversion region for the applied a positive gate bias and all of the carriers in channel participate in conduction. As it is expected that SiO_2 core reduces the total number of carriers in the channel that current in a R0=2nm device is smaller than a R0=0nm device as shown in Figure2a [12].

However, the numerical simulation results show that when R0 increases up to exceed 4nm, the strong inversion current begins to increase with R0 increases. A new study from the University of Texas seems to demonstrate similar result [8-9]. In that group work, a Si nanowire field effect transistors (FETs) with tiny cross sectional size (diameter (D) =3-5nm) is manufactured. As shown in the Figure2 (a), the channel current with R0=8nm is significant bigger than the GAA-TFET when V_{gs}>0.2V. I_{on} is improved by about two orders of magnitude. That means the smaller channel cross-sectional area corresponds to a larger current. In fact, it's the increased mobility that leads to the current ramps [8]. In this regard, the enhancement of mobility is attributed to the smaller scattering and uniform energy distribution of electron. Unlike in conventional GAA-TFET with larger conductive channel, appreciable accumulation of carriers in our devices is not probable, particularly in devices with R0=8nm. In Ref [8], it has been proven that there is a severe shortage of carriers in the channel region. Therefore, electrons in our GAA-SOI-TFET likely flow through fully depleted nanowires. So the electrons flow through the channel receiving smaller scattering. In addition to this, the 1D nanowire quantum confinement will also improve the mobility [9]. As illustrated in Figure1, the channel of GAA-SOI-TFET is confined in both x and y directions, so that motion normal to z is restricted physically and the electrons are free to move only in the z direction, producing a series of quantized energy levels; each energy level forms a subband. Each GAA-SOI-TFET with R0=8nm essentially forms a 1D system of electrons, since the equivalent diameter of the devices is close to the wavelength of an electron (10nm) [9]. The energy band of Si becomes discrete and a more uniform energy distribution appears. Mobility enhancement effect becomes significantly under uniform energy distribution.

Figure2 (b) shows the output characteristic of the GAA-SOI-TFET with R0=8nm and the GAA-TFET. When V_{ds} is low, current is a function of both V_{ds} and V_{gs}. As V_{ds} increases, the current reaches saturation as the common field effect transistors [10].

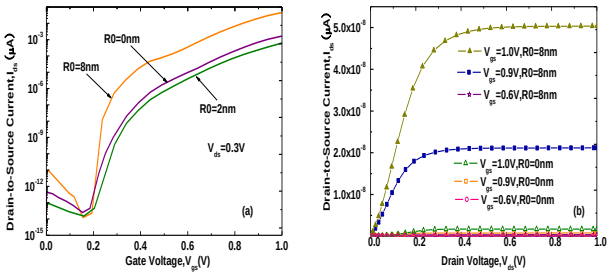

Figure2: Transfer characteristic (a) and output characteristic (b) comparison between GAA-SOI-TFET and GAA-TFET.

3.2 Effects of R0 and Nc

Figure3 (a) shows the I_{on} with increased R0 when V_{ds}=0.3 and V_{gs}=1V. The undoped channel (Nc = 0) has been analyzed at first. When R0<5nm, the core shielding effects is dominant, and I_{on} of GAA-SOI-TFET is smaller than GAA-TFET [12]. When 5nm<R0<8nm, quantum confinement effects plays a major role and I_{on} is increasing [8]. When R0=9nm, the shell region is so narrow that current begin to decrease. In Ref [8], it has been proven that there is indeed a peak mobility when tsi=3nm. Figure3 (a) also shows the impact of channel doping concentration on the I_{on}. Only when dopant concentration is large enough, the I_{on} can be influenced by Nc. When R0<7nm, the dopant can provide more electrons and promote current growth.

When R0>7nm, the number of additional dopant is small relatively and the dopant will reduce mobility, resulting in current decrease [8]. Since GAA-SOI-TFETs and GAA-TFETs commonly use lightly doped or intrinsic channels, their dependence on variations of channel doping can be neglected.

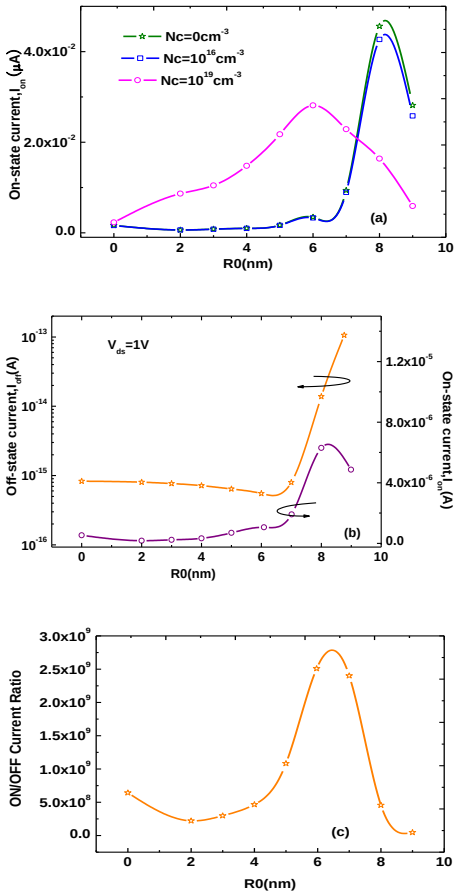

Figure 3: (a) Variation of on-state current I_{on} with different channel doping concentration Nc and core radius R0 when V_{gs}=1V, V_{ds}=0.3V. (b) Variation of I_{on} and I_{off} with intrinsic channel when V_{gs}=1V, V_{ds}=1V. (c) Variation of on/off current ratio when V_{gs}=1V, V_{ds}=1V.

Figure3 (b) shows the off-state current I_{off} and on-state current I_{on} with different R0 when V_{ds}=V_{gs}=1V. The I_{on} has the same trend with the situation that V_{ds}=0.3V. When R0>7nm, the I_{off} has an obviously increase. It may because drain current oscillation which is a byproduct of quantum confinement effect [8]. Figure3(c) shows that the largest on/off current ratio of the GAA-SOI-TFET can be up to 10^9 orders of magnitude when R0 is between 6nm and 7nm. The result is similar with Ref [11].

In Figure4, the characteristics of the average subthreshold swing (SS) and drain-induced barrier-lowering (DIBL) for GAA-SOI-TFETs are shown. TFET has a stepper subthreshold swing compared with the traditional metal-oxide-semiconductor field effect transistor is due to own tunneling transport mechanism has more strong channel current dependence on the bias voltage than the drift0-diffusion mechanism in the common MOSFET[1]. As a result, the key to the better voltage scaling of a TFET than a MOSFET is that SS remains below 60 mV per decade over several orders of magnitude of drain current [1]. In this paper, the average SS is calculated using formula (1):

$$SS = \frac{V_{I=10^{-5}\mu A} - V_{I=10^{-13}\mu A}}{\log(10^{-5}) - \log(10^{-13})} \quad (1)$$

The formula indicates that the SS can be improved by decreased the voltage at I=10^{-5} μA and increased the voltage at I=10^{-11} μA. From the Figure3 (b), it is observed that core can reduce the subthreshold current due to the shielding effect [12]. In other words, with the growth of the core radius, larger voltage is required in order to get the same subthreshold current. Apart from this, Figure3 (a) shows that the on-state current increases with core radius. That means with the growth of the core radius, smaller voltage is needed to obtain the same on-state current. As a result, SS can be improved by an increase in core radius. It is clearly that average subthreshold swing become lower as R0 increase (t_{si} decreases). When R0>2nm, the result means that SS remains below 60 mV per decade over 8 orders of magnitude of drain current.

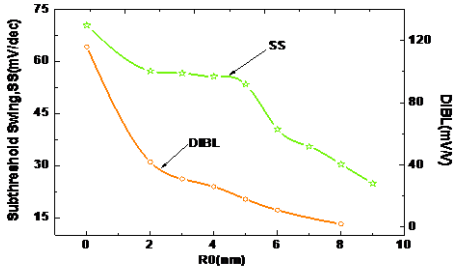

Figure 4: Variations of the average SS and DIBL effect with varied R0 at a fixed channel length L=40 nm. R0=0 correspond to the GAA-SOI-TFET.

The values of DIBL are calculated using the formula (2):

$$DIBL = \frac{V_{th}(V_{ds} = 0.1V) - V_{th}(V_{ds} = 1V)}{0.9V} \quad (2)$$

It is observed that DIBL has a sharp decrease with the introduction of R0 from the GAA-TFET due to improved gate control [12].The GAA-SOI-TFET with R0=8nm is regard as a combination of gate-all-around (GAA) structure and ultra thin silicon shell which has best electrostatic potential control. The thin body can compensate the degraded DIBL by 3-D electric field in the oxide core [12].

Figure5 shows the transfer characteristic of GAA-SOI-TFETs with R0=8nm and R varying from 10nm to 20nm. The dashed lines are the average subthreshold swing (SS). I_{on}, I_{off} and average subthreshold swing are improved with decreased R. Considering the Figure2 and Figure4, the device with smaller effective channel radius (R-R0) has better performances, such as small power consumption and a large drive current.

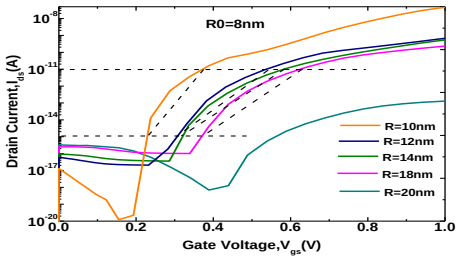

Figure 5: Transfer characteristics of the GAA-SOI-TFET with R0=8nm and R0 varying from 10nm to 20nm. Average subthreshold swing is depicted by dotted lines.

3.3 Effects of gate oxide layer

The dependences of channel current and the average subthreshold slope (dashed lines) on gate oxide layer (t_{ox}) in GAA-SOI-TFETs are shown in Figure6. The transistor has the gate oxide thickness varying from 2.5nm down to 1.5nm. Thicker gate oxide layer causes the worse subthreshold swing due to the weaker gate capability. What's more, the current increase as t_{ox} is decreased. It is because a thinner gate oxide thickness (t_{ox}) will cause a higher electric field in the silicon inversion layer that an enhancement of the band to band tunneling in the TFET occurs and current increases. Similar to the traditional MOSFET, tunneling transistor performance can be improved by using the ultra-thin-gate oxide, e.g. the high-k dielectric.

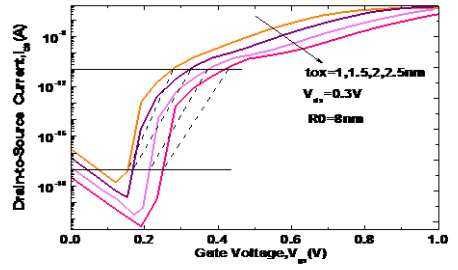

Figure 6: Transfer characteristics of the GAA-SOI-TFET with R0=8nm as a function of gate oxide layer thickness. Average subthreshold swing is depicted by dotted lines.

4 CONCLUSION

The electrical characteristics of the GAA-SOI-TFET are simulated and it is presented that the appropriate effective channel radius (R-R0) and thin gate oxide thickness are the keys for fabricating the high performance GAA-SOI-TFET. The average subthreshold swing below 60mV/dec over 8 orders of magnitude of drain current and leakage current of 10^{-16}Aare obtained. Meanwhile, the I_{on} is 10^{-6} A. The low power consumption and high I_{on} make the GAA-SOI-TFET to be a potential candidate of the MOSFET.

ACKNOWLEDGMENTS

This work is supported by the National natural Science Funds of China (61274096, 61204043). This work is also supported by the Fundamental Research Key Project of Shenzhen Science & Technology Foundation (JC201105180786A), Shenzhen Science & Technology Foundation (CXB201105100089A, CXB201005250031A), The Fundamental Research Project of Shenzhen Science & Technology Foundation (JC201005280670A, JC201105180781A).

REFERENCES

[1] A. M. Ionescu, H. Riel, " Tunnel field-effect transistors as energy-efficient electronic switches," Nature, pp. 329-337, Nov. 2011.

[2] http://www.hqew.com/tech/news/290484.html

[3] S. O. Koswatta, S. J. Koester and W. Haensch, "1D Broken-gap Tunnel Transistor with MOSFET-like On-currents and Sub-60mV/dec Subthreshold Swing," IEEE Electron Devices Meeting, pp. 1-4, 2009

[4] Z. X. Chen, H. Y. Yu, N. Singh, N. S. Shen, R. D. Sayanthan, G. Q. Lo and D. L. Kwong, "Demonstration of Tunneling FETs Based on Highly Scalable Vertical Silicon Nanowires," Electron Device Letter. , vol. 30, no. 7, pp. 754, 2009.

[5] Y. Lu, A. Seabaugh, P. Fay, S. J. Koester, S. E. Laux, W. Haensch and S. O. Koswatta, "Geometry dependent Tunnel FET performance-Dilemma of electrostatics vs quantum confinement," Device Research Conference, pp. 17-18, 2010

[6] A. S. Verhulst, B. Sorée, D. Leonelli, W. G. Vandenberghe, and G. Groeseneken, "Modeling the single-gate, double-gate, and gate-all-around tunnel field effect transistor," Journal of Applied Physics, vol. 107, no. 2, pp. 024518-024518-8, Jan. 2010

[7] K. K. Bhuwalka, J. Schulze and I. Eisele, "A simulation approach to optimize the electrical parameters of a vertical tunnel FET," IEEE Trans. Electron Devices, vol. 52, no. 7, pp. 1541–1547, July, 2005.

[8] K .Trivedi, H. Yuk, H. C. Floresca, M. J. Kim, and W. Hu, "Quantum Confinement Induced Performance Enhancement in Sub-5-nm Lithographic Si Nanowire Transistors," Nano Lett. , pp. 1412-1417, Nov. 2011.

[9] K. S. Yi, K. Trivedi, H. C. Floresca, H. Yuk, W. Hu, "Room-Temperature Quantum Confinement Effects in Transport Properties of Ultrathin Si Nanowire Field-Effect Transistors," Nano Lett. , pp. 5465-5470, Nov. 2011.

[10] K. K. Bhuwalka, S. Sedlmaier, A. Ludsteck, C. Tolksdorf, J. Schulze, and I. Eisele, "Vertical tunnel field-effect transistor," IEEE Trans. Electron Devices, vol. 51, no. 2, pp. 279–282, Feb. 2004.

[11] K. Boucart and A. M. Ionescu, "Double-Gate Tunnel FET With High-κ Gate Dielectric," IEEE Trans. Electron Devices, vol. 54, no. 7, July, 2007.

[12] L. N. Zhang, J. He, C. Y. Ma, X. Y. Zhou, W. Bian, L. Li, and M. Chan," An Oxide/Silicon Core/Shell Nanowire FET," IEEE International Conference on Nanotechnology, 2011