Doping-less Bipolar Transistor with f_T Surpassing that of Conventional BJT

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ABSTRACT

A novel ultrathin SOI based bipolar charge plasma transistor (BCPT) for RF circuit applications is presented in this paper. The proposed device structure exhibits a high cut-off frequency and an improved current drive while still maintaining the inherent super high current gain of the BCPT. Using two-dimensional device simulation, the performance of the proposed device has been evaluated by comparing its charcteristics with those of the conventional lateral bipolar transistor structure. Together with the improved RF characteristics, super high beta, and the fact that the BCPT is fabricated with low thermal budgets without the need for diffusing any impurities into the SOI layer, the proposed BCPT structure becomes a viable option for the future nano-scale BJTs in the BiCMOS technology.

Keywords: Bipolar Charge Plasma Transistor, Silicon-on-insulator, current gain, simulation, CMOS technology.

1 INTRODUCTION

With the integration of the high-density MOS logic with the current-driving capabilities of BJT on silicon-on-insulator (SOI), BiCMOS technology has opened up new avenues for the lateral bipolar transistors (LBT) on SOI. However, to meet the strict demand on device performance parameters such as current gain β, transconductance g_m and cut-off frequency f_T, complex process steps and high thermal budgets are required [1,2]. This can create complications while integrating the bipolar process with the CMOS process. The BCPT structure proposed in this paper overcomes the above issues with the improved current drive, enhanced RF characteristics and a super high current gain. The BCPT has metal electrodes with different work-functions [3-4], to induce (i) electrons for forming the emitter and collector regions and (ii) holes to form the base region. Absence of the doped regions avoids the necessity of complicated thermal budgets using expensive annealing equipment.

2 DEVICE STRUCTURE

Using 2D device simulations [5], the proposed device, which is an improved version of the BCPT [3] as shown in Fig. 1 is simulated and compared with the conventional lateral BJT. The device parameters used in our simulations are given in Table 1 . The work functions of the metal electrodes are chosen to satisfy the following conditions: Emitter and collector work-functions, $\varphi_{m,E}$ and $\varphi_{m,C}$, respectively, less than the work function of silicon (φ_{Si}) and the work function of the base region $\varphi_{m,B}$ greater than the work function of silicon (φ_{Si}).

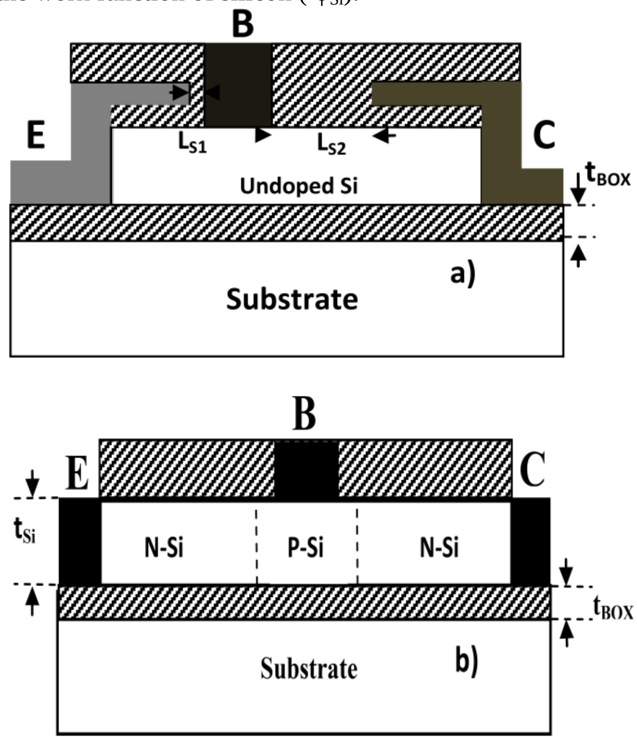

Figure 1: Schematic cross-sectional view of a) the BCPT and b) the conventional BJT.

The choice of the above work function will induce (i) electrons in the emitter and the collector region and (ii) holes in the base region on an undoped SOI layer. It is also important to choose an appropriate thickness for the silicon film. To maintain uniform induced carrier distribution throughout the silicon thickness, from the oxide-Si interface to the Si-buried oxide interface, the silicon film thickness has to be kept within the Debye length, i.e., $L_D = \sqrt{((\varepsilon_{Si} \cdot v_T)/(q \cdot N))}$ where ε_{Si} is the dielectric constant of silicon, V_T is the thermal voltage, and N is the carrier concentration in the body [4]. As shown in Fig. 2, the simulated net carrier concentration (2 nm away from the oxide-silicon interface) for a BCPT structure, under thermal equlibrium and under forward active bias (V_{CE}=1 V and V_{BE}=0.7 V) permits the formation of a BCPT in an undoped silicon film. Identical metal electrode (a stack of TiN/ HfSiOx/ SOI doped with Fluorine) [6] is used for the base contact of the BCPT and the conventional BJT to ensure to

SOI Thickness t_{Si}		30 nm
BOX Thickness t_{BOX}		300 nm
Gate Oxide Thickness t_{ox}		5 nm
Base Contact Length		45 nm
SOI Doping		1×10^{14} /cm^3
Emitter metal work-function		Hf (3.9 eV)
Base metal work-function		5.4 eV
Collector metal work-function		Al (4.28 eV)
Intrinsic Gap length		L_{s1}= 10 nm L_{s2}= 200 nm
	BCPT	**BJT**
Base length	40 nm	145 nm
Emitter length	50 nm	55 nm
Collector length	100 nm	200 nm
Base doping	NIL	9×10^{17}/cm^3
Emitter doping	NIL	10^{20} /cm^3
Collector doping	NIL	2×10^{17}/cm^3

Table 1: Formatting summary for Nanotech manuscripts.

ensure that the base contact properties are identical in both the transistors. The lateral n-p-n structure with which we have compared our results is also an SOI structure and has the same device parameters as that of the BCPT except for the length and the doping concentartion of the base, emitter and the collector region,
which are given in Table 1. The lenghts are chosen so as to have equal neutral base width for both the transistors. The doping profile is chosen similar to that of a practical bipolar transistor.

3 RESULTS AND DISCUSSION

From the gummel plots shown in Fig. 3, it is observed that the collector current of the BCPT is an order higher as compared to that of the conventional BJT, giving a significant boost to the current drive and as well as to the current gain. It is also seen that the BCPT exhibits a lower base current in comparison to that of the conventional BJT. This is due to the SALTRAN (Surface Accumulation Layer transistor) effect at the emitter metal-semiconductor interface as explained in [7]. Consequently, the peak current gain of the BCPT (9313) is several orders higher compared to that of the conventional BJT (16.2) as shown in Fig. 4.

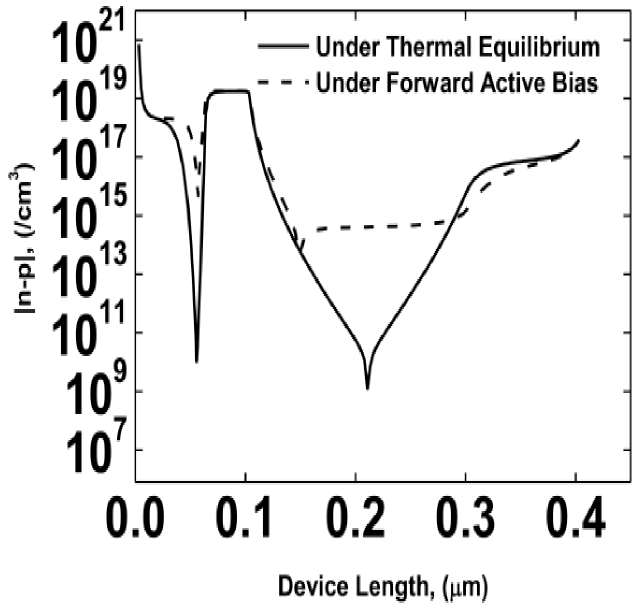

Figure 2: Simulated net carrier concentrations in the BCPT and BJT for different biases.

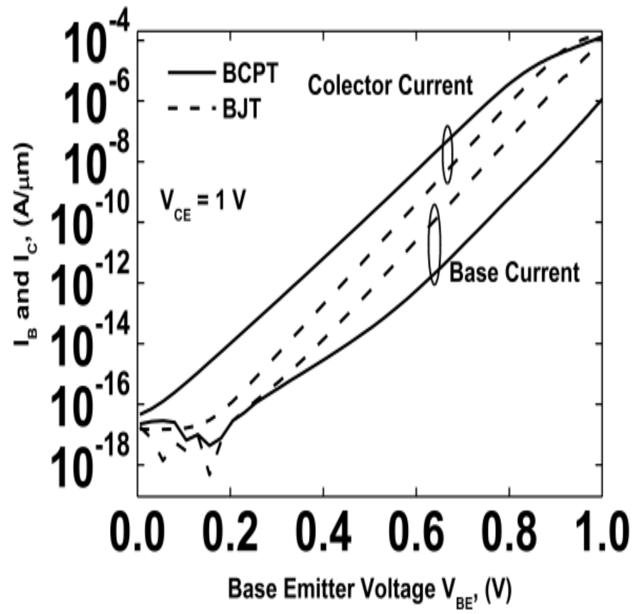

Figure 3: Gummel plots of the BCPT and the BJT.

Cut-off frequency f_T of the BCPT (31.9 GHz) surpasses that of the comparable conventional BJT (17.9 GHz) as can be seen in Fig. 5.Considering the BV_{CEO}*f_T figure of merit, BCPT performs well with a BV_{CEO}*f_T of 51.04 V-GHz (BV_{CEO} =1.6 V) compared to a BV_{CEO}*f_T of 35.8 V-GHz of the conventional BJT (BV_{CEO} = 2 V). As shown in Fig.6a), the saturation voltage ($V_{CE\ (sat)}$) is marginally higher for the BCPT. This is due to the lower electron concentration in the emitter of the BCPT.

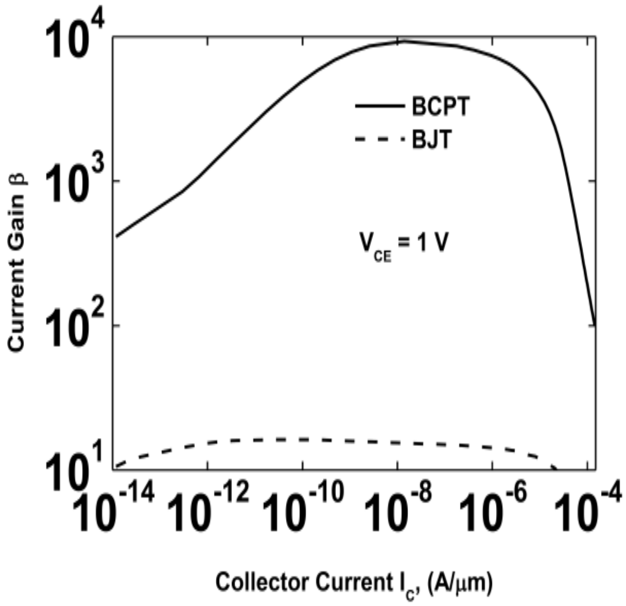

Figure 4: Current gain variation of the BCPT and the BJT.

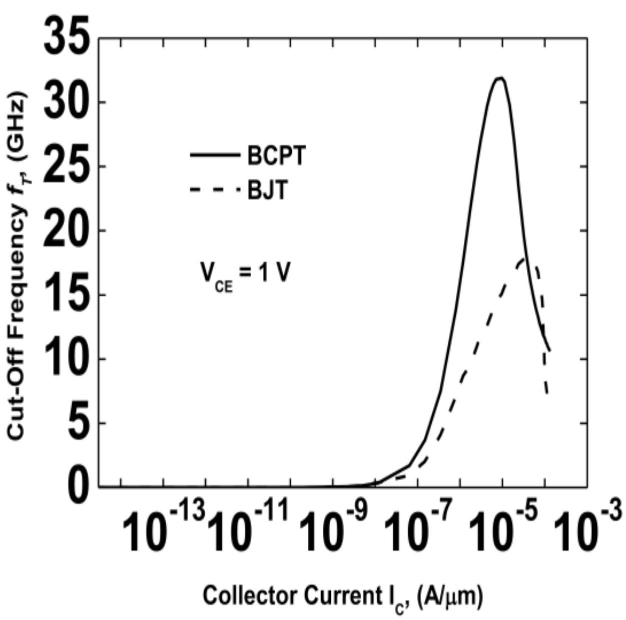

Figure 5: Cut-off frequency of the BCPT and the BJT.

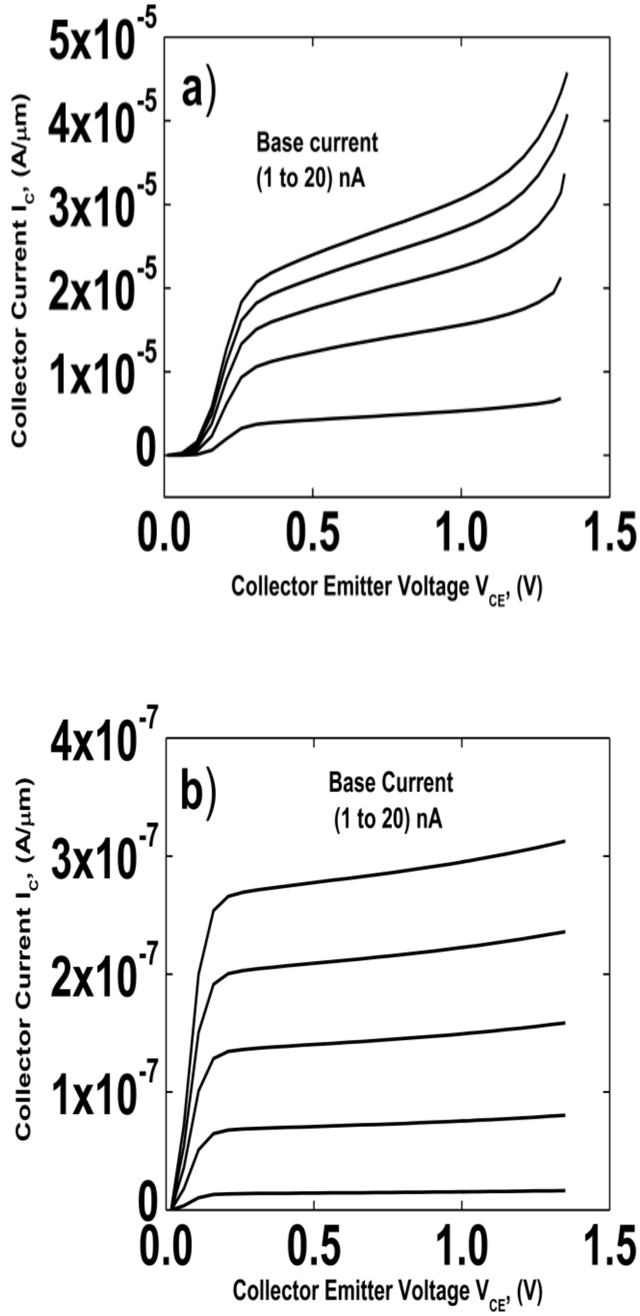

Figure 6: Output characteristics of a) the BCPT and b) the BJT.

4 CONCLUSION

In conclusion, using two dimensional device simulation, a doping-less bipolar transistor is realized that surpasses the dc as well as the AC characteristics of the conventional BJT. This concept can be further explored for realizing BJTs on materials like poly-silicon and laying the foundation for system-on-glass topology.

REFERENCES

[1] M. J. Kumar and D. V. Rao, “A New SiGe Base Lateral PNM Schottky Collector Bipolar Transistor on SOI for Non-Saturating VLSI Logic Design,” Proceedings of the 16th International Conference on VLSI Design, New Delhi, India, pp.489-492, 4-8 January 2003.

[2] M. J. Kumar and D. J. Roulston, “New buried P+ grid poly-emitter bipolar transistor,” Solid-state Electronics, Vol. 38, no.10, pp.1854-1856, October, 1995.

[3] M. J. Kumar and K. Nadda, “Bipolar charge plasma transistor: A Novel Three Terminal Device,” IEEE Trans. Electron Devices, Vol. 59, No. 4, pp. 962-967, April 2012.

[4] B. Rajasekharan, C. Salm. R. J. E. Hueting, T. Hoang, J. Schmitz, “The charge plasma p-n diode,” *IEEE Electron Device Letters*, vol. 29, pp. 1367-1369, December 2008.

[5] *ATLAS Device Simulation Software*, Silvaco Int., Santa Clara, CA, 20110.

[6] A. Fet, V. Haublein, A. J. Bauer, H. Ryssel, and L. Frey, “Effective work function tuning in high-k dielectric metal-oxide semiconductor stacks by fluorine and lanthanide doping,” *App. Physics Letters*, Vol. 96, no. 5, Feb. 2010.

[7] M. J. Kumar and V. Parihar, “Surface Accumulation Layer Transistor (SALTran): A New Bipolar Transistor for Enhanced Current Gain and Reduced Hot-Carrier Degradation,” *IEEE Trans. on Device and Materials Reliability*, Vol. 4, no.3, pp. 509-515, Sep- 2004.