Investigation on Reliability of Interconnects in 3D Heterogeneous Systems by Ageing Beam Resonance Method

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ABSTRACT

This paper is the ongoing research report and discusses important aspects of new investigation method selected for interconnects reliability and ageing which has to be considered in nano-scale. The research is ongoing and applies to heterogeneous device structures like SiP, SoC where mechanical stress caused by thermal cycling, heat dissipation, assembly technique etc. distributes inside thin layers of metal interconnects [1, 2]. Several approaches have been presented on functional aspects as well as the influence of integration technology on the system behavior in context of the 3D integration design process of micro systems. One of approaches (the modular simulations by with PDE solvers and model generation for system level simulation) is presented in [3].

Practical experience from R&D European projects like successfully concluded e-Cubes [4] (thermo-mechanics), SE2A [5] (accelerometer design & integration) and Corona [6] project (heterogeneous systems design methodology), as well as on-going projects like e-BRAINS [7], Parsimo [8] and SMAC [9] led to focusing on investigation of interconnects reliability. As technical feedback to the designers on interconnect design rules and long-term properties referring several operation domains is necessary the research on interconnect ageing method will be presented in this paper starting from problem identification, through simulation results by CoventorWare and Comsol systems, test structures design, measurements methodology, to device fabrication, and perspective of measurements, results conclusions.

Keywords: accelerated ageing, indirect method, MEMS beam, interconnect reliability, SiP

1 OVERAL IDEA

The accelerated ageing technique has been developed and applied. It relies on MEMS silicon cantilever beams excited by an external mechanical vibration system. It allows to speed up the ageing process by high frequency vibration. Single second of experiment with beam mechanically stimulated by substrate vibration should reflect respective number of stress cycles based on beam oscillation frequency.

Dedicated silicon MEMS structures for accelerated ageing process (AABS – Accelerated Ageing Beam Structures) with metal interconnects on the top of the beam which undergoes ageing investigation have been fabricated in ITE (Fig.1). Resonant frequencies of the 1'st harmonic vibration mode vary from single 0.5kHz up to 20kHz. Predicted resonant modes have been successfully verified by experiment based on MEMS cantilever beam [10] developed in frame of e-BRAINS project [7]. AABS parameters have been calibrated. MEMS silicon cantilever beams length varies from 1mm to 4mm, width is 300-700um for thickness in range 5-20um. Following the simulation results in some cases (long cantilever beam structures) it is even possible to exceed elastic deformation of metallization and led the metal interconnect into plastic deformation in mechanical resonance conditions.

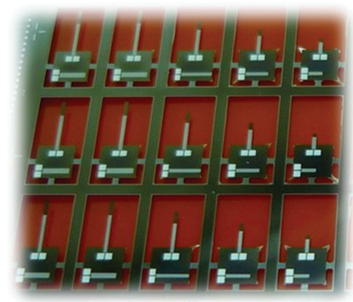


Figure 1: Real test structures developed in ITE for experimental verification of CoventorWare and Comsol Multiphysics modeling and simulation results.

On the current stage of investigation the interconnects layer is made from aluminum. In order to strengthen results of metal degradation the AABS MEMS and make ageing results better detectable, the design has been optimized by application of specific interconnect layout with a dedicated multi-bend strip chaining in the beam root area (Fig.2). It is expected that for the 1'st vibration mode mechanical stress should reach highest levels in this area. It is expected that the applied measurement method (discussed below) should detect noticeable interconnect degradation.

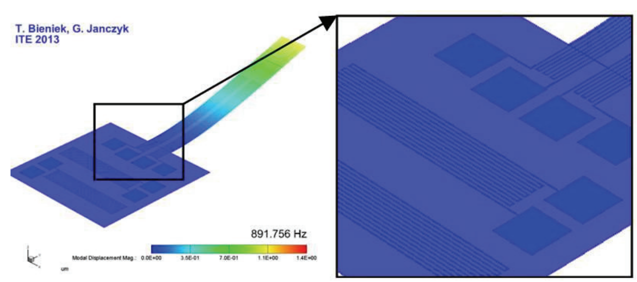


Figure 2: First harmonic resonance mode with multi-bend interconnect strip.

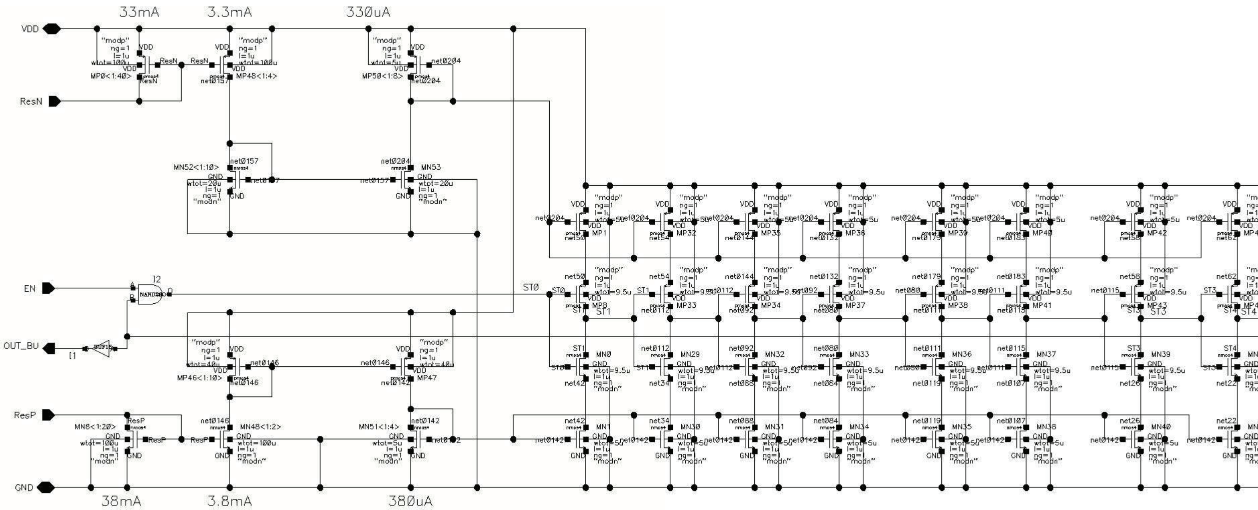


Figure 3: Dedicated RO structure.

2 METHODOLOGY

Interconnect degradation stimulated during accelerated ageing will be evaluated on the basis of measurements on interconnect resistance. To achieve sufficient measurement stability, accuracy and real-time observation of ageing phenomena and progress of interconnect degradation dedicated an indirect measurement technique has been elaborated, implemented and will be applied during the experiment on accelerated ageing soon.

The fundamental assumption is that material fatigue causes deviation in interconnect resistance. There are expected two types of resistance deviation:

- reflecting material ageing, observable after series of ageing experiments;
- reflecting temporary deformations of the interconnect material - temporary deviation observable only in a real time during mechanical excitation of the cantilever beam.

The first type of deviation can be well investigated by precise measurements of impedance. Accurate measurement of second phenomena has to be recorded in a real time and it is expected to observe deviation of interconnect resistance during the accelerated ageing experiment. If so, it will affect frequency of a dedicated ring oscillator (RO) sensitive on interconnect resistance (Fig.3). The metal layer is placed on the dedicated MEMS cantilever beam exposed on vibration. There are multiple passes of the interconnect strip through the area of peak deformation and mechanical stress (Fig.2).

3 INDIRECT MEASUREMENTS

The dedicated RO is the clue of real-time observation of interconnect ageing process. It is designed to achieve 5% deviation of oscillation frequency with nominal frequency 25MHz. Deviation of RO frequency stimulated by layer deformation is transformed into subsequent PDM signal modulation (PDM - pulse density modulation). Following the Fig.4 RO is followed by frequency demodulator and an amplifier which support correlation of the output voltage with deviation of the interconnect resistance.

As it comes from Fig.3 this is a 9-stage RO structure driven by cascade of current mirrors and controlled by two complementary current sources driven by interconnect resistance. For the case the interconnect resistance is 50Ohms. Whole the readout system has been developed as an ASIC being prototyped by Europractice service in AMS 0.35um technology. The detection concept is based on current controlled ring oscillator which output frequency depends on the value of external metal resistors formed by metal paths deposited on MEMS cantilever beams. Resistance change causes ring oscillator current change what results in output frequency change. This frequency change is detected by frequency demodulator. Demodulator AC output signal is amplified by output amplifier (Fig.4).

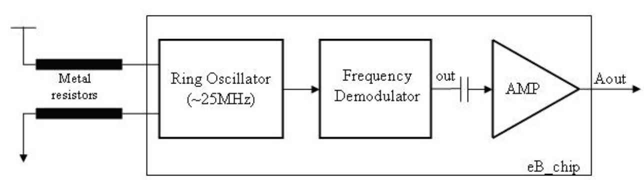


Figure 4: Block diagram of the readout chip

The readout chip has been design for AMS 0.35µm CMOS process in Cadence environment. Results of ring oscillator simulations have presented on figures 5 to 7, where RFACT is a normalized metal resistance factor and RFACT=1 corresponds to 50Ohms of nominal resistance value. Dependence on deviation of fabrication process parameters (mismatch of parameters) is presented on Fig.5. Three parameters sets have been taken into consideration (three from five predefined): TM - typical mean - statistically most common (middle line), WP - worst case - power (top line) and WS - worst case - speed (bottom line). One can see that all worst case simulations meet specification and assumptions on selected indirect measurements method.

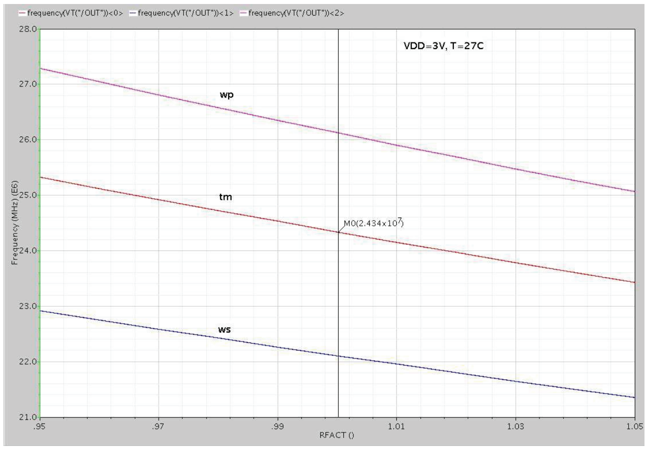


Figure 5: Ring oscillator output frequency vs. resistance change (process variation)

Dependence on temperature variation (Fig.6) covers ASIC device temperatures ranging from -40°C (top line), 27°C (middle line) and +85°C (bottom line). Those results also meet expectations on RO behavior dependence on temperature change.

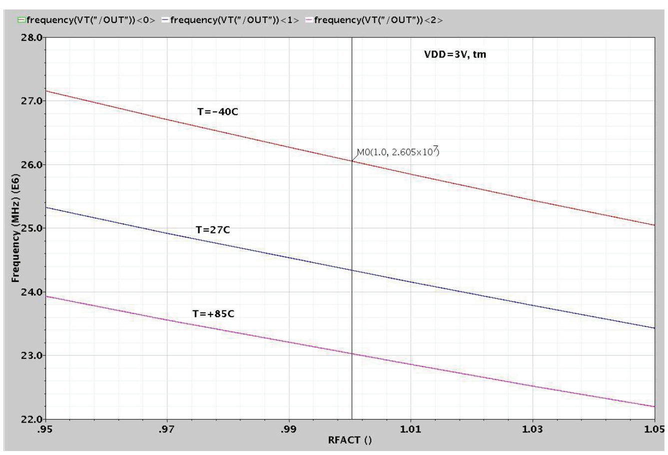


Figure 6: Ring oscillator output frequency vs. resistance change (temperature variation)

For typical process (TM) and T=27°C, nominal output frequency is about 24.4MHz. As it can be seen, for +/-5% resistance variation, output frequency change is about +/-1MHz (+/-4%). As it comes from the Fig.7 the output signal change of the demodulator is about 120mVpp for corresponding RO frequency.

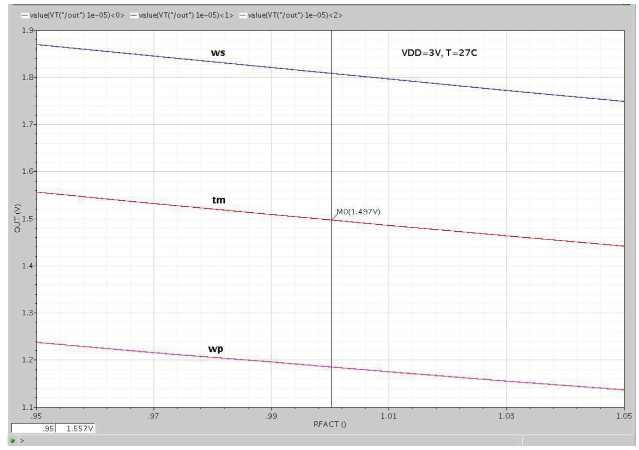


Figure 7: Frequency demodulator output vs. resistance variation

The ac output signal of the demodulator is amplified by an output amplifier by the factor of 8. It gives maximal output signal of about 1Vpp on VDD/2 dc level (for +/-5% resistance variation). Final chip layout has been presented on Fig.8.

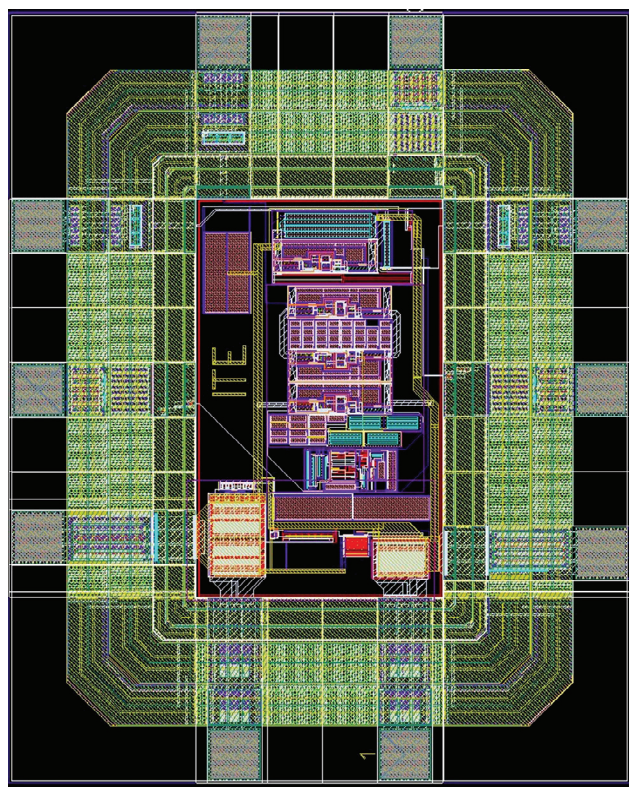
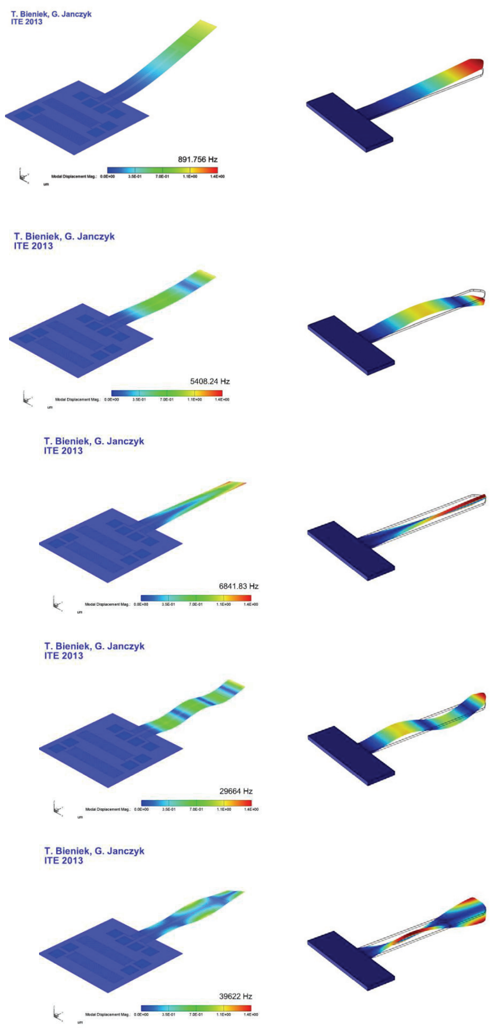


Figure 8: Final layout of the readout indirect measurements chip (AMS 0.35μm CMOS)

4 WORKPLAN

After the successful fabrication of the readout ASIC and subsequent cantilever beams the series of real case measurements will be performed for various temperatures, and excitation frequencies. According to the presented oscillation modes: basic (Fig.9a) and subsequent harmonic basic modes (a,b,d) and twisting ones (c,e), the next step of the experiment will cover investigation on stimulated ageing with high frequency beam stimulation for cantilever beams with interconnects and strips layout optimized to profit from multimode excitation. Various interconnect materials like Al, Au, Ti will undergo investigation.



a) 1'st mode basic: 891Hz

b) simple

c) twisting

d) simple

e) twisting

Figure 9: Modal analysis of beam excitation by CoventorWare (left) and Comsol (right).

5 CONCLUSIONS

This paper presents methodology of investigation for accelerated ageing of thin metallization layers commonly met in 3D heterogeneous structures prone to thermo-mechanical cycling which stimulates thermo-mechanical generation of mechanical stress and interconnect ageing. The paper presents in details dedicated MEMS structures along with description of ageing indirect measurement technique profiting from ageing-sensitive ring oscillator structure.

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