A Novel Simulation Methodology For Full Chip-Package Thermo-Mechanical Reliability Investigations

B. Karunamurthy*, T. Ostermann** and M. Bhattacharya***

*KAI Kompetenzzentrum Automobil- und Industrieelektronik GmbH,
Technologie park, Europastrasse 8, Villach, 9524, Austria, bala.karunamurthy@k-ai.at
**Infineon Technologies, Villach, Austria, thomas.ostermann@infineon.com
***Coventor Inc, Sunnyvale, CA 94086, USA, monojitb@coventor.com

ABSTRACT

A methodology for simulating the accurate 3D structural details of a non-planarized technology chips is presented. This approach uses a virtual semiconductor fabrication technique to create geometry and finite element mesh on complex chip topology features. Multi-scale simulations are used to compute the strains and stresses induced on the chip by the package when exposed to thermal loads. A microscopic power metal stack of a power IC was simulated to demonstrate this new simulation methodology and the results are presented. These numerical simulations, which included the non-linear behavior in the matrix, show that the detailed information of the large stress and strain gradients in the micro-fields can be obtained.

Keywords: simulation, thermo-mechanics, reliability, chip-package, virtual fabrication

1 INTRODUCTION

It is well known that thermo-mechanical related failures account for almost 65% of the reliability problems in the semiconductor industry [1]. These failures, such as cracks and delamination are driven by stress arising due to the thermal coefficient mismatch between the materials. Chips are integrated in advanced packages, typically made of plastic. The stress induced by the package on the chip is critical and is often evaluated by finite element simulations. Normally, the chip is assumed to be a homogenous and isotropic block of silicon. This level of abstraction provides no information on the stress behavior of thin films, such as metals and dielectrics on the chip. The in-plane and out-of-plane shear stresses imposed on the chip by the package are higher at the corner and at the edges of the chip. This shear stress in conjunction with the chip internal stress can cause plastic deformation in high CTE (Coefficient of Thermal Expansion) materials such as metals and cracking in the low CTE dielectric materials such as oxide and nitrides. This leads to failures like short circuits, leakage current and corrosion. Multi-scale and multi-level simulations are the state of the art approach to include these thin films in the model [2,3]. However, the topological features of these thin layers are neglected due to the complexity in geometry and finite element mesh generation. This leads to an inaccurate stress prediction, because the magnitude of stress in built-in features e.g. via is much higher compared to planar layers [4].

Non-planar technology is cost effective as it reduces the number of wafer fabrication processes. These chips have complex topological features as shown in Figure 1. A two dimensional modelling of such structures by digitizing images obtained from scanning electron microscope was reported early by the author [5]. Stress redistribution, brittle cracks and plastic yielding are prevalent at the corners and therefore a 3-D study becomes mandatory. Creating a 3D geometry using CAD (Computational Aided Design) programs is very tedious and time consuming. This work provides a methodology to accurately include these structural details in 3-D, thereby providing the details of localized stresses at micro level in a relatively large package. The virtual fabrication platform used to create geometry and finite element mesh is described in the Section 2. Section 3, describes the multi-scale modelling used to integrate the mesh generated by this technique. An example model of a power metallization stack is also presented in the last section.

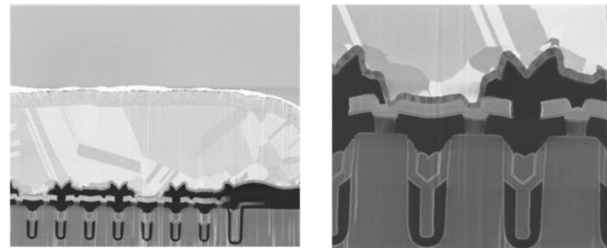

Figure 1: SEM images of non-planarized topology chips

2 VIRTUAL FABRICATION PLATFORM

A virtual fabrication platform called SEMulator3D™ is a 3D semiconductor process modelling software that utilizes “voxel” [6] based engine instead of traditional Nurbs (Non-uniform Rational Basis Spline) or BREP (Boundary Representation) for geometry generation. Voxel’s are 3D pixels that can be deposited and etched away from a 3D mathematical space. Compared to traditional methods, the voxel based SEMulator3D™

propriety algorithms are uniquely fault tolerant to the complex shapes routinely encountered in semiconductors. To accurately model geometries a library of process steps with settings to control various process parameters is employed. For instance, a High density Plasma Chemical Vapour Deposition (HDP-CVD) process is described using 10 topology parameters such as “angle of minimum deposition rate” and “deposition rate at minimum angle”. Furthermore, the proprietary compression algorithms integrated into the geometric kernel also enable the large scale modelling necessary for thermo-mechanical analysis as well as to gain speed advantage for fast Design-of-Experiments (DoE) studies.

The flow consists of reading 2D layout information in GDS or DXF format and entering the process stack information using a library of processes. Both layout and process parameters can be changed to create iterative design changes. As illustrated in Figure 2 the SEMulator3D^{TM} engine integrates the two pieces of information, layout and process stack, to automatically generate a 3D representation of the device.

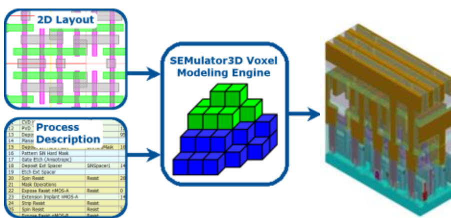

Figure 2: SEMulator3D design flow

A built-in and full-featured mesher in SEMulator3D^{TM} is used to generate a volume mesh. The SEMulator3D^{TM} mesher can create linear and parabolic Tetrahedron mesh and has local and global settings. The mesh algorithm is adaptive and iteratively re-meshes the geometry based on user-defined accuracy settings to achieve an optimum size and accuracy balance.

The generated volume mesh is then read into ANSYS [7], a commerical FEM software for simulation. Nested sub-modelling approach is employed, where the displacements from the package model are transferred to the chip model using cut-boundary interpolation.

3 SIMULATION METHODOLOGY

This section describes the methodology implementation on a power IC. The mesh generated on the chip features cannot be integrated directly into the global model for a single step simulation due to computational limits. A conformal meshing on such a system would result in several hundred millions of elements, making it computationally expensive. A multi-scale modelling is therefore used, namely sub-modelling, which allows the transfer the displacements from the global package model to the chip micro model. The simulation is performed sequentially in three stages on three models as shown in Figure 3:

1. The global model, which consists of plastic package, lead frame and silicon and an equivalent material layer, is computed for strains and stresses for the required thermal loading. This equivalent material layer is homogenized and assumes the effective linear elastic material properties among the volume averages of the micro layers. A quarter of the chip-package system is simulated by taking advantage of the symmetry.

2. The first sub-model was built with all chip planar layers, which was represented by the equivalent layer in the coarse model. The displacements from the global model are transferred as boundary conditions to the exterior nodes for each load step to be simulated.

3. Mesh output from SEMulator3D, is the micro-model and the region of interest for reliability investigations. The displacements from the first submodel are transferred as boundary conditions. This model is then solved by the same method to obtain local stress and strain data.

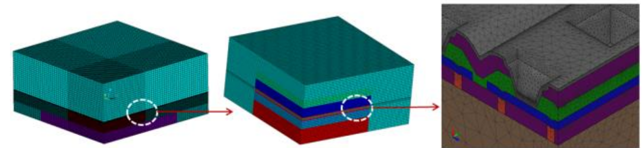

Figure 3: Multi-scale models: coarse, sub-model and micro-model

Figure 4 shows the simulation flow of this approach. A chip layout file is read-in along with the process description. The geometry at the region of interest in the chip is created, which in this case, is 30 X 30um. The size of the features in the model range from 0.3 um to 20 um. The built-in mesher generates a volume mesh, which can be directly transferred to ANSYS. The global and the first sub-models are solved, followed by the chip micro-model. The global and first sub-models are created in FEM software and the micro model is created by SEMulator3D. Mesh settings and program controls allow the mesh refinement at desired regions, thereby providing sufficient elements even in the 0.3um thick features. The resulting finite element mesh on the “via” region is shown in the Figure 3.

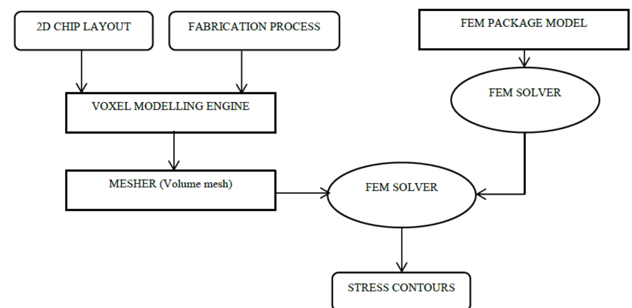

Figure 4: Simulation Methodology flow chart

3.1 Material Models

The system consists of elastic, elastic-plastic, temperature dependent and visco-elastic materials. The material data used for these simulations are listed in Table 1. The chip multi-layer system is normally subjected to cyclic loading which results in thermo-mechanical fatigue. This could cause plastic shake down, ratcheting and crack initiation and propagation. Therefore, the elastic-plastic behaviour of the materials was included in the simulation for accurate stress prediction. The shear stresses imposed by the package during mould compound shrinkage are important, so the time-dependent strain rate is also included. The material models used in this study were obtained from our previous characterization work and also from literature [8 -10].

Table 1: Material data used for simulation

Material	Model
Silicon	Temperature dependent
Mould compound	Visco-elastic (Prony)
Lead frame	Elastic-plastic (KINH)
Polyimide	MKIN
Copper	Elastic-plastic (BKIN)
Titanium	Elastic-plastic (BKIN)

3.2 Chip Package Analysis

The global model, which includes the equivalent layer and silicon in a package, is simulated for one temperature cycle: ramp up to 150^0C and ramp down to -55^0C. The system is assumed to be stress free before loading i.e. no residual stresses were taken into account for this simulation. Also, perfect adhesion between the material interfaces was assumed. The resulting in-plane shear stress on the chip is shown in Figure 5.

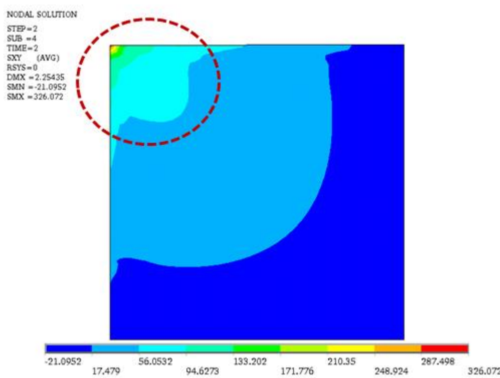

Figure 5: In-plane shear stress on the chip

The mould compound with higher CTE shrinks further compared to the low CTE silicon. Therefore, intense stress concentration is observed at the chip corner, with the deformation direction acting towards the centre as marked in Figure 5. This helps to identify the critical chip region and to decide where to build the sub and micro models. The other shear stress components, which are out-of-plane, are concentrated at the chip edges. These shear stresses are often the major cause for chip failures, such as passivation cracks, metal plastic deformation and delamination. In order to illustrate our simulation methodology, we choose to place the sub and micro models at the chip corner.

3.3 Power Metallization Stack

The power metallization stack in the DMOS region of a power device was built and simulated as the micro-model. This stack consists of several layers with via holes between metals to allow electrical connectivity. Metals are separated by oxide and nitrides, which act as inter-layer dielectric. During active cycling, temperature loads are applied in this stack, which lead to crack formation after several thousand cycles as shown in the Figure 6 (a). Due to the complexity in this geometry and observed crack, we used this structure to demonstrate our methodology for identifying stress peak locations.

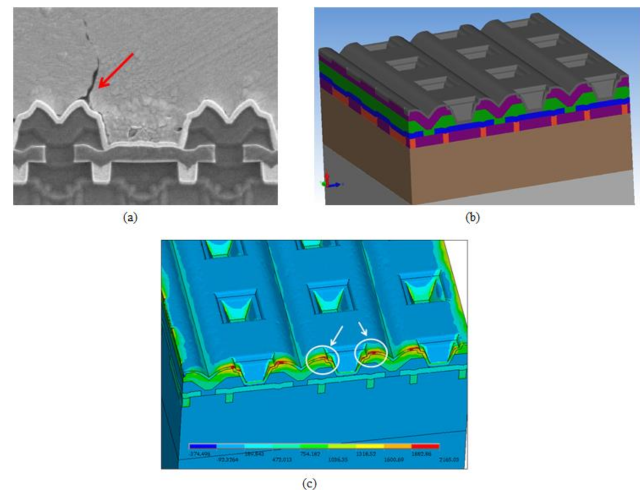

Figure 6: (a) Crack near via region (b) 3D Micro-model (c) Stress contour on the micro-model

By computing the micro-model for thermal loads along with the boundary conditions from the sub-model applied, stress concentrators are seen at the edges of the passivation as marked in the Figure 6 (c). These stress peak regions correspond with the cracking location identified in the active cycling experiments. The large power metal on top of this passivation can expand and contract much higher due to low stiffness and higher CTE values. The passivation layer, which is much stiffer compared to the metal act as a structural constraint for the metal expansion and contraction. Therefore stress is generated on the passivation layer. This stress accumulates at the corner of the via regions and reaches up to 2 GPa for a single temperature cycle. This stress magnitude is lower than the fracture strength of this passivation layer (Nitride), which is reported as 8-9 GPa [11], and therefore this may or may not be sufficient to cause fracture. Hence, it is likely that the

observed cracks are initiated during one of the subsequent thermal cycles.

When this stack is subjected to several hundreds or thousands of thermal cycles, thermo-mechanical fatigue will occur. Fatigue causes micro-structural changes in the metal in the form of plastic deformation. These changes will alter the magnitude of the stress state at this corner region because of stress redistribution and as a result of yielding. Simulating this 3D micro-model for several temperature cycles is not possible due to computational limits. However, this result help identify the likely locations of failures. Including the chip topology is therefore important to accurately predict the damage locations. With this knowledge, further simulations on failure or damage initiation and growth can be performed. Homogenizing or assuming the chip layers as planar in simulation would not be possible to achieve this otherwise.

4 CONCLUSIONS

A methodology to compute stress and strain distribution at the 3D micro level on an complex non-planar chip topology is presented. The virtual fabrication platform used in this work made it possible to achieve this in a reasonable time. The simulated micro region of a power metal stack, showed a good correlation with the likely damage initiation locations. Stress-strain data from these FEM results provides a substantial contribution to the thermo-mechanical reliability investigation to further investigate the material, design and failure growth in order to safe design for increased life time. This study concludes as follows:

1. Extremely complex 3D chip topologies can be built and meshed by utilizing 3-voxel based engine and built-in mesher of SEMulator3D^{TM}.
2. Multi-scale modelling allow to integrate this micro-model in a global package to capture the local stress field for the loads applied globally.
3. FEM results obtained using this methodology help thermo-mechanical reliability investigations by identifying likely damage initiation locations.
4. The simulation methodology proposed here is not limited to thermo-mechanics, but can be extended for other fields of engineering simulations.

Acknowledgements

This work was jointly funded by the Austrian Research Promotion Agency (FFG, Project No. 831163) and the Carinthian Economic Promotion Fund (KWF, contract KWF-15212274134186).

REFERENCES

[1] G.Q. Zhang, W.D. van Driel , X.J. Fan, Mechanics of Microelectronics (Solid mechanics and its applications), Springer; 1 edition, ISBN-13: 978-1402049347

[2] L Mercado, C Goldberg, S Kuo. A simulation method for predicting packaging mechanical reliability with low κ dielectrics, Interconnect Technology Conference, 2002. Proceedings of the IEEE 2002 International, pp. 119 – 121

[3] V. Fiori, S. Orain. A Multi Scale Finite Element Method to Evaluate Bond Pad Architectures. 6th. Int. Conference on Thermal, Mechanical and, Multiphysics Simulation and Experiments in Micro-Electronics and Micro-System, EuroSimE 2005.

[4] A.G. Evans, J.W. Hutchinson. The thermomechanical integrity of thin films and multilayers. Acta Metallurgica et Materialia. Volume 43, Issue 7, July 1995, Pages 2507–2530

[5] J Zarbakhsh, B Karunamurthy, C Trejo-Caballero, E Barti, T Detzel. Microscopic stress simulation of non-planar chip technologies. Microelectronics Reliability, Volume 50, Issues 9–11, September–November 2010, Pages 1666-1671

[6] Coventor, Inc. *SEMulator3D* (v2012) User Guide

[7] ANSYS. Academic Associate, Release 14.0.

[8] J Zarbakhsh, M Lederer, R Huang, T Detzel and B Weiss. Modeling of Multi-Temperature-Cycle Wafer Curvature. ITherm 2010: 12th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, Las Vegas, Nevada, USA, 02.06.2010

[9] K Matoy. Micro-Mechanical Characterization of Silicon based Dielectric Films and Metal/Dielectric Interfaces. Doctoral Thesis, Montanuniversität Leoben, Leoben, 2009

[10] P Alpern, P Nelle, E Barti, H Gunther, A Kessler, R Tilgner and M Stecher. On the Way to Zero Defect of Plastic-Encapsulated Electronic Power Devices—Part II: Molding Compound. IEEE Transactions on Device and Materials Reliability, Volume 9, No. 2, June 2009

[11] K Matoy, H Schönherr, T Detzel, G Dehm. Micron-sized fracture experiments on amorphous SiOx films and SiOx/SiNx multi-layers. Thin Solid Films (518), (2010) pp. 5796-5801