Ink-jet Printed CdS Thin Film Transistors Fabricated In-situ by Micro-reaction

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ABSTRACT

In this work, we report a simple, mask-free, very low material wastage method to deposit nanocrystalline CdS thin films as semiconducting layer for thin film transistors (TFTs). This method combines on-chip synthesis and ink-jet printing techniques. The physicochemical and morphological properties of the films were studied in function of jetting parameters including printed volume and substrate temperature. The fabricated TFTs have n-type conduction with resistivities in the order ~1x10^5 Ω·cm, on/off ratios of ~10^3, V_T of ~3.4 V and mobility (μ_{SAT}) of ~0.1 cm^2/V·s. This approach demonstrates a new and efficient solution-process route for manufacturing semiconductor CdS thin films with performance comparable or better than several organic n-type semiconductors.

Keywords: on-chip synthesis, inkjet printing, solution processes, thin film transistors, inorganic semiconductors, cadmium sulfide.

1 INTRODUCTION

Given its potential low cost, printed electronics has become a promising technology to replace conventional photolithography-based manufacturing for flexible electronics. In particular, a solution-based technique, inkjet printing to process solution-processed semiconductors has advanced rapidly [1]. However, several issues remain unsolved in inkjet. Among the most important are the fact that most inkjet printable semiconductors are organic molecules with mobilities lower than 10^{-2} cm^2/V·s and the poor air and moisture stability of the resulting devices. Both of these compromise device lifetime and reliability [2]. On the other hand, inorganic II-VI chalcogenide semiconductors, such as cadmium sulfide (CdS), offer the possibility to fabricate devices with higher performance and excellent chemical stability. In addition, II-VI materials can be synthesized using solution-based processes through a variety of routes [3,4]. Several authors have reported deposition of CdS thin films active layers in electronic devices by first printing nanoparticles and then annealing the resulting films. Such techniques yield devices that are stable in air and moisture [5]. However, these devices have poor performance. Furthermore, this technique requires the synthesis of nanoparticles with tight size distribution as well as the use of organic stabilizers to maintain the nanoparticles dispersed in the ink. Organic stabilizers can potentially degrade the electrical performance of the resulting devices. In addition, the required high annealing temperature required to remove the organic stabilizers and sinter the nanoparticles is incompatible with flexible substrates [6].

In this work, we report the study of a simple method to produce nanocrystalline CdS thin films that are used as semiconducting layer in thin film transistors (TFTs). This method combines the merits of on-chip synthesis without the need of nanoparticle synthesis and ink-jet printing to selectively deposit the material without the need of further patterning.

2 EXPERIMENTAL

2.1 Ink formulation

The ink was prepared using cadmium acetate dihydrate ($Cd(CH_3COO)_2 \cdot 2H_2O$) [0.1 M] as cadmium source and thiourea (CH_4N_2S) [0.2 M] as sulfur source. Both reagents were mixed in a 95:05 methanol/ethylene glycol solution. All reagents were used as purchased without any further purification.

2.2 Thin film deposition and devices fabrication

The devices were printed in a commercial Omini Jet 100 printing system. Cartridges with a printing volume of 5pL were used. To optimize the inkjet printing the number of drops and substrate temperature were initially studied. TFTs were fabricated with the optimized parameters using a bottom, gate-top contact architecture, as shown in Figure 1. First, 500 nm of SiO_2 were thermally growth on a Si wafer as an insulating substrate. Then, 100 nm of gold (Au) was deposited by e-beam evaporation and patterned to form the gate contact. Next, 90 nm of hafnium oxide (HfO_2) was deposited using atomic layer deposition (ALD) as gate dielectric followed by the printing of the CdS films. The CdS was printed at room temperature and atmospheric conditions in the active areas on top of the HfO_2 surface.

During the printing process, the ink spreads in the active channel area and dries forming a thin layer with both precursors. After printing, the devices were transferred to a glove box filled with nitrogen (N_2) to carry out the CdS reaction. The reaction is performed in a hot-plate at 200 °C for 60 min. This results in CdS films ~50 nm thick. To further remove any organic contaminants, resulting from the reaction, the samples were annealed in air at 300 °C for 60 min. Later, 500 nm of parylene were deposited as hard-mask and the gate dielectric patterned. Finally, 100 nm of aluminum were deposited and patterned to define the TFT channel. This results in TFTs with channels width and length in the range of W = 40 to 80 μm and L = 80 to 160 μm, respectively (inset Figure 1).

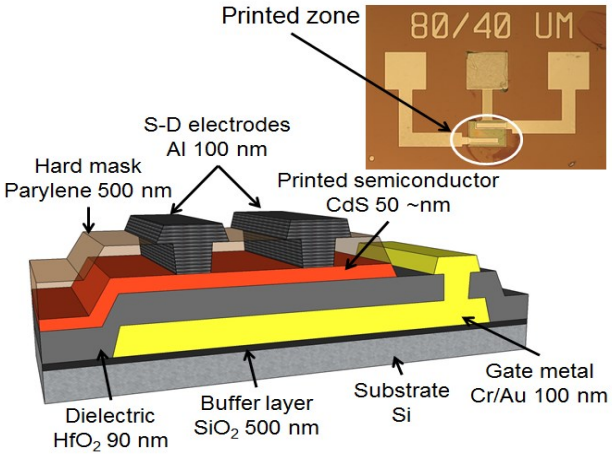

Figure 1. Schematic cross section of the TFT with printed CdS. Inset shows the actual device with CdS printed in the active zone (circled).

2.3 Films and devices characterization

The characterization of the resulting CdS films was performed using by X-ray diffraction (XRD) to define its crystalline structure. Morphology and thickness were analyzed by scanning electronic microscopy (SEM). X-ray photoelectron spectroscopy (XPS) was used to study chemical composition of the films. Resistivity was determined by transmission line model (TLM), as reported elsewhere [6]. The electrical characterization of the TFTs was evaluated using current–voltage (I–V) measurements at room temperature in air under dark conditions.

3 RESULTS AND DISCUSSION

One of the main features of the proposed approach is its simplicity. The printing and reaction of precursors takes place without stabilizers and the solvent acts simply as a transport medium. The CdS film synthesis occurs by heterogeneous nucleation on the substrate surface in solid state as heat is transferred to the deposited precursors through the overall reaction:

$$Cd(CH_3COO)_2+2(SC(NH_2)_2 \rightarrow CdS+(CH_3COOH)+2(NH_2CN) \quad (1)$$

Thiourea decomposes producing hydrogen sulfide and cyanamide. Cadmium acetate decomposes releasing the Cd^+ ion and an acetate group. The Cd^+ ions react with the sulfur from hydrogen sulfide, providing two hydrogen ions that interact with the acetate groups to produce acetic acid and cadmium sulfide.

The XRD results of the films exhibit characteristic peaks of the hexagonal phase of CdS, in good agreement with the JCPDS XRD spectra data (JCPDS No. 6-314) [7]. The presence of a broad CdS peaks indicate the potential formation of nanocrystalline films (Figure 2).

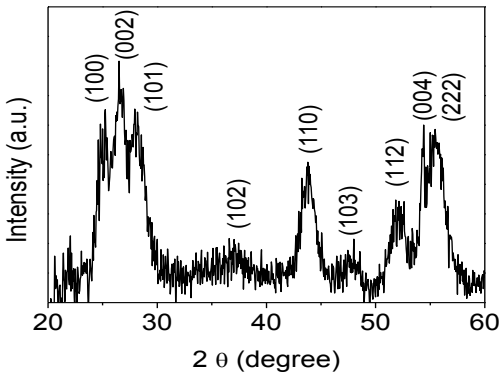

Figure 2. XRD pattern of CdS thin films with hexagonal phase.

XPS analysis confirmed the formation of CdS (Figure 3a). Figure 3a shows the characteristic doublet with spin-orbit separation of 6.6 eV and binding energies of 404.8 eV and 411.5 eV corresponding to the 3*d*5/2 and 3*d*3/2 electronic transitions of Cd bonded to S, respectively. The sulfur 2*p* spectrum exhibits a doublet from the spin-orbit split 2*p*3/2 and 2*p*1/2 with a separation of 1.18 eV at binding energies 161.0 and 162.2 eV, also corresponding to CdS (Figure 3b). Spectra deconvolution exhibits also a doublet at 405.8 and 412.4 eV in the Cd region and other one at 161.8 and 163.0 eV in the S region. These signals are related to oxidized form of CdS, such as $CdSO_3$ that are commonly present in solution processed CdS [8]. On the basis of quantitative analysis of the areas under the curves, XPS suggests a slight sulfur deficiency in the films; the estimated atomic ratio was 1.1:0.9 Cd/S. This effect could result in increased conductivity of the CdS due to excess of sulfur vacancies in the crystalline structure [9].

The optimization of the printing parameters was performed next (Figure 4). Increasing the number of printed drops, from 10 to 100, results in films with increased diameter and thickness, as expected. However, lower substrate temperature results in films with larger diameter. It was not possible to measure the diameters of the films deposited at ~25 °C, because the shape was highly irregular. However, circle-shaped films were obtained for substrate temperature between 40 - 60 °C. The larger diameter for films deposited

at low temperature is likely due to the fact that the boiling point of the methanol is 65 °C. At 60 °C the solution does not have time to spread, compared with films deposited at 40 °C. Considering that the largest area to cover the channels is ~2x10^4 μm^2 for a thickness of 50 nm, to ensure homogeneous coverage and free of pin-holes, the depositions were performed 50 drops at the time on the preheated surface at 60 °C. The printed CdS resulted in dense and uniform films composed of equiaxed nanosized grains free of pin-holes and cracks (Figure 5). This is one of the main achievements of the presented technique over inkjet printed nanoparticles based films [10,11].

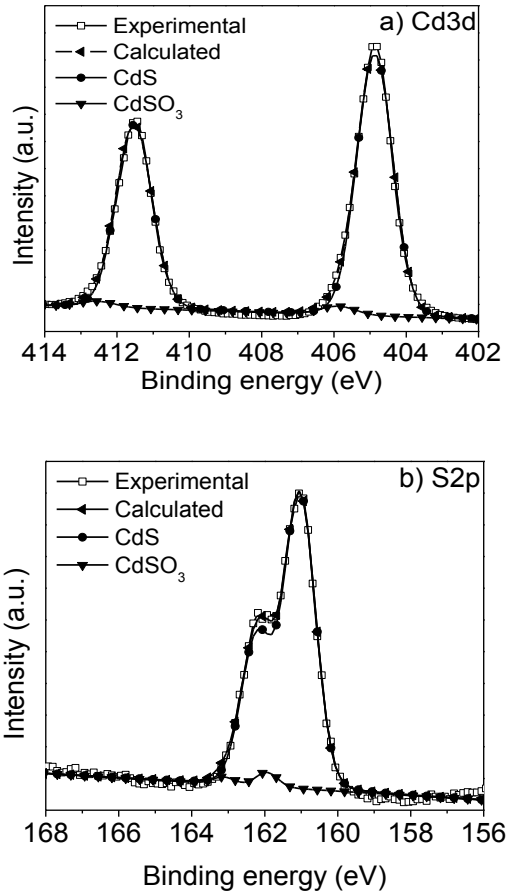

Figure 3. XPS spectra of CdS thin films. a) Cd3d and b) S2p.

The printed CdS films showed resistivities in the order of 1x10^5 Ω·cm. Figure 6a shows the transistor output curve (I_D-V_D) exhibiting characteristic n-type transistor behavior and operating in the enhancement mode. No contact resistance is observed, indicating a good interface between the CdS film and the metallic contacts. Mobility (μ_{SAT}) and threshold voltage (V_T) were determined from the slope and extrapolation of the linear fit in the $I_{DSAT}^{1/2}$ vs. V_G curve using the following equation (1):

$$I_{D\,SAT} = C_i\,(W/2L)\;\mu_{SAT}(V_G-V_T)^2 \qquad (2)$$

where C_i is the capacitance per unit area and V_G is the applied gate voltage. Extracted values were $I_{on/off}$ = 8.3x10^4, V_T = 3.4 V and μ_{SAT} = 7.5x10^{-2} cm^2/V-s, which are representative of the devices measured in the chip. This mobility is higher or in the same order compared to other solution-processed n-type organic semiconductors [12,13]. However, this mobility is lower than that obtained from CBD-deposited CdS [3]. However, in that technique, high amounts of material are wasted and just a small percentage is deposited as thin film [6]. The technique demonstrated in this work could be transferable to less expensive processes, such as roll-to-roll printing. We believe that the TFTs mobility is limited by the presence of defects in the CdS film. Some of these defects include nanocrystallites grain boundaries that could act as potential barriers, organic residue from the synthesis, etc. [14]. Higher mobility could be achieved by increasing the grain size to produce less carrier scattering and reducing potential leftover impurities [15]. Another remarkable feature of the fabricated TFTs is their low operation voltage in comparison with other organic and inorganic nanostructures based devices [16].

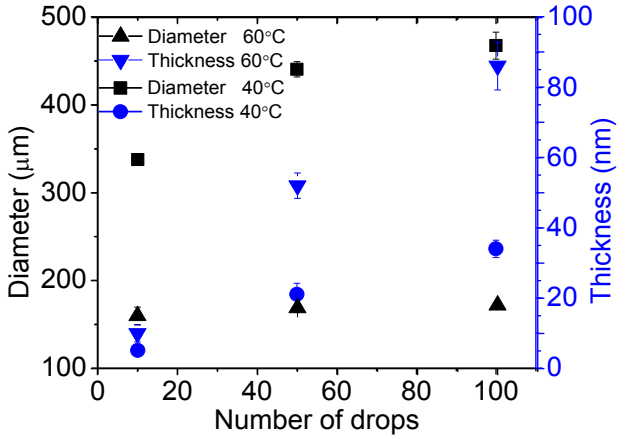

Figure 4. Variation in diameter and thickness of the thin films with the change of number of drops.

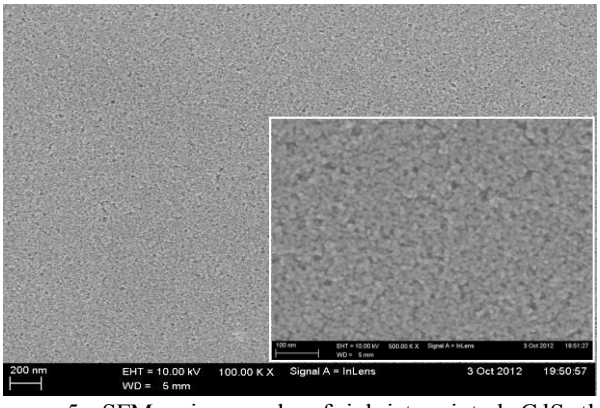

Figure 5. SEM micrograph of ink-jet printed CdS thin films. Inset, higher magnification micrograph.

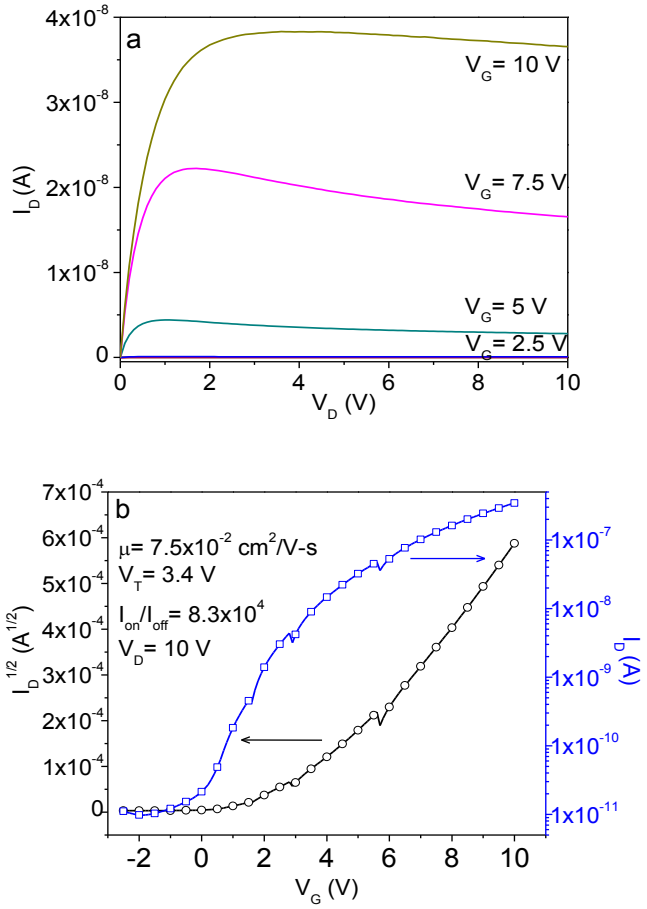

Figure 6. Current-Voltage characteristics of representative CdS printed TFTs. a) I_D-V_G curves for different gate voltages. b) I_D-V_G and $I_D^{1/2}$-V_G curves at V_D =10V.

4 CONCLUSIONS

The approach presented here demonstrates an efficient additive solution-process route to manufacture homogeneous and uniform nanocrystalline CdS thin films by printing the reagents only in the active area. It was also found that the deposition temperature affects the printed film diameter and thickness. TFTs fabricated with this method achieve mobility of 7.5x10^{-2} cm^2/V·s, V_T of 3.4 V and on/off ratio of 8.3x10^4. The process could be applied to produce many other materials and is not limited to semiconductor chalcogenides.

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