ZnO-Based Inverters for Flexible Electronics


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ABSTRACT

In this paper, we report the development of low power and low temperature zinc oxide (ZnO)-based inverters. Logic inverters were evaluated as function of gate dielectric thicknesses and several operation bias voltages. Hafnium oxide (HfO$_2$) was used as gate dielectric. The HfO$_2$ dielectric thickness was evaluated from 15 to 90 nm. TFTs and inverters show high gains (up to 150) when biased at 20 V. A low-voltage, low temperature ZnO inverter operating at V$_{DD}$= 2.5 V with gains ~20 is also demonstrated. Devices operating at V$_{DD}$= 1 V have gains ~10. This technology is a potential candidate for low-power consumption circuits for portable and low-cost applications.

Keywords: zinc oxide, thin-film transistors, logic gates, photolithography, low power electronic.

1 INTRODUCTION

Oxide semiconductors are commonly used for transparent and flexible electronic applications [1,2]. Unlike standard silicon technology, oxides are an alternative for flexible electronic applications required low temperature [3]. Oxides can also be used for transparent TETs given its wide band gap [4,5,6]. Among oxide semiconductors, ZnO is one of the most common semiconductors used for transparent applications given its compatibility with low temperature processing and band gap $>3.3$ eV. ZnO has already been used in several applications such as displays, health sensors, photodetectors and solar cells [7,8,9]. ZnO TFTs have attracted a lot of attention due to its high carrier mobility [2]. However, its use in low-power devices has been neglected for improvements. Reducing the power consumption is very important because low power allows the use of ZnO in portable electronics[10].

In this work we discuss the saturation mobility ($\mu_{SAT}$) and threshold voltage ($V_{TH}$) in terms of the applied gate voltage and HfO$_2$ thicknesses. Increasing the applied gate voltage in ZnO TFTs shows an increase in mobility. However, this change also results in higher $V_{TH}$ and $\Delta V_{TH}$. Similarly, logic inverters have larger gains and $\Delta V_{TH}$ for increased operation voltage. However, reducing the dielectric thickness allows acceptable gains with stable electrical behavior. This indicates that having the proper dielectric thickness improves the power consumption and results in devices operating at low power. The ZnO TFTs and inverters were fabricated using a maximum temperature of 100 °C and full photolithographic processes. This technology is compatible with low-power, low temperature flexible electronic applications.

2 EXPERIMENTAL

The ZnO TFTs were fabricated using a bottom gate-top contact configuration, as shown in Figure 1a. Different HfO$_2$ gate dielectric thicknesses (15, 30 and 90 nm) were used to evaluate the TFTs and inverters performance.

Fabrication was carried out on a silicon substrate with 500 nm of thermally grown SiO$_2$ on top. First, 30 nm of chrome (Cr) and 100 nm of gold (Au) were deposited by e-beam and patterned using standard photolithographic techniques. HfO$_2$ gate dielectric was deposited by atomic layer deposition (ALD) at 100 °C. Pulsed laser deposition (PLD) was used for the deposition ZnO (50nm). A KrF Excimer laser ($\lambda$=248 nm) at a frequency of 10 Hz with an energy density ~1 J/cm$^2$ was used for the PLD deposition. The distance from target-substrate was 6.5 cm. The PLD deposition chamber was evacuated to $1\times10^6$ Torr and then backfilled with O$_2$ to reach a pressure of 30 mTorr. After the ZnO deposition, a hard-mask film of parylene-C (poly-p-xylylene, 500nm) was deposited by chemical vapor deposition (CVD) at room temperature. The parylene hard-mask was patterned in an oxygen reactive ion etching (RIE) system. Then, ZnO film was selectively etched with HCl. RIE was also used to open the S-D vias. A 100 nm thick Au film was used as S-D contacts. Figure 1b shows an optical image of a
transistor and the inset shows an inverter circuit in the zero-drive configuration.

Electrical characterization was carried out with a Keithley 4200 semiconductor characterization system under dark and regular ambient conditions.

![Diagram](image)

Figure 1: a) Crosssection of the ZnO TFTs structure used in this work. b) Optical image of the completed TFT. TFT dimension are: W=160/L=20 µm. Inset in b) shows a logic inverter in a zero-drive configuration.

3 DISCUSSION

The $I_{DS}-V_{GS}$ transfer curves were measured six times. The $\Delta V_{TH}$ is calculated from the difference in $V_{TH}$ between the first and the sixth measurements. We note that after the fifth $I_{DS}-V_{GS}$ measurement the $\Delta V_{TH}$ saturates and no additional shift is detected. Figure 2a shows the final transfer curves (sixth measurement) for three different TFTs biased at 5V. The $I_{DS}$ and $I_{DS}^{1/2}$ vs. gate voltage ($V_{GS}$) are shown. $V_{TH}$ is calculated using the extrapolating of the linear fit in the $I_{DS}^{1/2}$ vs. $V_{GS}$. The $\mu_{SAT}$ is calculated with the slope of the same fit using the following equation (1).

$$I_{DS} = C_i \frac{W}{2L} \mu_{SAT} (V_{GS} - V_{TH})^2$$ (1)

Where $C_i$ is the capacitance density, $W/L$ are the channel width/length, respectively. For the TFT electrical characterization several channel dimensions ($W=160, 80$ and $20$ µm and $L=80, 40$ and $20$ µm) were evaluated. The TFTs show a decrease in the On/Off current ratio as the HfO$_2$ thickness increases and the transfer curves shift to negative voltages for thinner dielectrics. This is likely due to a reduction in the semiconductor-dielectric interface traps in thinner HfO$_2$ [11]. The calculated $V_{TH}$ increases from 3 to 4.2 V as the gate dielectric increases from 15 to 90 nm, respectively (see Figure 2b). The same trend is also observed for $\Delta V_{TH}$ (Figure 2b). The higher shift for thicker HfO$_2$ is also due to the more interface traps in thicker HfO$_2$ films. Figure 2b also shows the average mobility as function of dielectric thickness. It is clear that increasing the dielectric thickness reduces $\mu_{SAT}$ from 5.2 to 0.2 cm$^2$/V-s for 15 and 90 nm HfO$_2$, respectively when $V_{DD} = 5$ V.

![Graph](image)

Figure 2: a) Transfer curves for TFTs with different dielectric thickness (15, 30 and 90 nm). b) Average $\mu_{SAT}$, $V_{TH}$ and $\Delta V_{TH}$ extracted with $V_D = 5$ V.

To fairly compare the different devices, the electric field between the gate and source contacts was fixed at 1.66 MV/cm, which corresponds to 2.5, 5 and 15V for 15, 30 and 90 nm HfO$_2$, respectively. Figure 3a shows the transfer curves for the different HfO$_2$ thickness using these conditions ($E = 1.66$ MV/cm). The $I_{DS}^{1/2}$ vs. $V_{GS}$ curves were also used for parameter extraction ($\mu_{SAT}$, $V_{TH}$ and $\Delta V_{TH}$). Figure 3b shows that as the dielectric thickness increases the $\mu_{SAT}$ increases from 1 to 5 cm$^2$/V-s for 15 and 90 nm HfO$_2$, respectively.
However, \( V_{\text{TH}} \) and \( \Delta V_{\text{TH}} \) also increase. These results show that increasing the maximum applied voltage can improve the \( \mu_{\text{SAT}} \), but also increases the \( V_{\text{TH}} \) and the \( \Delta V_{\text{TH}} \).

Higher TFT mobilities and logic inverter gains are achieved increasing the operating voltage, but the dielectric has to be thick to manage larger operating voltage. However, thicker gate dielectric and higher voltages might lead to the creation of traps at the semiconductor-dielectric interface resulting in higher operation voltage shifts and reduced reliability. The observed reduction in operating voltage enabled with thinner HfO\(_2\) in the ZnO TFTs and inverters demonstrated in this work allows the integration of such ZnO TFTs and inverters in low power applications. In fact, inverters can operate at voltages below 2.5 V (\( V_{\text{DD}} \)), as shown in Figure 4b. Furthermore, we also characterized the ZnO-inverters fabricated with 15 and 30 nm thick dielectric and demonstrated that such devices can operate at \( V_{\text{DD}}=1 \) V with gains in the order of 10 with stable performance given the low voltage shift (~0.1 V).

![Figure 3: a) Transfer curve of TFTs with different applied voltage/dielectric thickness (2.5 V/15 nm, 5 V/30 nm and 15 V/90 nm) and b) average \( \mu_{\text{SAT}} \), \( V_{\text{TH}} \) and \( \Delta V_{\text{TH}} \).](image)

![Figure 4: a) Inverters performance for different applied voltage/dielectric thickness. Inset shows the corresponding gains. b) Average inverters gains and operation voltage shifts.](image)
4 CONCLUSIONS

The impact of dielectric thickness on the operating voltage of TFTs and inverters fabricated using standard photolithographic process and low temperature was analyzed. The complete process was carried out at a maximum temperature of 100 °C, which is compatible with transparent and flexible applications. Higher operation voltage increases $\mu_{\text{SAT}}$, $V_{\text{TH}}$ and $\Delta V_{\text{TH}}$. Inverters with gains as high as 150 for $V_{\text{DD}} = 20$ V, corresponding to a dielectric thickness of 90nm were achieved. However, inverters operating at $V_{\text{DD}} = 2.5$ V for a dielectric thickness of 15 nm were also demonstrated. Such inverters have a gain of ~10, but with very low instability. Such low-operation voltage enables the use of these devices for low-power consumption flexible electronics applications.

REFERENCES