ZnO-Based Inverters for Flexible Electronics

G. Gutierrez-Heredia*,**, I. Mejia*, M. E. Rivas-Aguilar*, F. S. Aguirre-Tostado** and M. A Quevedo-Lopez*

*Department of Materials Science and Engineering, University of Texas at Dallas, USA,
g.gutierrez@utdallas.edu, jimejia@utdallas.edu, mer095020@utdallas.edu, mquevedo@utdallas.edu
*Centro de Investigacion en Materiales Avanzados S. C. Campus Monterrey, Mexico,
gerardo.gutierrez@cimav.edu.mx, servando.aguirre@cimav.edu.mx

ABSTRACT

In this paper, we report the development of low power and low temperature zinc oxide (ZnO)-based inverters. Logic inverters were evaluated as function of gate dielectric thicknesses and several operation bias voltages. Hafnium oxide (HfO_2) was used as gate dielectric. The HfO_2 dielectric thickness was evaluated from 15 to 90 nm. TFTs carrier mobility decreases as the dielectric thickness increases for a maximum bias fixed to 5 V, while threshold voltage (V_{TH}) and threshold voltage shift (ΔV_{TH}) increases. Mobility, V_{TH} and ΔV_{TH} also have a direct correlation with applied gate voltage. Inverters fabricated show high gains (up to 150) when biased at 20 V. A low-voltage, low temperature ZnO inverter operating at V_{DD}= 2.5 V with gains ~20 is also demonstrated. Devices operating at V_{DD}= 1 V have gains ~10. This technology is a potential candidate for low-power consumption circuits for portable and low-cost applications.

Keywords: zinc oxide, thin-film transistors, logic gates, photolithography, low power electronic.

1 INTRODUCTION

Oxide semiconductors are commonly used for transparent and flexible electronic applications [1,2]. Unlike standard silicon technology, oxides are an alternative for flexible electronic applications required low temperature [3]. Oxides can also be used for transparent TFTs given its wide band gap [4,5,6]. Among oxide semiconductors, ZnO is one of the most common semiconductors used for transparent applications given its compatibility with low temperature processing and band gap >3.3 eV. ZnO has already been used in several applications such as displays, health sensors, photodetectors and solar cells [7,8,9]. ZnO TFTs have attracted a lot of attention due to its high carrier mobility [2]. However, its use in low-power devices has been neglected for improvements. Reducing the power consumption is very important because low power allows the use of ZnO in portable electronics[10].

In this work we discuss the saturation mobility (μ_{SAT}) and threshold voltage (V_{TH}) in terms of the applied gate voltage and HfO_2 thicknesses. Increasing the applied gate voltage in ZnO TFTs shows an increase in mobility. However, this change also results in higher V_{TH} and ΔV_{TH}. Similarly, logic inverters have larger gains and ΔV_{TH} for increased operation voltage. However, reducing the dielectric thickness allows acceptable gains with stable electrical behavior. This indicates that having the proper dielectric thickness improves the power consumption and results in devices operating at low power. The ZnO TFTs and inverters were fabricated using a maximum temperature of 100 ˚C and full photolithographic processes. This technology is compatible with low-power, low temperature flexible electronic applications.

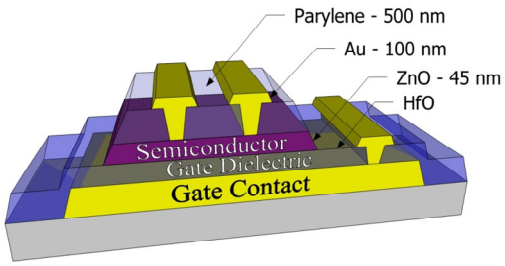
2 EXPERIMENTAL

The ZnO TFTs were fabricated using a bottom gate-top contact configuration, as shown in Figure 1a. Different HfO_2 gate dielectric thicknesses (15, 30 and 90 nm) were used to evaluate the TFTs and inverters performance.

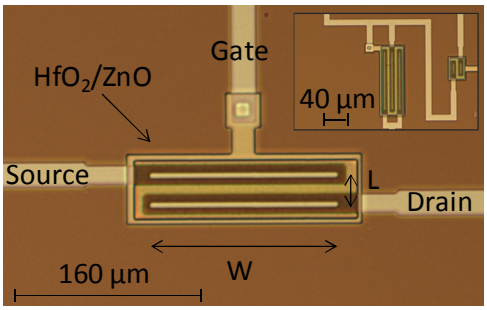
Fabrication was carried out on a silicon substrate with 500 nm of thermally grown SiO_2 on top. First, 30 nm of chrome (Cr) and 100 nm of gold (Au) were deposited by e-beam and patterned using standard photolithographic techniques. HfO_2 gate dielectric was deposited by atomic layer deposition (ALD) at 100 ˚C. Pulsed laser deposition (PLD) was used for the deposition ZnO (50nm). A KrF Excimer laser (λ=248 nm) at a frequency of 10 Hz with an energy density ~1 J/cm^2 was used for the PLD deposition. The distance from target-substrate was 6.5 cm. the PLD deposition chamber was evacuated to $1x10^{-6}$ Torr and then backfilled with O_2 to reach a pressure of 30 mTorr. After the ZnO deposition, a hard-mask film of parylene-C (poly-p-xylylene, 500nm) was deposited by chemical vapor deposition (CVD) at room temperature. The parylene hard-mask was patterned in an oxygen reactive ion etching (RIE) system. Then, ZnO film was selectively etched with HCl. RIE was also used to open the S-D vias. A 100 nm thick Au film was used as S-D contacts. Figure 1b shows an optical image of a

transistor and the inset shows an inverter circuit in the zero-drive configuration.

Electrical characterization was carried out with a Keithley 4200 semiconductor characterization system under dark and regular ambient conditions.



a)



b)

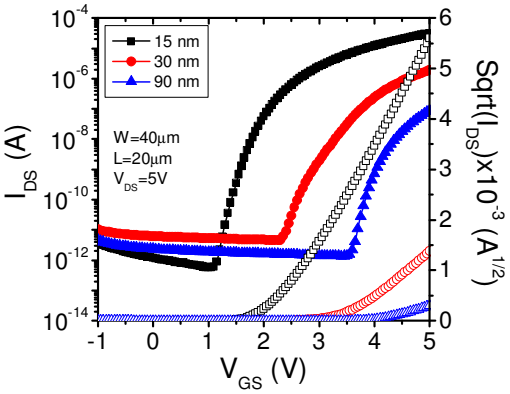
Figure 1: a) Crossection of the ZnO TFTs structure used in this work. b) Optical image of the completed TFT. TFT dimension are: W=160/L=20 µm. Inset in b) shows a logic inverter in a zero-drive configuration.

3 DISCUSSION

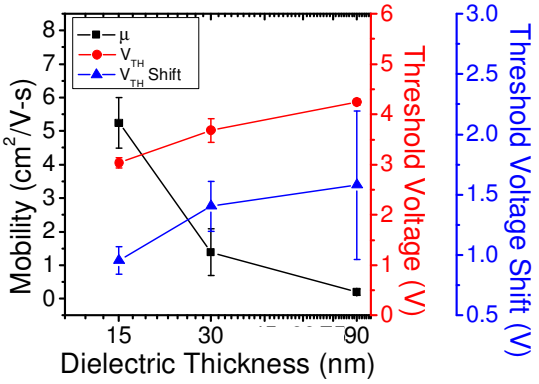
The I_{DS}-V_{GS} transfer curves were measured six times. The ΔV_{TH} is calculated from the difference in V_{TH} between the first and the sixth measurements. We note that after the fifth I_{DS}-V_{GS} measurement the ΔV_{TH} saturates and no additional shift is detected. Figure 2a shows the final transfer curves (sixth measurement) for three different TFTs biased at 5V. The I_{DS} and $I_{DS}^{1/2}$ vs. gate voltage (V_{GS}) are shown. V_{TH} is calculated using the extrapolating of the linear fit in the $I_{DS}^{1/2}$ vs. V_{GS}. The μ_{SAT} is calculated with the slope of the same fit using the following equation (1).

$$I_{DS} = C_i \frac{W}{2L} \mu_{SAT} (V_{GS} - V_{TH})^2 \quad (1)$$

Where C_i is the capacitance density, W/L are the channel width/length, respectively. For the TFT electrical characterization several channel dimensions (W=160, 80 and 20 µm and L=80, 40 and 20 µm) were evaluated. The TFTs show a decrease in the On/Off current ratio as the HfO_2 thickness increases and the transfer curves shift to negative voltages for thinner dielectrics. This is likely due to a reduction in the semiconductor-dielectric interface traps in thinner HfO_2 [11]. The calculated V_{TH} increases from 3 to 4.2 V as the gate dielectric increases from 15 to 90 nm, respectively (see Figure 2b). The same trend is also observed for ΔV_{TH} (Figure 2b). The higher shift for thicker HfO_2 is also due to the more interface traps in thicker HfO_2 films. Figure 2b also shows the average mobility as function of dielectric thickness. It is clear that increasing the dielectric thickness reduces μ_{SAT} from 5.2 to 0.2 cm^2/V-s for 15 and 90 nm HfO_2, respectively when V_{DD} = 5 V.



a)

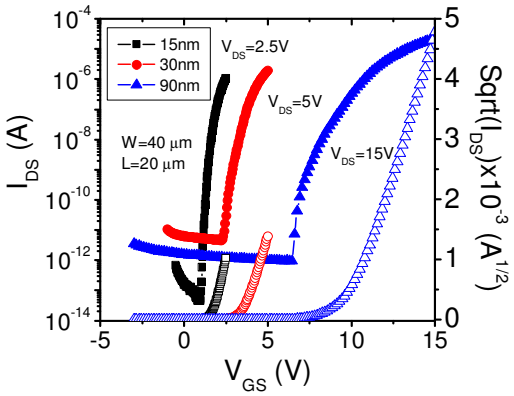


b)

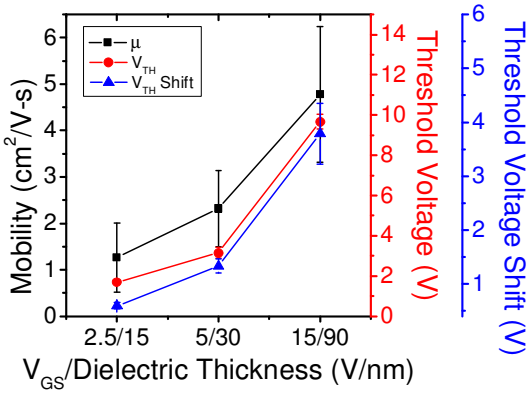
Figure 2: a) Transfer curves for TFTs with different dielectric thickness (15, 30 and 90 nm). b) Average μ_{SAT}, V_{TH} and ΔV_{TH} extracted with V_D = 5 V.

To fairly compare the different devices, the electric field between the gate and source contacts was fixed at 1.66 MV/cm, which corresponds to 2.5, 5 and 15V for 15, 30 and 90 nm HfO_2, respectively. Figure 3a shows the transfer curves for the different HfO_2 thickness using these conditions (E = 1.66 MV/cm). The $I_{DS}^{1/2}$ vs. V_{GS} curves were also used for parameter extraction (μ_{SAT}, V_{TH} and ΔV_{TH}). Figure 3b shows that as the dielectric thickness increases the μ_{SAT} increases from 1 to 5 cm^2/V-s for 15 and 90 nm HfO_2, respectively.

However, V_{TH} and ΔV_{TH} also increase. These results show that increasing the maximum applied voltage can improve the μ_{SAT}, but also increases the V_{TH} and the ΔV_{TH}.



a)

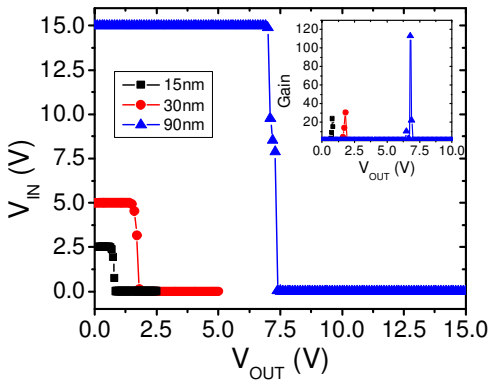


b)

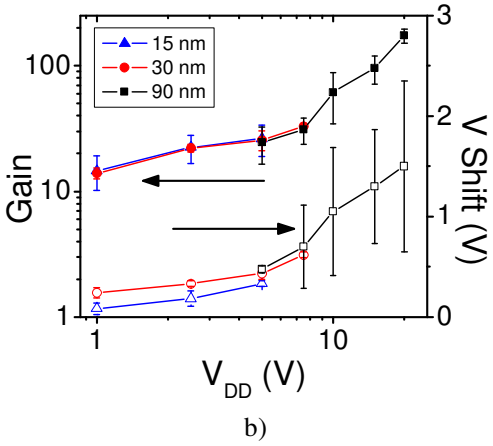
Figure 3: a) Transfer curve of TFTs with different applied voltage/dielectric thickness (2.5 V/15 nm, 5 V/30 nm and 15 V/90 nm) and b) average μ_{SAT}, V_{TH} and ΔV_{TH}.

Figure 4a shows the inverters transfer curves with different gate dielectric thicknesses using a zero-drive inverter configuration with dimensions of W/L = 40/20 for the drive transistor and 400/20 µm for load transistor. The inset in Figure 4a shows the calculated gains for these inverters. Gains were 23, 30 and 112 for 2.5 V/15 nm, 5 V/30 nm and 15 V/90 nm, respectively. The transition voltage $V_{DD}/2$ also shifts when consecutively measuring the inverter. Similarly as in the case of the TFTs, after the fifth cycle the transition voltage stabilizes and the shifting is negligible. Logic invers were tested using the same method as for TFTs with the maximum voltage applied corresponding to an electric field of 1.66 MV/cm. Figure 4b shows the inverter gains and transition voltage shift. The ZnO-inverters with 90 nm of HfO_2 were not able to operate with lower voltages (<5 V) due to the high V_{TH} required. However, inverters with thinner dielectrics (HfO_2 of 15 and 30 nm) present dielectric breakdown with the increasing voltage.

Higher TFT mobilities and logic inverter gains are achieved increasing the operating voltage, but the dielectric has to be thick to manage larger operating voltage. However, thicker gate dielectric and higher voltages might lead to the creation of traps at the semiconductor-dielectric interface resulting in higher operation voltage shifts and reduced reliability. The observed reduction in operating voltage enabled with thinner HfO_2 in the ZnO TFTs and inverters demonstrated in this work allows the integration of such ZnO TFTs and inverters in low power applications. In fact, inverts can operate at voltages below 2.5 V (V_{DD}), as shown in Figure 4b. Furthermore, we also characterized the ZnO-inverters fabricated with 15 and 30 nm thick dielectric and demonstrated that such devices can operate at V_{DD}=1 V with gains in the order of 10 with stable performance given the low voltage shift (~0.1 V).



a)



b)

Figure 4: a) Inverters performance for different applied voltage/dielectric thickness. Inset shows the corresponding gains. b) Average inverters gains and operation voltage shifts.

4 CONCLUSIONS

The impact of dielectric thickness on the operating voltage of TFTs and inverters fabricated using standard photolithographic process and low temperature was analyzed. The complete process was carried out at a maximum temperature of 100 ˚C, which is compatible with transparent and flexible applications. Higher operation voltage increases μ_{SAT}, V_{TH} and ΔV_{TH}. Inverters with gains as high as 150 for V_{DD} = 20 V, corresponding to a dielectric thickness of 90nn were achieved. However, inverters operating at V_{DD} = 2.5 V for a dielectric thickness of 15 nm were also demonstrated. Such inverters have a gain of ~10, but with very low instability. Such low-operation voltage enables the use of these devices for low-power consumption flexible electronics applications.

REFERENCES

[1] M. S. Oh, W. Choi, K. Lee, D. K. Hwang and S. Im, Appl. Phys. Lett. vol. 93, 033510, 2008.

[2] E. M. C. Fortunato, P. M. C. Barquinha, A. C. M. B. G. Pimentel, A. M. F. Martins and L. M. N. Pereira, Apl. Phys. Lett. vol. 85, no. 13, 2004.

[3] M. Grundmann, H. Frenzel, A. Lajn, M. Lorenz, F. Schein and H. von Wenckstern, Phys. Status Solidi A, 207 no. 6, 1437-1449, 2010.

[4] H. Q. Chiang, J. F. Wager, R. L. Hoffman, J. Jeong and D. A Keszler, Appl. Phys. Lett. vol. 86, 013503 2005.

[5] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano and H. Hosono, Nature, 432, 488-492, 2004.

[6] E. Fortunato, P. Barquinha, A. Pimentel, A. Gonçalves, A. Marques, L. Pereira and R. Martins, Adv. Mater. vol. 17, 5, 2005.

[7] S-H. K. Park, C-S. Hwang, M. Ryu, S. Yang, C. Byun, J. Shin, J-I. Lee, M. S. Oh and S. Im, Adv. Mater., vol. 21, 6, 678-682, 2009.

[8] C. H. Park, S. Im, J. Yun, G. H. Lee, B. H. Lee and M. M. Sung, Appl. Phys. Lett., vol. 95, 223506, 2009.

[9] W.-C. Shin, K. Remashan, J.-H.Jang, M.-S. Oh ans S-J. Park, J. Korean Phys. Soc., vol.55, 4, 1514-1518, 2009.

[10] A. P. Chandrakasan, S. Sheng and R. W. Brodersen, "Low-Power CMOS Digital Design", IEEE J. Solid-State Circuits, vol. 27, no. 4, pp. 473-484, 1992.

[11] M. McDowell, I. G. Hill, J. E. McDermontt, S. L. Bernasek and J. Schwartz, Appl. Phys. Lett., vol. 88, 073505, 2006.