Performance Comparison of Non-planar MOSFETs

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ABSTRACT

Three different non-planar MOSFETs including FinFET, and rectangular/circular gate-all-around (GAA) MOSFETs are compared based on the same electrostatic parameter-scale length. Device characteristics and intrinsic gate delay are predicted using 3-D numerical simulations. FinFET is found to have an advantage in speed though it is most sensitive to process variation on the fin width as compared with the GAA counterpart. Due to limited drive current of each GAA MOSFET, multiple wire or stack wire will be needed when performance is of concern.

Keywords: Gate-all-around (GAA), FinFET

1 INTRODUCTION

Among emerging VLSI technologies, non-planar devices such as FinFETs have been mass produced [1]-[3]. While transistors continue to shrink, short channel effects (SCEs) result in channel leakage current and hence need to be overcome in order to achieve sufficient I_{on}/I_{off} ratio. Gate-all-around (GAA) MOSFETs, which are in fact an infinite gate, provide excellent electrostatic characteristics regarding SCEs. However, it is not yet clear whether GAA can outperform FinFETs. Furthermore, unlike planar devices, the channel width cannot be arbitrarily defined and is actually quantized by the number of fins. In this work, we compare performances of non-planar MOSFETs based on same scale length and per single fin using 3-D TCAD numerical simulations [4]. Both device-level optimization and circuit-level simulation are included.

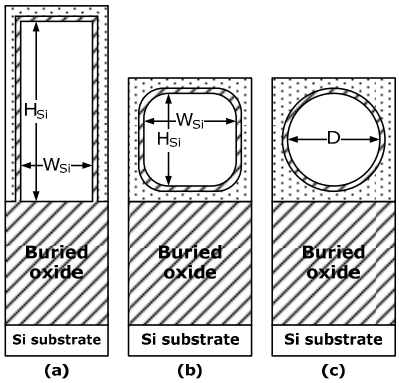

Fig. 1. 2D cross-sectional views of (a) FinFET, (b) circular GAA FET, and (c) rectangular GAA FET.

2 DEVICE DESIGN AND OPTIMIZATION

2.1. Nominal device structure

The 2D cross-sectional views of the FinFET and GAA FETs are shown in Fig. 1. Following ITRS [5] at 11.9 nm technology node, the gate work functions need to be adjusted to meet off-state leakage current ($I_{off} \leqq 100$ nA/μm for $V_{DD} = 0.68$V). The dimensions of nominal device are listed as follows: $L_g = 10$ nm, EOT = 0.62 nm, and with lightly-doped channel doping ($N_a = 10^{15}$ cm^{-3}). Dimensions of channel such as W_{Si} and H_{Si} are optimized by electrostatic scale lengths (λ) which were proposed by Yan *et al.* [6] and Suzuki *et al.* [7] for double-gate structure as follows:

$$\lambda_{Double\ gate} = \sqrt{\frac{1}{2}\frac{\epsilon_{Si}}{\epsilon_{ox}} W_{Si} + \frac{1}{8} {W_{Si}}^2} \quad (1)$$

The scale length of GAA structure was proposed by Bangsaruntip *et al.* [8] as follows:

$$\lambda_{GAA} = \frac{\lambda_{W_{Si}} + \lambda_{H_{Si}}}{\sqrt{{\lambda_{W_{Si}}}^2 + {\lambda_{H_{Si}}}^2}} \quad (2)$$

where

$$\lambda_{W_{Si}} = \sqrt{\frac{1}{2}\frac{\epsilon_{Si}}{\epsilon_{ox}} W_{Si} + \frac{1}{8} {W_{Si}}^2} \text{ and } \lambda_{H_{Si}} = \sqrt{\frac{1}{2}\frac{\epsilon_{Si}}{\epsilon_{ox}} H_{Si} + \frac{1}{8} {H_{Si}}^2}.$$

Fig. 2 shows the calculated H_{Si} versus W_{Si} plot where same λ of 3.3 nm was assumed. Based on 3D TCAD simulator [4], the Fermi-Dirac statics, drift-diffusion transport using Philips unified mobility model, and density gradient quantization model are included.

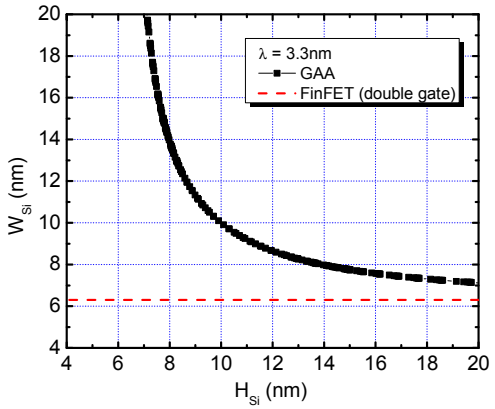

Fig. 2. Calculated H_{Si} vs. W_{Si} following the electrostatic scale lengths of GAA and double-gate MOSFETs.

2.2. DC characteristics comparison

Fig. 3 shows simulated I_{DS}-V_{GS} characteristics of different device structures using the device dimensions suggested in Fig. 2. The FinFET case shows highest I_{DLIN} and I_{DSAT}, also as indicated in Table 1. The GAA counterparts suffer severe quantum confinement and hence have less channel charge-driven currents.

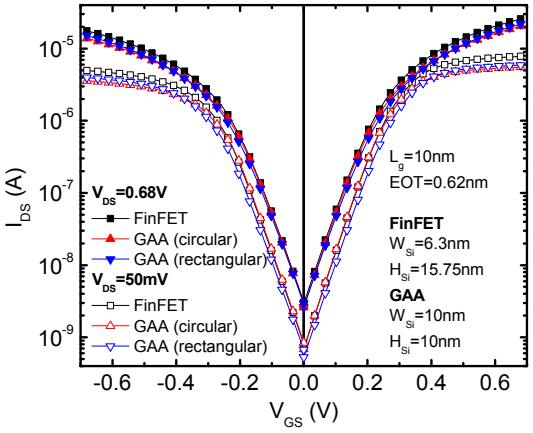

Fig. 3. I_{DS}-V_{GS} characteristics of different device structures.

Table 1. Predicted electrostatic characteristics and channel currents in different device structures.

	FinFET		GAA (rectangular)		GAA (circular)	
	nMOS	pMOS	nMOS	pMOS	nMOS	pMOS
L_g (nm)	10					
W_{Si} (nm)	6.3		10		Diameter = 10 nm	
H_{Si} (nm)	15.75		10			
Φ_m (eV)	4.39	4.88	4.41	4.86	4.38	4.89
I_{off} (nA)	2.93	3.05	2.64	2.95	2.58	2.83
I_{DSAT} (μA)	25.76	17.65	21.85	15.06	20.40	13.87
I_{DLIN} (μA)	7.79	4.96	5.90	3.96	5.33	3.57
SS (mV/dec)	80.20	83.33	83.92	87.59	79.45	83.33
DIBL (mV/V)	61.90	63.49	71.43	71.43	55.56	57.14

3 DEVICE INSIGHTS AND PERFORMANCE COMPARISON

3.1. Device scaling and sensitivity study

To gain insights into device variability, device scalability and even circuit performance, more comprehensive simulation data are presented. As shown in Fig. 4, FinFET shows the highest transconductances corresponding to aforementioned highest I_{DLIN} and I_{DSAT}.

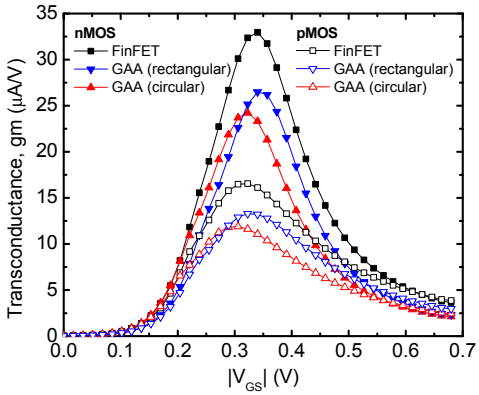

Fig. 4. Predicted transconductances for different device structures.

Regarding process variation, same W_{Si} variation was accounted for in Fig. 5. The GAA cases have better immunity to dimension variation due to better electrostatics in quad-gate control. The gate control capability could be remained by top and bottom gates when channel width is varied. On the other hand, FinFET is a double-gated device, relying on the thin channel width to maintain good gate control. Hence, FinFET is more sensitive to channel width variation. For V_{DD} scalability as shown in Fig. 6, similar impacts were predicted for all cases while I_{DLIN}'s stay almost unchanged near 0.6 V. Good supply bias scaling can be applied for low power design without degrading much performance.

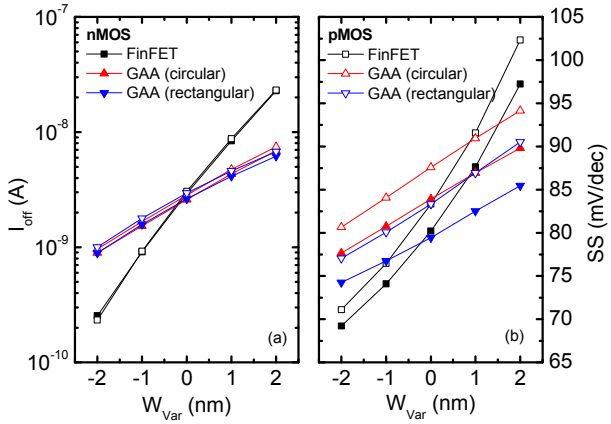

Fig. 5. Predicted (a) Ioff and (b) SS vs. W_{Si} variation.

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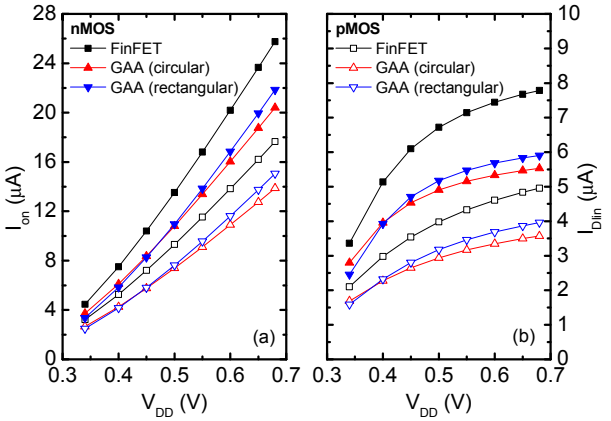

Fig. 6. Predicted (a) I_{on} and (b) I_{DLIN} vs. V_{DD} scaling.

Fig. 7 shows C_{gg}-V_{GS} characteristics in different device structures. The FinFET and rectangular GAA show higher C_{gg} due to larger effective channel width. CV/I is commonly used to predict intrinsic gate delay. Fig. 8 shows the predicted gate delay using different drive currents: I_{on} and I_{eff} [8]. FinFETs shows significantly shorter intrinsic delays due to higher drive current than others. Furthermore, the intrinsic delays of circular GAA devices are lower than rectangular ones due to lower C_{gg}.

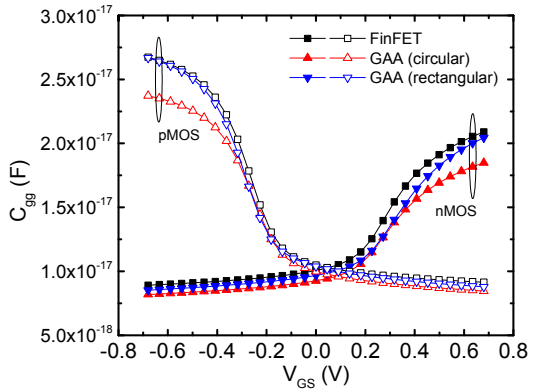

Fig. 7. Predicted C_{gg}-V_{GS} characteristics in different device structures.

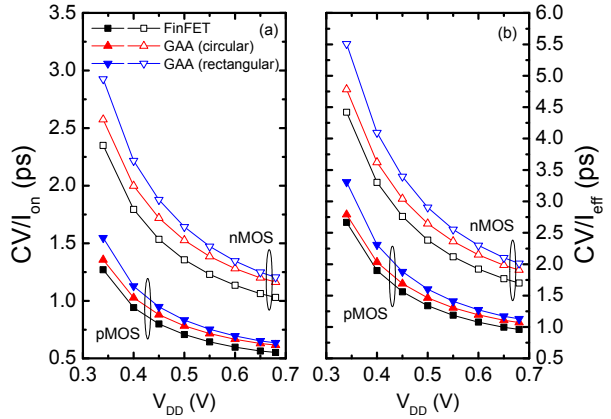

Fig. 8. Predicted CV/I_{on} and CV/I_{eff} characteristics in different device structures and supply voltages.

3.2. CMOS inverter comparison

To further compare circuit performances, mixed-mode simulations (Fig. 9) were included in our work. FinFET case outperforms GAA counterparts in inverter delay, benefited from higher drive current, as shown in Fig. 10. For speed consideration, FinFET design is suggested to be the optimal approach whereas the GAA devices provide good immunity to fin width variation. Regarding power efficiency, Fig. 11, and Fig. 12 provide more information. At a fixed supply bias, the circular GAA inverter is most efficient, as shown in Fig. 11 whereas the FinFET inverter is still the fastest design considering limited energy for mobile application, as shown in Fig. 12.

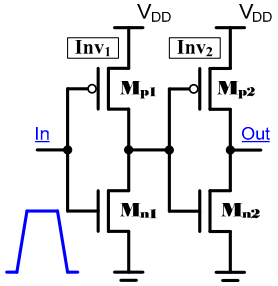

Fig. 9. Inverter schematic used for intrinsic gate delay projection.

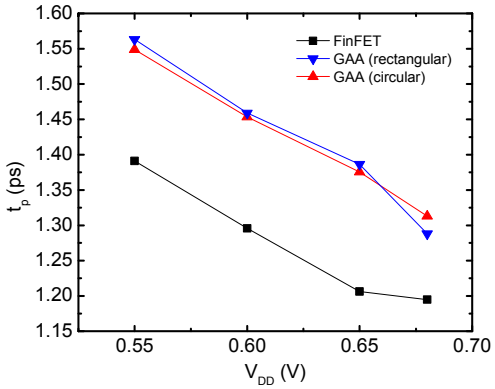

Fig. 10. Predicted gate delays in different supply voltages.

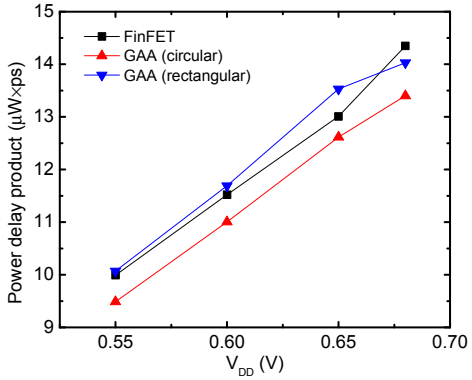

Fig. 11. Predicted power delay product in different supply voltages.

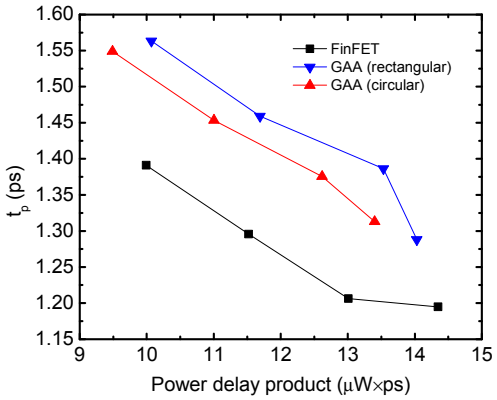

Fig. 12. Predicted gate delay vs. power delay product.

4 CONCLUSIONS

Three different non-planar MOSFETs including FinFET, and rectangular/circular GAA MOSFETs were compared. FinFET CMOS inverter gives an optimal design in speed mainly due to its high drive current though it is most sensitive to process variation on the fin width as compared with the GAA counterparts. Because of quantum-confined drive current of each GAA MOSFET, multiple wire or stack wire will be needed for high performance. However, GAA inverter was found to have an advantage in power efficiency for low power application.

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