Atomically Precise, No Interface, Device Regime Workshop

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ABSTRACT

This paper summarizes the results of the Atomically Precise, No Interface, Device Regime Workshop which was held June 7-8, 2012 at The Mansion on O Street, in Washington DC and at the National Institute of Standards and Technology (NIST) in Gaithersburg Maryland. The purpose of the workshop was to explore the possibilities for novel devices and devices with improved performance in the evolving device regime being explored by the seminal work of Michelle Simmons [1-15] and others. This new device regime creates metallic conductor, semiconductor, and insulator regions by deterministic and atomic precision placement of dopant atoms in Si[1], without metal-oxide-semiconductor interfaces. This is sometimes referred to as a no-MOS device.

Keywords: atomically precise, no interface, quantum computing, devices

1 INTRODUCTION

Recent work at the University of New South Wales in Sydney Australia in the group of Michelle Simmons has shown that it is possible to make transistors in a device regime that is dramatically different than is used for current semiconductor devices.

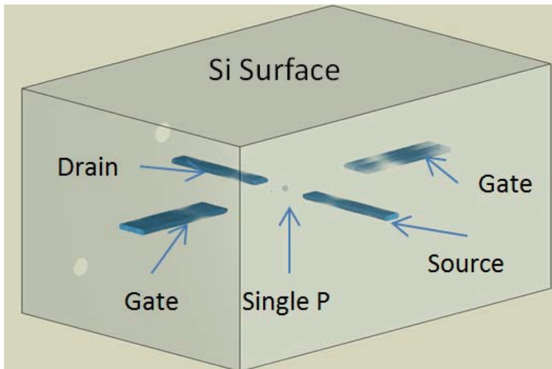

Fig. 1 No interface, single atom transistor where the device is well below the surface.

Using Scanning Tunneling Microscope (STM) lithography and dosing with phosphine, Phosphorous atoms (N-Type Dopants) can be placed by design (both number and position) in the silicon lattice. The device is overgrown with crystalline Si using Molecular Beam Epitaxy and is completely embedded in the silicon. In this way, a number of devices have been made without metal or oxide including a single atom transistor as shown in the figure. In other words this is not a Metal-Oxide-Semiconductor (MOS) device. For comparison, a schematic of a conventional MOSFET device is also shown in Fig. 2. Table 1 points to some advantages of this new no-MOS device regime that avoids some of the problems that limit conventional devices.

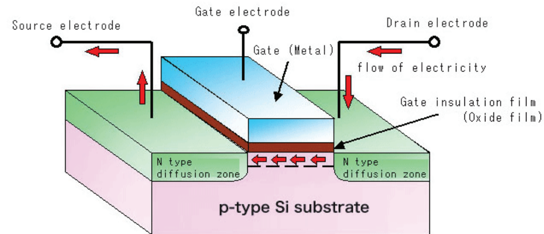

Fig. 2 Conventional MOS transistor

Feature	No-MOS	MOS
Free of surface/interface defects	✓	✗
Deterministically placed Dopant atoms	✓	✗
Atomic Precision placement of components	✓	✗
Conduction channel far away from surface	✓	✗
3D circuit architecture possible	✓	✗
Extremely low noise operation	✓	✗
Proven device technology	✗	✓

Table 1: No-MOS features compared to MOS

2 WORKSHOP GOALS

With single electron[2], quantum dot[3], and single atom transistors[4], as well as 4 atom wide nanowires[5], and extremely low noise operation[6] already demonstrated, the intention of the workshop was to gather some of the world's leading device and atomic precision fabrication experts to explore new possibilities in the quantum computing, digital, and analog device areas and the improvements and extensions of atomic resolution processes, fabrication tools, and modeling/design tools that would be required to enable these new devices. There were approximately 40 participants from 15 institutions from Australia, Canada, the U.K. and the U.S. A series of presentations were made by: Michelle Simmons - UNSW, Josh Ballard - Zyvex Labs, Lucian Livadaru - Univ. of Alberta, Gordie Shaw - NIST, Richard

Woolley- U of Nottingham, Steven Schofield - UCL, James Owen - Zyvex Labs, Carl Williams - NIST, Gerhard Klimeck - Purdue, Rajib Rahman - Sandia, Richard Silver - NIST, Frank Register - UT Austin, Malcolm Carroll - Sandia, and Ezra Bussman – Sandia. These formal presentations were followed by two breakout sessions. The first breakout session was on device implications. The second breakout session was on process and tool development priorities.

3 DEVICE POSSIBILITIES

Several classes of electronic devices were identified that could benefit from this new device regime made possible by emerging atomic resolution processing:

P in Si Quantum Computing Devices: The P in Si (and Ge) approach to quantum computing devices being pursued by the Simmons group appears to be one of the most attractive, as it is supported by existing semiconductor processing technology.

While single ion implantation for placement of individual P dopants has yielded some interesting results, the inevitable uncertainty in position due to limited spatial resolution in position of ion impact and straggle of ion trajectory after implant will simply not support the required precision in placement of the P atoms. Rahman explicitly made this point in his presentation. This leaves H depassivation lithography, phosphine dosing, and epitaxial overgrowth as the consensus approach for building P in Si quantum computing devices.

Tunneling Field Effect Transistors (TFET): In his presentation, Frank Register pointed out that TFETs have been identified as a very promising device for future technology nodes, but band tailing effects have limited the performance of these devices. With atomic precision placement of both N and P type dopants giving extremely sharp PN junctions, combined with three dimensional arrangement of gate electrodes, tunnel FETs fabricated[9,12] with these approaches should have superior performance.

Low noise analog amplifiers : Analog devices are far more sensitive to noise than digital devices. The unprecedentedly low noise demonstrated by conduction in ∂-doped P in Si devices[6] points to a major opportunity to develop analog circuitry with much better noise performance leading to enhanced dynamic range. RF amplifiers, telecommunications, low-noise, high-speed, low-power-consumption amplifiers, control circuitry for quantum computers, and analog to digital and digital to analog converters are exciting opportunities. Existing tools such as NEMO [16] could be used to design such a device.

Resonant tunneling devices with improved On/Off ratio: Previous versions of resonant tunneling devices and circuits were limited in their on/off current ratios. The greater precision in size control and placement of quantized structures available in this new regime should remove this limitation. The three dimensional placement of device elements should also have significant advantages. Circuit and device approaches previously conceived, but abandoned because of fabrication issues, could be enabled by this technology. For instance a proposal for a complex logic cell based on a resonant tunneling quantum dot architecture that proved impractical because of limitations in fabrication may be possible in the No-MOS regime[17].

Magnetic impurities: Nano magnetic devices of various sorts including spintronic devices, were of significant interest to several workshop participants. Patterning of an element such as Mn, which is used as a magnetic impurity in III-V semiconductors, and is also ferromagnetic in Si[18] could provide a route to fabrication of such devices. Another suggestion was to use three-dimensional placement of atoms to create a spiral inductor that could be used to create a localized and controllable magnetic field.

Optical devices: A number of optical devices were deemed to be of interest by taking advantage of the atomic precision size control and/or the inclusion of Er as a dopant (if possible) that could be placed with atomic precision.. A key advantage of manufacturing with atomic precision would be the integration of optical and electronic components, particularly when exploiting the properties of plasmonic behavior[19]. Not only could the atomically precise fabrication of silicon construct well defined subwavelength waveguides for focusing light, but this can also be coupled with the direct integration of suitable dopants for high sensitivity low loss devices.

Dangling bond as quantum dot devices: Both Steven Schofield and Lucian Livadaru described dangling bonds, or depassivated H atoms as quantum dots with discrete energy states. Livadaru described how these quantum dots can be used as elements in a Quantum Cellular Array (QCA) architecture as described by Lent et al.[20] at Notre Dame. The advantages of this architecture include extremely low power and extremely small devices.

Enhanced crossbar QCA and CMOL architectures: It was postulated that crossbar architectures or Likharev's CMOL architecture [21] might be realized in a much more robust form. Crossbar-like architectures suffer fundamentally in their energy balance from diode-based leakage or dark currents. Atomically precise crossbar links, possibly based on single electron charging, may offer the capability to reduce the unintended current flow.

Engineered nucleation sites for metal oxide crossbar switches: There are crossbar switch or memory devices that operate by filamentary growth in Metal Oxides. Device limitations in the variability of this material transformation are in part because the unknown nucleation of the filament growth. It was postulated that nucleation sites might be engineered by atomic precision processing and that the result would be more reliable device operation.

Single electron pumps: With superior control of dimensions and electronic states, it is suggested that single electron pumps would benefit significantly from this device regime.

Si terahertz lasers: Recently proposed [22] THz technology is based on a $2p^0$ to 1s transition in a donor atom. So far, all the experiments have used a bulk-doped sample in the low doping limit where this energy difference is fixed and only varies slightly from one donor species to another. Since the No-MOS regime enables us to create precise donor islands with controlled doping density (in the high doping regime), covalent interaction between neighboring donors will change the $2p^0$-> 1s gap. It may be possible to engineer this gap precisely, and hence to control the emitted wavelength radiation.

Medical devices: A small, low-noise, low-power set of electronics perhaps could be developed in the No-MOS regime that would be attractive for implantable medical devices or for ultrasensitive analytical devices. Another possibility is DNA sequencing nanopores. Constructing nanopores for this purpose could involve tip based atomically precise fabrication, and the integrated electrodes and sense amps could be No-MOS devices.

4 PROCESS/TOOL DEVELOPMENT PRIORITIES

The processes that enable this new device regime are all in their infancy. The following tools and processes were discussed and prioritized.

Other Substrates: Higher-mobility substrates such as Ge, graphene, GaAs would improve device performance. Silicon on Insulator (SOI) substrates reduce leakage currents into the substrate. A wide bandgap material that could be grown epitaxially on Si would give an alternative to intrinsic Si for an insulating layer, or provide modulation doping of Si. Si(111) and Si(110) are other possible substrates.

Automated SPM: The automated operation of scanning probe microscopes such as demonstrated by Richard Woolley and Zyvex Labs, has a significant opportunity to improve productivity in this new device regime.

Other dopants: An acceptor (group three) dopant would be required for a number of the device applications discussed in the workshop. For example, mixed donor-acceptor doping would provide stronger band bending, and provide deeper donor levels, desirable for higher-temperature device operation. More generally, a process for placing and maintaining the atomic precision placement of dopants including Ga, In, Al, As, Sb, Er, Mn or other magnetic species, NV centers in diamond etc. would widen the range of nano devices that could be produced in the No-MOS regime.

Other species that deposit selectively: Early on the pathway toward process development, literature searches should be done along with exploratory experimental and theoretical work to identify possible species that could be included in the toolbox for atomically precise fabrication.

More reliable tips: STM tips are notoriously variable, capricious, and a major liability when it comes to instrument productivity. Tip construction, materials, and operation are all key areas to be explored. Tiptek [23] a spin-off company from the of Univ. Illinois is developing alternative tip materials such as HfB_2 coatings for STM tips.

Registration and other processing for 3D patterning: In order to place dopant atoms with atomic precision in three dimensions, a process for aligning to previously written patterns that have been overgrown with one or more layers of epitaxial Si must be developed [14,15]. Either the ability to image previously-buried dopants, or the ability to reference a registration mark which has survived the overgrowth will be required. Obtaining nicely ordered, atomically flat Si surfaces after epitaxial overgrowth[14] would be desirable for this purpose.

Better H depassivation litho: It is clear that the lithography tools must improve if significant progress is to be made in this area. Specific areas that should be developed include: automated alignment to the Si lattice and registration markers, device design tools and rules, and field stitching.

Additionally the group expressed a desire to see one or more technical paths to scale the throughput and area that an atomically precise lithography tool could address for more advanced research and eventually manufacturing.

Contact technology for No-MOS devices: There is a need to study contacts with the devices. Is the method used by Simmons good enough? Will there be a need to move to other methods of contacting, like low T silicides [24]? If we make super-low noise No-MOS devices, we will require contacts which do not introduce high noise themselves.

Better modeling and design tools: While there are some tools, such as NEMO, which have proven valuable in modeling in this device regime, developing the device types that are mentioned above would be aided significantly by improved modeling and design tools. There is a need to bridge from the atomic scale to the mesoscopic scale.

Integration Scheme with CMOS: Carl Williams and Frank Register in their presentations, as well as a number of others in breakout session discussions, brought up the issue of integration of No-MOS devices with CMOS devices. The current high temperature processing in both device regimes makes homogeneous integration processing difficult or impossible. Flip chip or 3D packaging is a possible avenue. Some technical paths should be explored.

Selective Epitaxy: Selective epitaxial processes such as patterned Atomic Layer Epitaxy[25] (ALE) would have a number of advantages, not the least of which would be in aiding the alignment to previously defined dopant patterns. The patterned ALE process might also permit selective growth to produce better surfaces for subsequent patterning steps.

Lower temp processing: The high temperatures required to produce well-ordered Si (100) 2x1 surfaces have multiple drawbacks. Post processing of Si that already contains CMOS circuitry is excluded. Etched alignments marks must be disproportionately large to survive the high temperature processing. A surface preparation process, for example an ex-situ wet chemical etch process, that operated at much lower temperatures and resulted in well-ordered Si (100) 2x1 surfaces would be beneficial.

Deal with large screening length in Si: A current limitation in controlling the energy state of individual device elements by electrostatic interaction of gate electrodes is that the screening length of intrinsic Si is relatively long (~100nm). This makes it difficult to isolate the effect of a gate electrode to the intended device component. One potential solution would be acceptor dopants that could be strategically placed to screen the effect of the electrode to the intended device component. 3D placement of dopants would improve the ability to do this sort of screening.

Other resists: A patterned monolayer of H has proven effective for the selective deposition of P[10], Si, and Ge. However, H is not an effective mask for many potentially useful tasks such as high-quality overgrowth, because the H becomes mobile on the Si surface at 300°C and above. Other monolayer resists that are also self-developing and could be patterned with atomic precision should be explored. Self-assembled monolayer resists are also of interest.

H repassivation: One of the advantages of H depassivation lithography is the ability to examine a pattern after it is written for error correction. If there are some H atoms in the pattern which were not successfully removed, then more lithography can be used to remove the unwanted H atoms. However, for H atoms that have been unintentionally removed there is no current process to "repair" the defect by selectively repassivating the Si surface.

Large Terraces: Current sample preparation for Si (100) 2x1 surfaces produces surfaces with relatively small atomic terraces (<100nm). Work by Simmons[27] and Silver[28] have used etched features and high temperature annealing to create relatively large atomic terraces as large as 10µm. However, a process that produced large terraces with lower temperature processing would be desirable.

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