Reliable nanoscale electrical characterization using Graphene-coated Atomic Force Microscope tips

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ABSTRACT

Electrical characterization at the nanoscale is an essential procedure for analyzing the performance of many materials used at both industry and academia. In this field, one of the most powerful tools is the Conductive Atomic Force Microscope (CAFM), which can characterize the electrical properties of both conductive and thin insulating materials at areas as small as 3nm^2[1,2]. The main challenge associated with this technique is the poor reliability of the tips, which metallic varnish can wear out very fast due to high current densities and frictions when scanning the surface of the sample under test. Therefore, finding a new method to avoid fast tip wearing is essential for cheap and reliable nanoscale electrical characterization. In this work, we used a Graphene Single Layer (GSL) film to prevent premature tip wearing during conductivity measurements, and we report the first electrical characterization of nanostructured materials using a novel graphene-coated CAFM tip [3].

Keywords: nano fabrication, graphene, conductive atomic force microscopy

1 INTRODUCTION

Traditionally, metal-varnished silicon tips are commonly utilized in several fields of applications [4]. However, due to the relatively low mechanical resistance of the metallic varnish against wear out, it is likely to wear out very fast when measuring high currents and/or experiencing frictions during the sample scan. One approach among others, to overcome this drawback, is to varnish the AFM tips with a material (e. g. doped diamond) capable to preserve its intrinsic properties, such as tip radius and conductivity. Another starting point would be tips entirely made up of a conductive material – bulk tips. However, they all imply a lowered lateral resolution and high cost. Therefore, finding a new method to avoid fast tip wearing is essential for cheap and reliable nanoscale electrical characterization.

Due to its excellent mechanical, physical and electronic properties, [5] graphene (a mono-atomic layer of carbon atoms arranged in a honeycomb lattice) [6] has drawn the attention from researchers and industry, as well. In its early stages, the production of such layers was made from mechanical exfoliation of graphite and preferably used to fabricate FETs (field-effect-transistor) [7]. A much more versatile method consists to grow graphene layers by chemical vapor deposition (CVD). The advantage is, that it allows the fabrication of large-area sheets of graphene, which is a requirement for the industry [8]. Another interesting property is that, unlike epitaxial graphene, CVD-grown graphene can betransferred to arbitrary substrates [9]. This step forward, made it possible to broaden the use of graphene onto different applications [10-11].

In this work, the properties of commercially available CAFM tips are modified by coating them with CVD-grown graphene. There have been works involving similar devices, such as reported by Wen et al. [12]. The fundamental difference is that they grew multilayer-graphene directly on the AFM tip and used it as an electrode for molecular junctions. The resulting graphene-coated tip proved to be extremely stable and resistant in terms of mechanical durance and electrical characterization, such as high frictions and elevated current densities, respectively. The tips can also inhibit the sample interaction with the conductive tip coating, which is a source for false imaging.

2 EXPERIMENTAL

2.1 Sample fabrication

The transfer process is show in Figure 1a and is divided into 3 consecutive steps: Firstly, a commercially available Pt-Ir varnished AFM tip is immobilized on a piece of silicon wafer using a thin film of Poly-methyl methacrylate (PMMA) below and on it (Fig. 1). Due to its sensitivity, the tip cantilever flexes when loaded with PMMA (Fig. 1f and g). On the other hand, GSL sheets are grown on Copper, covered with PMMA, and then the Copper was etched in FeCl3 and etched with HCl and ultra-pure H2O. Then, the graphene film was picked up using the PMMA/AFM-tip/PMMA/Silicon block as the target substrate for the graphene sheet transfer. Lastly, the PMMA layers are stripped using acetone. The etching time found in this process is roughly 30 minutess, whereas in the standard transfer process only 5 minnutess are needed. This excess of time can be explained by the facts, that at one hand, the presented fabrication procedure implies to maintain the sample horizontal at all time (in order to prevent the AFM tip from falling off and most likely break), and on the other hand, 3 different layers of PMMA are used, instead of one. After having successfully concluded the stripping the cantilever flexes back to its initial positions. The described process concludes with a graphene-coated tip, which is depicted in Fig. 2b. In order to determine, whether the tip was successfully coated, the quantitative chemical composition and the physical dimensions of the tip are investigated. To carry out this analysis energy-dispersive X-ray spectroscopy (EDS) and scanning electron microscope (SEM) is used.

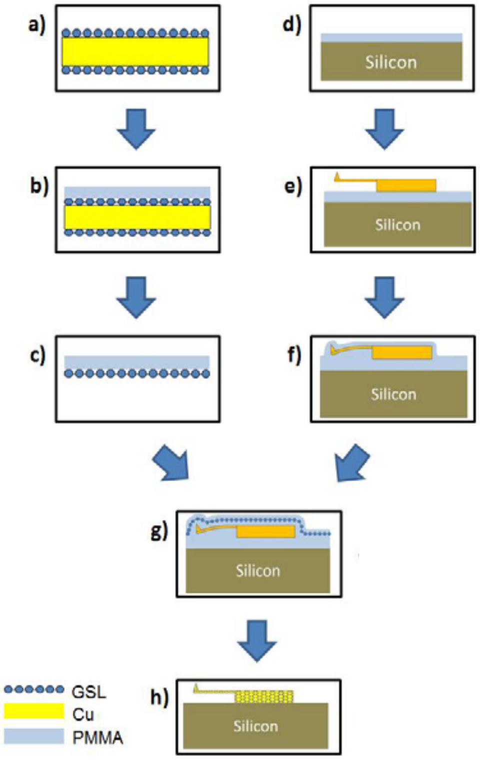

Figure 1: Schematic of the tip fabrication: (a) As-grown GSL on both sides of a Cu foil; (b) One side of the sample is covered with spin coated PMMA; (c) The bottom GSL and the Cu foil are etched; (d) A piece of Silicon is covered with spin coated PMMA; (e) The tip is attached on the sample and heated to fix the structure; (f) The AFM tip / PMMA / Si structure is again spin coated with PMMA; (g) the Graphene/PMMA stack in (c) is transferred on the tip; (h) the PMMA is removed using Acetone and maintaining the tip completely horizontal. [Lanza et al. Adv. Mater. 2013, 25, 1440–1444].

In Figure 1c it can be clearly distinguished the signal corresponding to the as-received (red line) and the graphene-coated tip (black line). Qualitatively, the main difference consists in the content of carbon, which is represented by a peak. In term of physical dimensions, the SEM images reveal no significant change by the additional graphene coating.

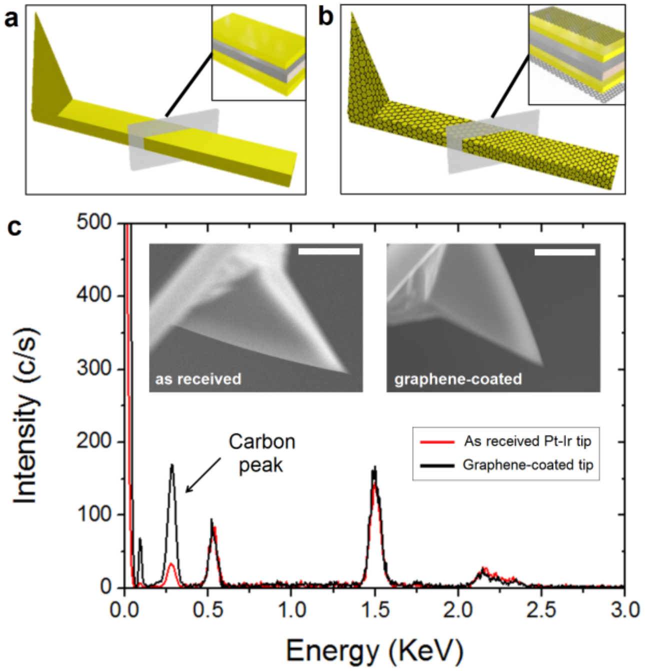

Figure 2: Schematic of an (a) as-received, and (b) graphene-coated, commercially available Pt–Ir varnished tip. The bulk of the tip consists of doped silicon (grey), which is varnished with a Pt–Ir alloy (yellow), and the graphene is highlighted with the typical hexagonal lattice. Large area SEM images of both as-received (c) and graphene-coated tips (d) show similar sizes and shapes. (e) EDS analysis of both as-received (red line) and graphene-coated (black line) tips. [Lanza et al. Adv. Mater. 2013, 25, 1440–1444].

2.2 Characterization

The performance is experimentally evaluated by characterizing two different samples: first, an HfO_2/SiO_2 stack (3nm/1nm) deposited on an n-doped Si substrate [2, 14] and were exposed to a thermal treatment in order to provoke polycrystallization. Secondly, a conductive sample was used to intentionally drive high currents through the graphene-tip arrangement. The ramped voltage stresses (RVS) and current maps were carried out using SPA3800N AFM working in high-vacuum (10^{-7} torr), which excludes the effect of the water meniscus formed between the tip and the sample in air conditions. Due to the current saturation limit of the AFM a Keithley 6430 Sub-Femtoamp Remote Sourcemeter [15] is used to significantly increase the current range. When applying ramped voltage stresses (RVSs) its excellent current/voltage configurability provides the needed functionality to carry out I–V characteristics with a very wide current dynamic range (1pA–1mA) and different current compliances (CC).

3 RESULTS AND DISCUSSION

3.1 Spectroscopic measurements

At the beginning, the HfO_2/SiO_2 stacks are characterized by spectroscopic measurements. In Fig. 3 a two sets of curves (a and b) are depicted, which show 1st, 3rd, 5th, 10th, 15th, and 20th I-V curves at different positions. Fig. 3a and 3b correspond to 20 different and randomly chosen fresh positions using an as-received and a graphene-coated tip, respectively. A significant tip wear out with increasing number of recorded I-V curves is observed in Fig. 3a. Taking into account, that the sample is very homogeneous and that each curve corresponds to a different fresh location, it can be derived that the tip loses its conductivity. As the tip is maintained static, the effect of tip-sample frictions is neglected, which means that due to high current densities ($J \approx 10^8$ A/cm^2 when it reaches the CC, which gives 100μA through an area of 100nm^2) [15] the Pt-Ir varnish of the as-received tip is worn out. In contrary, the graphene-coated tip supports several similar measurements (Fig. 3b), whose variation is attributed to intrinsic inhomogeneities of the material itself [14, 16, 17], without noticeable wear out. In order to investigate the effect of the tip wearing on the dielectric breakdown (DB) topographic maps before and after the DB event are recorded with as-received and graphene-coated tips. Fig. 3c and 3d depict the topographic maps recorded at locations, where the DB was previously induced. Comparing these two images, it can be observed, that in unstressed locations the variations in topography are similar. On the contrary, the remarkable differences can be observed at those locations where the DB event was induced. For as-received samples (Fig. 3c) the DB site corresponds to a hillock of 31.2nm in height.

This well-known behavior related to DB event in the insulating stack [18] has already been observed, where two phenomena play a major role. The first is the so-called Dielectric Breakdown Induced Epitaxy (DBIE), [19] which is related to the microstructural rearrangements triggered by DB-induced thermo-chemical reactions in the dielectric. And secondly, it has also been demonstrated that the height of the hillock is likely to be related to a high concentration of trapped charges at the conductive filament (CF) with atoms originating from the metallic varnish of the as-received tip [20]. These phenomena are especially harmful when inducing the DB with the CAFM tips [18]. The metal atoms from the tip can penetrate into the HfO_2 layer being measured. In fact, this not only an accelerated tip wearing, but also provides false electrical information. Fig. 3d reveals a completely different behavior, as no surface changes are observed it follows the topographic pattern of unstressed locations. SEM images (Fig. 3e and 3f) underline the observations, that as-received AFM experience a much higher wearing compared to tip with graphene coating.

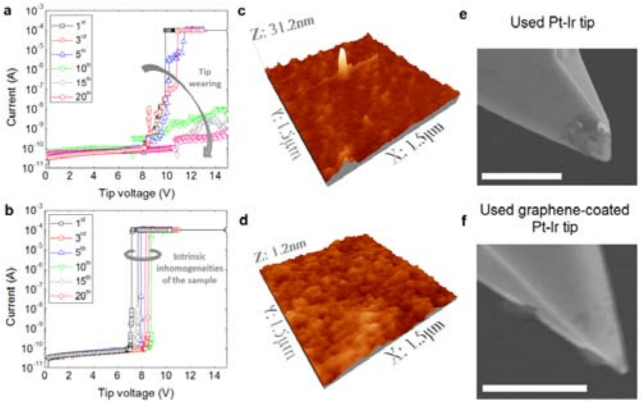

Figure 3: *I–V* curves performed on the bare surface of an HfO_2/SiO_2 stack using a) a non-coated tip, and b) a graphene-coated tip. Each graph shows the 1st, 3rd, 5th, 10th, 15th, and 20th *I–V* curve measured. All *I–V* curves were collected at fresh different locations by applying a RVS to the tip (sample substrate grounded). The typical topographic maps recorded after reaching the dielectric breakdown (DB) at the center of the scanned area using c) as-received and d) graphene-coated tips. The SEM images of e) Pt–Ir, and f) graphene-coated Pt–Ir tips, after 20 IV curves and one topographic map. The scale bars in (e) and (f) are 5μm and 3μm, respectively. [Lanza et al. Adv. Mater. 2013, 25, 1440–1444].

3.1 Electrical characterization

In order to analyze the mechanical resistance of graphene coated tips, current maps have been measured. The material under test consists of as-grown GSL on Cu stacks. The current measurements are carried out under the high-vacuum ambient conditions (below 5×10^{-7} torr) and biasing the samples to –0.1V (e. g. injecting of electrons from the substrate). Figure 4a shows the typical current maps after some measurements with as-received tips. In this case, for this tip we observe a decay of the current signal measured after measuring a total area of 6μm². On the contrary, the graphene-coated tip allows performing much more scans without observing any tip wearing. As an example, Figure 4b shows the typical current map obtained after scanning a total area of 903μm². We even applied high contact forces up to 50nN and never observed a degradation of the current signal. We also corroborated this behavior scanning $HfO_2/SiO_2/Si$ stacks. Figures 4c and 4d show the typical current scans for both tips after using them for scanning 18μm^2 and performing 20 IV curves. Again, the graphene-coated tips show much higher currents, indicating that they can preserve their intrinsic conductivity during longer times. This observations leads to the conclusion, that the graphene protects the conductive layer of the AFM tip, from frictions when being in contact with the sample under investigation. The only plausible explanation for this observation is that the graphene layer is effectively protecting the metallic tip varnish from frictions with the substrate, enhancing its lifetime. We also confirmed this behavior by recording current maps on HfO_2/SiO_2 stacks (for which obtaining reliable consecutive scans is especially difficult) [19], providing similar results (Fig. 4c and 4d).

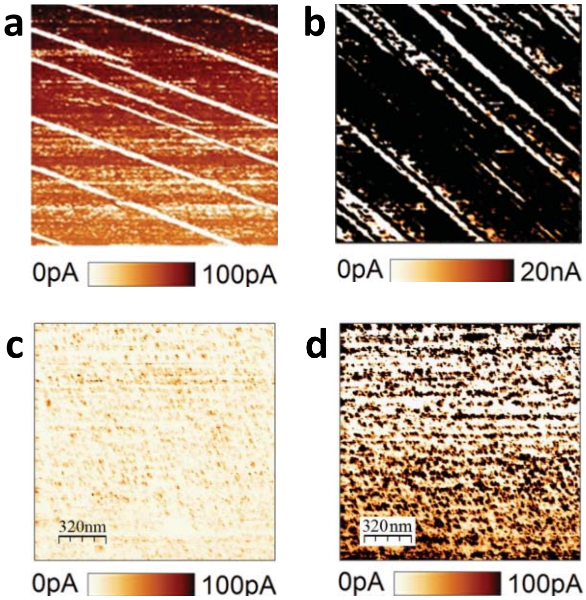

Figure 4: Current maps measured on the surface of GSL/Cu stacks recorded with as-received (a and c) and graphene-coated tips (b and d). All scans are 1µm x 1µm. (a) shows a substantial conductivity loss after 6 scans, while in contrast (b) does not show such degradation even after scanning an area 150 times larger. Current images measured on $HfO2/SiO_2$ stacks obtained with (c) PtIr and (d) graphene-coated PtIr tip. Before these images, for each tip, an area of 18 μm_2 was scanned, and 20 I-V curves until DB were performed. [Lanza et al. Adv. Mater. 2013, 25, 1440–1444].

4 CONCLUSIONS

In conclusion, conductive AFM tips for nanoscaele electrical characterization have been successfully fabricated by coating commercially available metal-varnished tips with a sheet of GSL following the standard transfer process. Graphene-coated tips are much more resistant to both high currents and frictions than commercially available metal-varnished CAFM tips, leading to much longer lifetimes and preventing false imaging due to tip–sample interaction. The novel devices can be interesting not only for reducing tip replacement costs, but also for those applications that require high stability and low tip–sample interaction (e.g., resistive switching). The patented prototype can save a lot of money to researchers that perform CAFM electrical characterization.

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