Optimized Topology of an ASIC for Thermal Analysis of Multi-Core Processors

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ABSTRACT

The main goal of the paper is to present the optimized ASIC design for the investigation of thermal-coupling among cores in multi-core processors. The detailed methodology of our approach was presented in our previous publications [1], [2]. In short, we designed a dedicated ASIC composed of regular 16x24 heat cell array that is a part of a project aimed at defining the thermal coupling coefficients between cores in multi-core architectures using a dedicated thermal-logic simulator. The power dissipation in each cell is configurable in a wide range. Therefore, it can be used to emulate the power dissipation in the units of a multi-core processor and produce the resulting temperature distribution in a chip. Due to its flexible structure, the described ASIC allows the investigation of any core topology and fabricated in modern nanometer technologies. For example, it can be used to predict the thermal behavior of 16-core processor fabricated using 16 nm process.

The technology used for the fabrication of the ASIC is 0.35 μm (high voltage). The high number of heat cells allows the emulation of up to 96 cores in the processor. Each heat cell or a group of heat cells can represent the power dissipation in processor units (floating-point ALU, integer ALU, cache L1, cache L2, etc.). The power dissipation can be regulated between 0 and 0.5 W per heat cell. The circuit configuration was described in detail in previous papers [1], [2], where the behavior of its components were also explained. Although our concept of the chip was correct, it was discovered that the temperature distribution within a cell was not quite uniform [3]. Thus, such heat cells would not emulate properly the temperature distribution in processor units. Therefore, several improvements to the chip architecture were proposed.

The advantages of this approach include the possibility of predicting thermal behavior of processors fabricated down to 8 nm technology, elaboration and validation of software thermal models and the chance of investigating dynamic temperature changes in the chip.

In order to collect experimental data, a special measurement stand was designed. It is equipped with dedicated multichannel data acquisition card and the dual cold plate cooling assembly with Peltier thermo-electric modules enabling active control of cooling conditions. It allows setting the power in each heat cell independently every 0.1 s and reading the temperature from sensors every 10 ms.

Keywords: ASIC, multi-core processor, thermal analysis

1 INTRODUCTION

Thermal analysis of integrated circuits is a crucial issue in new microprocessors with very small feature size and more than 4 cores. Some authors expect processors with dozens or even hundreds of cores to be produced soon [4]. Constantly growing the number of cores in the new microprocessors is directly connected with the growing demand of computational power. This in turn is closely connected with high power density inside the chip. The excess of the heat has to be dissipated outside the integrated circuits in order to avoid physical damage which is especially important in new technologies with high gate densities. New research shows that temperature of a core significantly rises during calculation. Due to shrinking distance between elements of modern microprocessors, an active core may influence its neighbourood. This leads to very fast overheating the chip which is critical in modern processors which are equipped with more than 8 cores. It is foreseen that in the future generations of software tools, it will be possible elaboration of smart programs that allow distribution computation over cores that are not in close proximity in order to reduce thermal coupling between active cores.

Additionally, we decided to elaborate a thermal simulator which will not suffer from the performance/ /accuracy tradeoff. Our approach allows the simulator to run a cycle-accurate execution of various applications and dynamically compute the transient temperatures in every part of the chip within reasonable time. The main novelty of the proposed approach is the use of a custom-designed dedicated ASIC, which serves a thermal emulator of a true multi-core processor.

2 ASIC DESIGN

2.1 Overview

This section briefly summarizes the idea of the proposed ASIC. It is based on the previous experience gained during design of the circuit containing overlapping matrices of 9 heat sources and 25 diode temperature sensors. The detailed description of this work can be found in [5]-[7]. The presented ASIC was designed in the 0.35 μm CMOS high-voltage technology provided by austriamicrosystems® (AMS). This chip contains an array of 384 heat cells organized in the 16×24 matrix which allows to emulate temperature distribution in multi-core chips.

2.2 Heat cell details

The heating cell structure is based on current-mode devices. It comprises two current mirrors and a modified first-generation switched-current (SI) delay cell (see figure 1). The operation rule is that the heater itself is a current mirror. An output transistor of this mirror is connected to high-voltage supply node. In order to get possibly high density of dissipated power the heater mirror is composed of NMOS transistor. All the remaining heating cell circuitry is powered by low-voltage supply. The heating mirror is driven by a PMOS transistor-based current-providing circuit based on a SI delay cell. The cell is equipped with one current input and three current outputs able to provide currents equal 1, 2 and 4 time the input current. The switchbox used for driving the current-providing cell reconnects output of the current-providing cell between the cell input and low-voltage supply node. The switchbox is driven with three CMOS logic signals, which enables activation of arbitrary sets of the cell outputs. Thus, 8 current levels can be defined, including no-flow condition. Currents coded by consecutive control bit combinations differ by constant current value. Due to mode of its operation, the current-providing cell can be referred to as a 3-bit current-mode Digital-to-Analog Converter. The input NMOS-type mirror buffers internals of the SI-based current providing circuitry from influence of external bias-current dissemination net.

There are three ways for control of power dissipated in the heater cell.

Firstly, the input bias current can be used for control of the power dissipated in the heating cell. In this case, power dissipated in all current-passing transistors of the whole heating cell changes linearly with bias current changes. This is true as long as both low- and high-voltage supply levels remain stable. The control switchbox transistors do not pass current - they are either off or connected to at least one node with no DC current path. Thus, power dissipated by the switchbox transistors can be neglected. In fact, the whole heating cell - not only the heater mirror - can be treated as a linearly bias-current controlled heating device. This property is the main reason for choosing current-based operation-mode of the complete heating cell. Linear control over the whole current flow provides linear control over all the dissipated power.

Secondly, the control switchbox logic signals provide discrete control over dissipated power. In this case only the power dissipated in whole heater mirror and in the output side of the current-providing cell changes in linearly proportional manner based on the control switchbox input signals.

Thirdly, high-voltage supply level can be changed so as to control power dissipated in the heater cell. In this case, only the power dissipated by the output side of the heater mirror changes accordingly to changes of the high-voltage supply node.

The second and third modes of control over power dissipation in the heating cell require the output heater mirror to pass possibly large current comparing to the remaining parts of the heating cell. The third presented operation mode holds linear control over dissipated power over only the output side of the output heater mirror. Thus, the mirror multiplier should be rather high, to make the output side current-flow dominate source of heat.

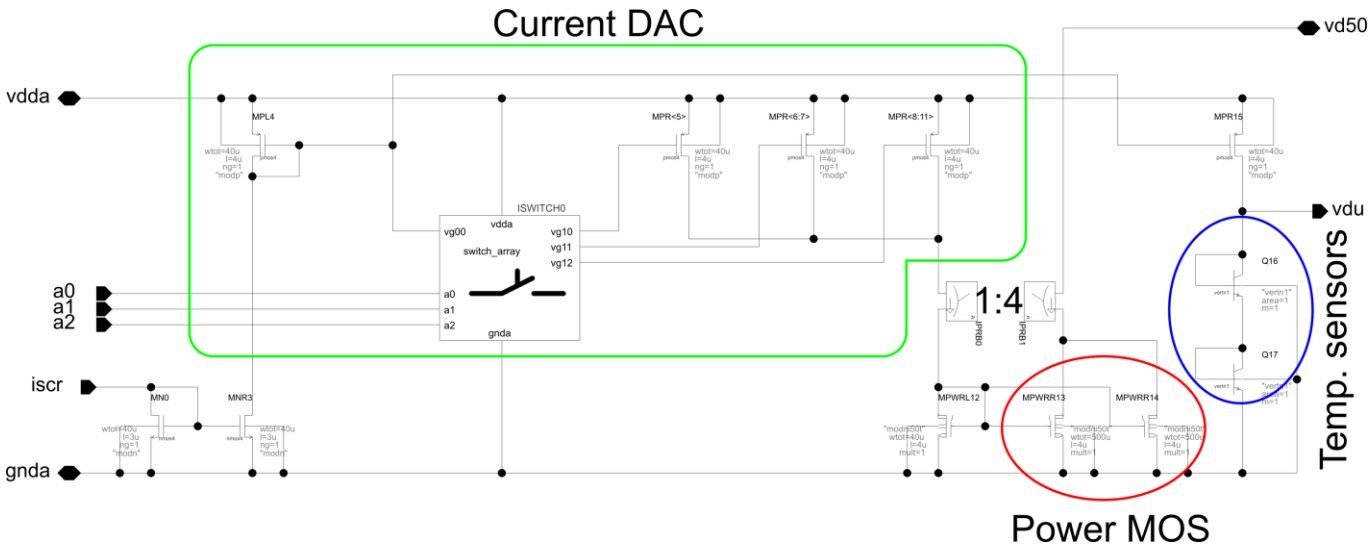

Figure 1. Electrical scheme of the power heat cell.

2.3 Optimized topology description

Although our concept of the chip was correct, it was discovered that the temperature distribution within a cell was not quite uniform [3]. Thus, such heat cells would not emulate properly the temperature distribution in processor units. Layout of the initial version of the cell is shown in figure 2. Therefore, several improvements to the chip architecture were proposed. The active heat cell area was increased from 30% in the first version of a chip to over 50% in the final version at the cost of slight decrease of linearity of the DAC included in the cell. This modification produced a much more uniform temperature distribution in a cell and in the whole chip.

The final version of a heat cell is composed of two power MOS transistors, a temperature sensor, current mirrors and some control elements. The total cell area is about 0.05 mm^2, thus the total heat cell array area is almost 20 mm^2. The power supply for power MOS transistors is equal to 50 V and 3.3 V for other elements. The high voltage for MOS transistors allows relatively high dissipated power density close to real power density of modern processors. Final cell layout is shown in figure 3, while the final layout of an ASIC is shown in figure 4.

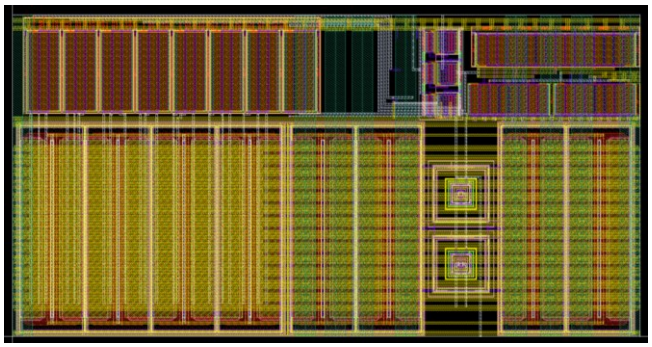

Figure 2. Layout of the first version of the power heat cell.

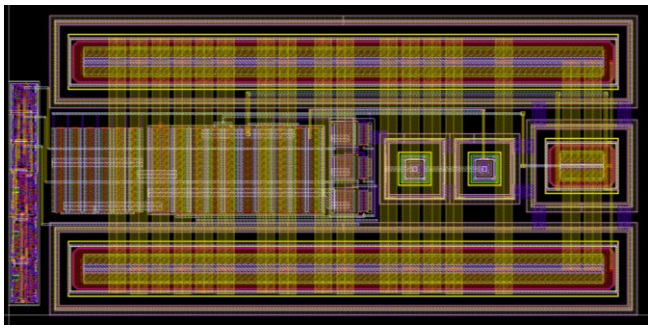

Figure 3. Layout of the final version of the power heat cell.

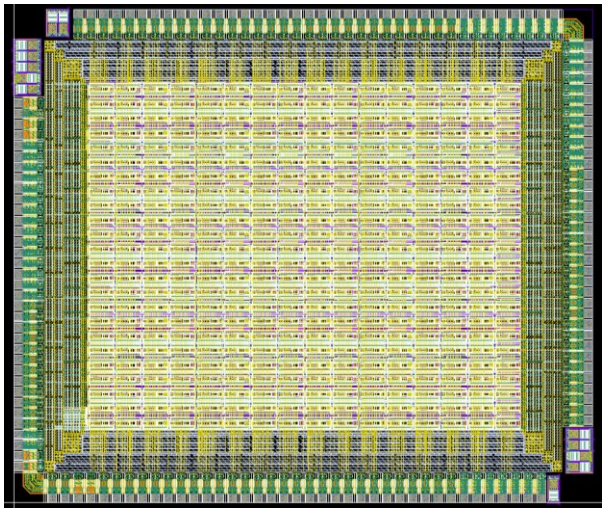

Figure 4. Layout of the ASIC.

3 SIMULATION RESULTS

We did the simulations starting from the first ASIC to the last one. The results shown in figure 5 prove that the temperature distribution is not uniform in one heat cell (first design). In single cell there are two high power MOS transistors. If both are switched on it is clearly shown a temperature drop between two peaks. The temperature drop is not acceptable for further analysis that is why we modified our heat cell. Finally, we designed a new cell when temperature distribution is more uniform. This is visible in figure 6. This modification allow obtaining the better results for temperature distribution in the chip, because it is more uniform.

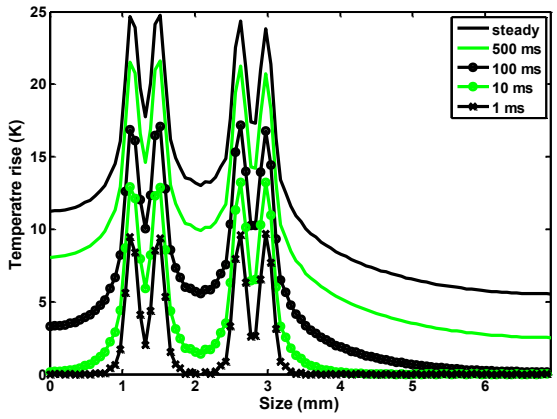

Figure 5. The temperature distribution in the single heat cell (first version of a cell).

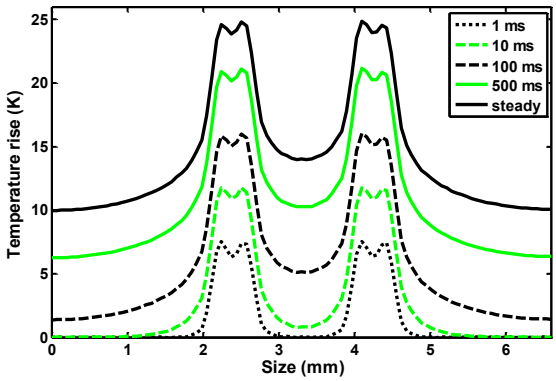

Figure 6. The temperature distribution in the single heat cell (last version of a cell).

4 CONCLUSIONS

In this paper, we described the final version of an ASIC dedicated to verifying thermal analysis of multi-core processors. Our approach is based on the use of thermal emulator – a dedicated ASIC, specially designed for this purpose. The proposed design of the analog power cell, as the most important part of the proposed ASIC, was verified using simulations using software tools delivered by Cadence®.

Furthermore, we modified existing power modelling tools to be able to simulate power dissipation in processors manufactured in the 32 nm and the 16 nm technologies and thus provide the power trace needed by the ASIC.

The limitations of our approach include: limited area resolution (due to relatively small number of heat sources) and limited power level resolution. Moreover, some physical chip parameters (e.g. die thickness) do not correspond to these of modern processors. However, in our opinion these disadvantages are significantly outweighted by the benefits.

In future, the authors consider the comparison of the results obtained with thermal emulator with those obtained using existing software thermal modelling tools. This in turn will lead to the improvement of analytical models or developing new, more accurate ones.

5 ACKNOWLEDGEMENTS

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