IN-SITU ASSESSMENT OF WAFER LEVEL HERMETICITY BY MICRO-MEMBRANE TECHNIQUE

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ABSTRACT

Vacuum packaging is required for some MEMS devices. For example, capacity diaphragm vacuum sensors, resonators in which there is no need to avoid viscous damping for high Q-factors or thermal infrared sensors in which thermal dissipation by convection should be minimized. \cite{1}

Ultra-small and low cost IR sensors are highly required for mobile applications such as hand-held and automobile camera. These kinds of low-end sensors need small array size and low cost vacuum packaging technology. Wafer-level vacuum packaging (WLVP) is indispensable to satisfy the requirement of small size and low cost IR sensors at the same time. While WLVP process consisting of solder deposition, getter activation and bonding are very well known, wafer level characterization have not been studied systematically. For the commercialization of WLVP, wafer level characterization is so important to decrease overall chip cost including WLVP process cost.

Generally, the quantitative hermeticity of WLVP has been evaluated by integration of pirani gauge vacuum senses. \cite{2-5}
But, this requires complex fabrication process and higher chip cost. In this work, hermeticity and inner vacuum value of Au/Sn eutectic bonded 8 inch wafer were calculated by analytical method through micro-membrane test.

Keywords: wafer level vacuum packaging (WLVP), eutectic bonding, hermeticity

1. DESIGN AND FABRICATION

For the wafer level vacuum package, required two wafers are cap (cavity) wafer and chip wafer. The process flows are as shown below figures, respectively.

Figure 1 shows the cap wafer manufacturing process. The cavity structure of cap wafer was etched by deep reactive ion etching (Deep RIE) method. Before the cavity formation process, the eutectic bonding metals were deposited by E-beam evaporates. The patterning of bonding metal was applied by lift-off method.

The eutectic bonding metal patterning of chip wafer was performed the same method of cap wafer as shown in figure 2.

Figure 1: Cap wafer manufacturing process

Figure 2: Chip wafer manufacturing process
Figure 3 shows the structure of eutectic bonded two wafers. Au and Sn were selected for eutectic bonding material. Eutectic temperature of Au/Sn was 280°C and the temperature of bonder pressure was set up until 320°C, because the temperature of up and down chuck pressure were made uniform. The upper chuck was pressured until 3000N for 1 hour. The bonder maker was EVGroup Company.

Figure 3: Eutectic Bonding and CMP process

After the eutectic bonding process, cap wafer was thinned by Chemical Mechanical Polisher (CMP) until 50μm thickness for the calculation of inner vacuum level as shown in figure 3. The bending deformation phenomenon of thinned membrane was evaluated the inner vacuum level. [6]

Table 1 shows the bonding layer thickness value. Cap and Chip wafer were deposited by same bond material multi-layers and thickness. Ti was adhesion layer. And Au/Sn was evaporated for uniform eutectic formation of bonding layer.

<table>
<thead>
<tr>
<th>THK. (nm)</th>
<th>Top (Cap wafer)</th>
<th>Bottom (Chip Wafer)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ti</td>
<td>50nm</td>
<td>50nm</td>
</tr>
<tr>
<td>Au</td>
<td>20nm</td>
<td>20nm</td>
</tr>
<tr>
<td>Sn</td>
<td>200nm</td>
<td>200nm</td>
</tr>
<tr>
<td>Au</td>
<td>300nm</td>
<td>300nm</td>
</tr>
<tr>
<td>Sn</td>
<td>250nm</td>
<td>250nm</td>
</tr>
<tr>
<td>Au</td>
<td>200nm</td>
<td>200nm</td>
</tr>
</tbody>
</table>

Table 1: Bonding layer thickness value

Figure 4 shows a SEM image of the cross-section of bonded metal layer. A void or delamination phenomenon was not observed by SEM.

Figure 4: SEM image of a bonded metal layer

And after membrane thinning by 60um membrane thickness, Deformation was appeared in wafer, as shown in figure.5. This deformation is considered that inner cavity was vacuum condition. But the precise vacuum level can not evaluate this condition but evaluate the hermeticity. So. For the evaluation of Precise vacuum level, this deformation was calculated the profile by surface profiler of Dektak.

Figure 5: Photo image of wafer

Figure 6 shows the max value of deformation profile. The result was about 1.6um deformation under flat zone. This means vacuum level condition. Figure 7 shows SEM image of the cross-section of membrane structure. The thickness of membrane and the cavity depth were confirmed about 61.5μm thickness and 58.5μm depth, respectively.
2. RESULT AND DISCUSSION

The correlation of membrane thickness, membrane deformation and inner vacuum parameter was shown in figure 8.

All the values of inner vacuum in any membrane thickness were saturated under 200torr. This means that low vacuum level is more accurate than high vacuum level. From the equation 1, we can confirm the inner vacuum value is 635torr at the membrane thickness of 60um, as shown in figure 9.

\[
\omega_0 = \frac{1}{66} \frac{a_m^4 (1 - v_m^2)}{d_m^3} \frac{E_m}{\Delta p}
\]

\( \omega_0 \): Membrane Thickness
\( E_m \): Young’s modulus
\( v_m \): Poisson’s ratio

3. CONCLUSIONS

A distinction of well-sealed MEMS sensor applied WLVP will be evaluated from this work. The yield of above 80% in 8 inch wafer was obtained by analytical method.

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REFERENCES


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