Metal-Oxide-Semiconductor Structures with Two and Three-Region Gate Dielectric Containing Silicon Nanocrystals: Structural, Infrared and Electrical Properties


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ABSTRACT

Two types of MOS structures, c-Si/SiO$_x$/Al and c-Si/SiO$_x$/SiO$_2$/Al (x = 1.15 and 1.3) were prepared by thermal evaporation of silicon monoxide with thickness of ~ 100 nm on Si substrate or on thermal oxide. The effect of the annealing conditions on the gate dielectric properties was studied by TEM, FTIR and I-V measurements. Cross-sectional TEM revealed that a two-step annealing process at 1000 °C, first in N$_2$ and then in N$_2$+O$_2$ atmosphere leads to formation of two regions in the SiO$_2$ layer: a homogeneous amorphous region, free of nanocrystals close to the top surface and a region with nanocrystals underneath it. FTIR and electrical measurements showed that the top region is with properties close to that of stoichiometric SiO$_2$.

Keywords: Si nanocrystals, MOS, TEM, FTIR, I-V

1 INTRODUCTION

The use of electrically isolated charge storage nodes instead of a conventional floating gate leads to several important advantages, especially for devices operating in radiation environment. Examples are non-volatile memories with enhanced radiation hardness and dosimeters for ionizing radiation [1-3]. Usually, nanocrystal MOS devices employ a gate dielectric consisting of three layers: thermal SiO$_2$, SiO$_x$ containing silicon nanocrystals and top SiO$_2$. The top oxide can be deposited by one of the following techniques: Chemical Vapor Deposition (CVD) [4], Physical Vapor Deposition (PVD) [5] or Plasma Enhanced CVD (PECVD) [6]. For radiation tolerant devices the top oxide quality is of critical importance. It is well known that the quality of oxide films deposited by CVD, PVD or PECVD in general is inferior compared to that of thermal silicon oxide. Here we present results for nanocrystal MOS structures in which the top SiO$_2$ is formed by thermal oxidation of silicon-rich SiO$_x$ films. The oxidation is part of a high temperature process, usually used only for phase separation and formation of Si nanocrystals.

2 EXPERIMENTAL DETAILS

Two groups of Metal-Oxide-Semiconductor (MOS) structures were prepared, with and without separately produced thin thermal SiO$_2$ between the film with nanocrystals and the Si wafer. The structures were produced on n-type (100) c-Si wafers with resistivity of 4-6 Ω cm. The thermal oxide was grown in dry O$_2$ atmosphere at 1000 °C for 5 minutes. SiO$_x$ films with thickness of ~ 100 nm and initial compositions of x = 1.15 and 1.3 were deposited on the thermal oxide or on the Si substrate by thermal evaporation of silicon monoxide under vacuum of 1 × 10$^{-3}$ Pa. The sample thicknesses are appropriate for application in ionizing radiation dosimeters.

Two types of high temperature processes were used, annealing in N$_2$ and annealing/oxidation in N$_2$/N$_2$+O$_2$ atmospheres, both at 1000 °C for 60 min. Previous results [5,7] have shown that annealing of SiO$_x$ films with x = 1.15 and 1.3 in N$_2$ for 60 min at 1000 °C leads to phase separation and formation of silicon nanocrystals (Si NCs) in an amorphous matrix. The two-step N$_2$/N$_2$+O$_2$ process used here was: first, annealing in N$_2$ and then oxidation in 90% N$_2$ + 10% O$_2$ ambient in order to obtain a region free of nanocrystals close to the top SiO$_2$ surface [8,9]. The depth to which the SiO$_2$ film was intentionally oxidized was controlled by varying the N$_2$ and N$_2$+O$_2$ annealing times. Control samples annealed for stabilization at 250 °C for 30 min in Ar were also prepared.

After the annealing Al metallization was carried out through a mask and MOS capacitors with area of ~ 2 × 10$^{-3}$ cm$^2$ were formed. Aluminum was also used as a back contact to the crystalline silicon. The structures were characterized electrically by Current-Voltage (I-V) measurements using Agilent B1500A Semiconductor Device Analyzer.

Structures without metallization were kept for structural and infrared characterization. Transmission Electron Microscopy (TEM) analysis was performed using a Jeol 2010 microscope operating at 200 kV. Samples for cross-sectional view micrographs were produced by gluing two samples film to film and then cutting vertical sections which were ground and milled to electron transparency.
Infrared spectra were measured by Perkin Elmer Spectrum One FTIR spectrometer.

3 RESULTS AND DISCUSSION

3.1 Transmission Electron Microscopy

Figure 1 (a), (b) shows cross-sectional TEM micrographs of SiO$_x$ films with thickness of ~ 100 nm after high temperature treatment with annealing/oxidation times of 45/15 and 40/20 min, respectively. In Fig. 1 (a) the SiO$_x$ film is on crystalline Si wafer (two-region dielectric) and is with a composition of $x = 1.3$, while in Fig. 1 (b) it is on thermal SiO$_2$ (three-region dielectric) and is with $x = 1.15$. In both micrographs the top SiO$_2$ region formed by the second annealing step is clearly visible. The thermal oxide can also be clearly distinguished in Fig. 1 (b).

![TEM image](image1.png)

Fig. 1. Cross-sectional TEM images of annealed/oxidized samples for 45/15 min (a) and 40/20 min (b) at 1000 °C. The SiO$_x$ film is with a composition of 1.3 (a) and 1.15 (b).

The two samples exhibit silicon nanoclusters seen as dark spots randomly distributed in an amorphous matrix. High resolution TEM (HR TEM) image of a single dark spot (not shown here) reveals a crystal structure of the cluster. The averaged nanocrystal size estimated from HR TEM is ~ 3-5 and 4-6 nm for films with $x = 1.3$ and 1.15, respectively. Previous studies [5,10] have shown that the host matrix obtained after 60 min annealing at 1000 °C in N$_2$ is stoichiometric SiO$_2$. The thicknesses of the homogeneous amorphous regions free of nanocrystals, close to the top surfaces in Fig. 1 (a) and (b) are approximately 25 and 20 nm. The smaller thickness of the top oxide region in Fig. 1 (b) is related to the larger amount of excess Si in the SiO$_{1.15}$ matrix. Therefore the N$_2$/N$_2$+O$_2$ annealing leads to formation of a top homogeneous amorphous region, free of nanocrystals and a nanocrystal region (SiO$_2$-Si NCs) underneath it.

Similar results were obtained on films with shorter oxidation times (in the range 5 - 15 min), however the resulting thickness of the top oxide was smaller.

Under 60 min N$_2$ annealing the SiO$_x$ films exhibit nanocrystals all along the film thickness except for a thin (~ 5 nm) region close to the top surface. Most likely the NCs at distances < 5 nm get transformed into SiO$_2$ due to native oxide formation after exposure to air.

3.2 Infrared Spectroscopy

Figure 2 (a), (b) presents Fourier Transformed Infrared (FTIR) spectra of thermal SiO$_2$/SiO$_x$ samples with $x = 1.15$ and 1.3.

![FTIR spectra](image2.png)

Fig. 2. FTIR spectra of a control, N$_2$ and N$_2$/N$_2$+O$_2$ annealed samples with $x = 1.15$ (a) and 1.3 (b).
The control sample spectrum in Fig. 2 (a) exhibits a wide absorption band in the 920-1160 cm$^{-1}$ range with two minima at ~ 985 and 1096 cm$^{-1}$. Such broadening of the characteristic band of the Si–O–Si stretching vibration mode, which is at ~1080 cm$^{-1}$ for stoichiometric SiO$_2$ [11,12] and reduction of the peak amplitude is typical for SiO$_x$ films with x < 2 [13]. The IR spectrum of the SiO$_{1.3}$ control sample (Fig. 2 (b)) has a similar shape but with one minimum. Both types of high temperature annealing, in N$_2$ and N$_2$/N$_2$+O$_2$ atmospheres, have similar effect on the IR spectra shown in Fig. 2 (a) and (b); a decrease of the band width, a “blue” shift of the peak and an increase of its amplitude are observed. In Fig. 2 (a) the full width at the half maximum (FWHM) of the N$_2$ and N$_2$/N$_2$+O$_2$ annealed films in Fig. 2 (a) is ~86 cm$^{-1}$, in Fig. 2 (b) FWHM is ~85 cm$^{-1}$, both values are close to that of stoichiometric SiO$_2$, ~ 85 cm$^{-1}$ [13]. The position of the minimum of both, SiO$_{1.5}$ and SiO$_{1.3}$ films, shifts to that of thermal SiO$_2$, ~1086 cm$^{-1}$ [11]. All these results indicate that the oxide matrix obtained after the high temperature annealing of SiO$_x$ (x = 1.15, 1.3), in which the nanocrystals are embedded, as well as the top region formed by the second (oxidation) step have composition close to the stoichiometric SiO$_2$, in agreement with our previous findings in [5,7].

3.3 Current-Voltage Measurements

Figure 3 (a), (b) shows current-voltage dependencies of MOS capacitors with SiO$_{1.15}$ and thermal SiO$_2$/SiO$_{1.15}$ gate dielectrics, respectively. The exponential increase of the current through the control sample with SiO$_{1.15}$ dielectric (Fig. 3 (a)) begins at ~± 6 V; the average electric field obtained using ~100 nm for the film thickness is $E_{av} = ±0.6$ MV/cm. The observed asymmetry in the I-V characteristics indicates that the current is controlled by the injecting interface, c-Si wafer /SiO$_2$ at positive and Al/SiO$_2$ interface at negative gate voltage (V$_{g}$). The high temperature annealing in N$_2$ does not change substantially the voltages at which the exponential current increases through the Al/SiO$_2$-Si NCs/Si structure begins (Fig. 3 (a)). The change of the slope at V$_g < 0$, which corresponds to electron injection from the Si wafer, can be related to an increase of the roughness of the c-Si wafer/dielectric interface after SiO$_2$ annealing at 1000 °C [5,14]. However, the two-step annealing/oxidation process shifts the I-V characteristics to higher positive/lower negative voltages, i.e. to electric fields with higher absolute value $|E|$; larger oxidation time results in larger $|E|$. For example, a 10 min oxidation time shifts the beginning of the exponential increase to approximately + 10 and ~ 20 V, i.e. to $E = ±1$ MV/cm and ~ 2 MV/cm. After 20 min oxidation the corresponding electric fields are ~ +1.3 and ~2.5 MV/cm. The obtained I-V data for the two-step annealed Al/SiO$_2$/Si structure are in agreement with the TEM results showing formation of two-region SiO$_2$-Si NCs/SiO$_2$ gate dielectric (Fig. 1 (a)) and indicate a high quality of the top SiO$_2$ region.

The beginning of the exponential current increase in all Al/SiO$_2$/SiO$_{1.15}$/Si capacitors is at higher electric fields (Fig. 3 (b)) when compared to the corresponding Al/SiO$_{1.15}$/Si structures. For the control, N$_2$ and N$_2$/N$_2$+O$_2$ annealed samples the exponential part begins at average electric field of ~ 2, 1.6 and 2.5 MV/cm for positive voltage and at approximately ~2, ~1.9 and ~2.9 MV/cm for negative voltage. Taking into account that the main part of the voltage drop is in the silicon oxide, which has a thickness of ~ 20 nm in the control and N$_2$ samples and of ~ 40 nm in the three-region N$_2$/N$_2$+O$_2$ sample the calculated electric fields at which the exponential increase begins are higher than the value for Fowler-Nordheim injection in SiO$_2$. The slope of the I-V curves of the N$_2$ and N$_2$/N$_2$+O$_2$ annealed Al/SiO$_2$/SiO$_{1.15}$/Si samples is higher than the slope of the control structure (Fig. 3 (b)). This can be related to transformation of the SiO$_x$ matrix to stoichiometric oxide with embedded Si NCs and reduction of the trap density. In addition, the two-step annealing reduces the small current flowing at lower voltages from ~ 350 pA in the control and N$_2$ samples to less than 100 pA.

**Fig. 3.** I-V dependencies of a control and annealed samples with SiO$_{1.15}$ (a) and thermal SiO$_2$/SiO$_{1.15}$/Si gate dielectrics.

4 CONCLUSIONS

Si/SiO$_2$/Al and Si/SiO$_2$/SiO$_2$/Al MOS structures have been prepared by thermal evaporation of silicon monoxide with thickness of ~ 100 nm and initial compositions of x = 1.15 and 1.3 on Si substrate or on thermal oxide. The effect of two high temperature processes on the gate dielectric properties has been studied. The first process is
annealing in N\textsubscript{2}, while the second one is annealing/oxidation in N\textsubscript{2}/N\textsubscript{2}+O\textsubscript{2} atmosphere, both at 1000 °C for 60 min. TEM data showed formation of two regions in the SiO\textsubscript{x} layer under the N\textsubscript{2}/N\textsubscript{2}+O\textsubscript{2} annealing: a homogeneous amorphous region, free of nanocrystals close to the top surface and a region with nanocrystals underneath it. The IR results indicate that the matrix containing nanocrystals as well as the top homogeneous region are with composition close to that of stoichiometric SiO\textsubscript{2}. The I-V measurements revealed good insulating properties of the top oxide region.

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