Modeling and Fabrication of Quantum Dot Channel Field Effect Transistors Incorporating Quantum Dot Gate

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ABSTRACT

Quantum dot gate (QDG) field-effect transistors (FET) have shown three-state transfer characteristics. Quantum dot channel (QDC) field-effect transistors (FET) have exhibited four-state I_D-V_G characteristics. This project aims at studying the effect of incorporating cladded quantum dot layers in the gate region of QDC-FET. Four-state characteristics are explained by carrier transport in narrow energy mini-bands which are manifested in a quantum dot superlattice (QDSL) channel. QDSL is formed by an array of cladded quantum dots (such as SiOx-Si and GeOx-Ge). Multi-state FETs are needed in multi-valued logic (MVL) that can reduce the number of gates and transistors in digital circuits. The fabricated device showed the four-state characteristic (OFF, 'I_1', 'I_2', ON).

Keywords: quantum dot, field-effect transistor, mini-band, superlattice, multi-valued logic

1 INTRODUCTION

The construction of Quantum Dot Channel (QDC) with Quantum Dot Gate (QDG) Field- Effect Transistor (QDC-QDG-FET) using silicon quantum dot layers was reported in 2011 [1]. The structure of the QDC-QDG-FET using silicon quantum dots is shown in Figure 1. The channel consists of two layers of silicon quantum dots (SiO_x-cladded Si) which were site-specifically self-assembled [2]. In order to isolate the inversion channel from the gate, the dry oxidation was conducted on the top layer of the bottom set of silicon quantum dot layer. The gate consists of two layers of silicon quantum dots which were also site-specifically self-assembled.

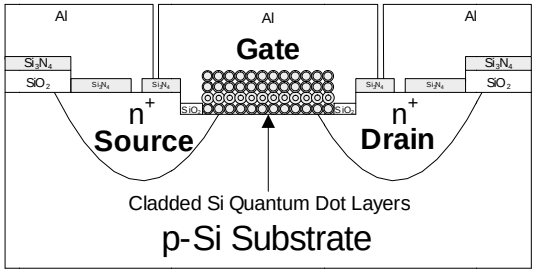

Figure 1: QDC-QDG-FET using Silicon Quantum Dots

1.1 I_D-V_G Characteristics

The published I_D-V_G characteristics are shown in Figure 2 [3]. One significant I_D current peak is observed at the V_G voltage equal to approximately 1.7 volts when V_D is equal to 1 volt. Two significant I_D current peaks are observed at the V_G voltages equal to approximately 1.6 and 2.1 volts when V_D is equal to 1.5 volts. The results corresponded to the four-state characteristic (OFF, 'I_1', 'I_2', ON).

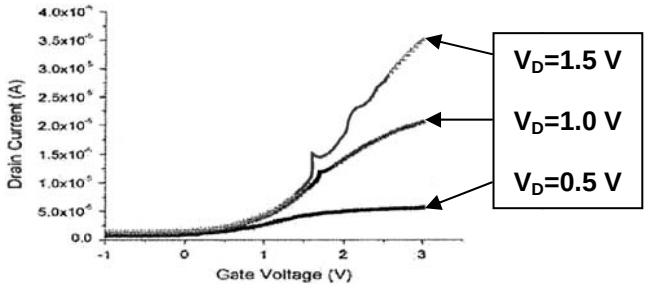

Figure 2: I_D-V_G Characteristics of the QDC-QDG-FET using Silicon Quantum Dots

1.2 I_D-V_D Characteristics

The published I_D-V_D Characteristics of QDC-QDG-FET using silicon quantum dot is shown in Figure 3 [3]. There are three I_D current groups in Figure 3. The first group consisted of V_G equal to 1.2, 1.3, 1.4 and 1.5 volts. The second group consists of V_G equal to 1.6 volts. The third group consists of V_G equal to 1.7, 1.8, 1.9 volts. The current line of V_G equal to 1.6 volts is almost straight, and extends between the first group and the third group.

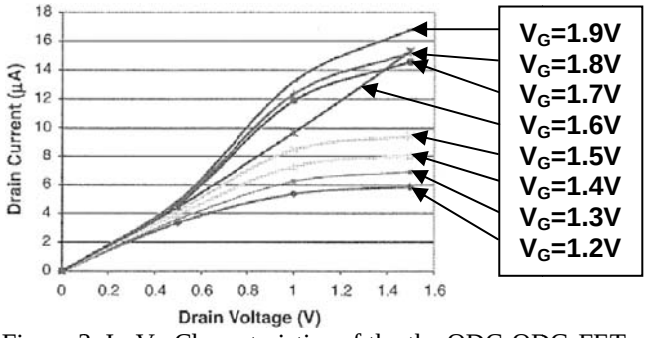

Figure 3: I_D-V_D Characteristics of the the QDC-QDG-FET using Silicon Quantum Dots

2 THEORY

In order to determine approximate locations and widths of the energy mini-bands in the quantum dot super lattice (QDSL), the well-known Kronig and Penney model was used [3]. Energy mini-band levels and widths for silicon quantum dot superlattice (QDSL) in the conduction band are shown in Figure 4. In the 4nm core diameter silicon quantum dot, the first, second and third energy levels locate at 0.102, 0.408 and 0.911eV, and the upper and lower energy limits are also shown above and below the center energy levels [3]. The first, second and third energy band widths are 0.07, 0.14 and 0.21eV [3].

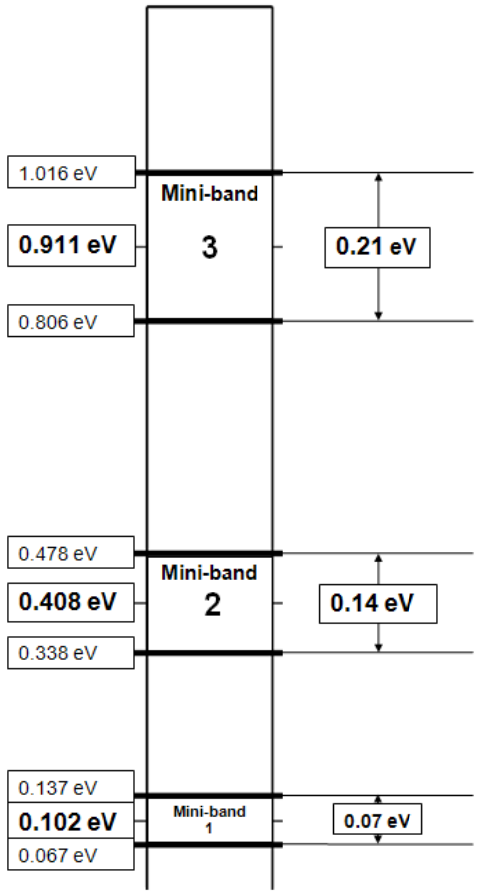

Figure 4: Energy Mini-band Levels and Widths for Silicon Quantum Dot Superlattice (QDSL)

2.1 Diagram across Horizontal Axis

The relationship between the V_D and locations of electrons is explained sequentially in Figure 5 [3]. (a) There is no V_D, and none of the mini-bands are under the Fermi level. (b) V_D is applied, and Mini-band 1 is under the Fermi level. So electrons start filling Mini-band 1. (c) Additional V_D is applied, and Mini-band 2 is under the Fermi level. So electrons start filling Mini-band 2. (d) Additional V_D is applied, and Mini-band 3 is under the Fermi level. So electrons start filling Mini-band 3.

2.2 Diagram across Vertical Axis

Electrons are moving from the source to the drain through minibands. But this electron path is shifted to the miniband in the next quantum dot well by applying V_G, and the I_D shows a jump during this shift. Figure 6 shows that the electron path is shifted from the first miniband in the first well to the first miniband in the second well by applying V_G [3]. It also shows that electrons are transferred from the first mini-band to the second mini-band in the first well by applying V_D [3].

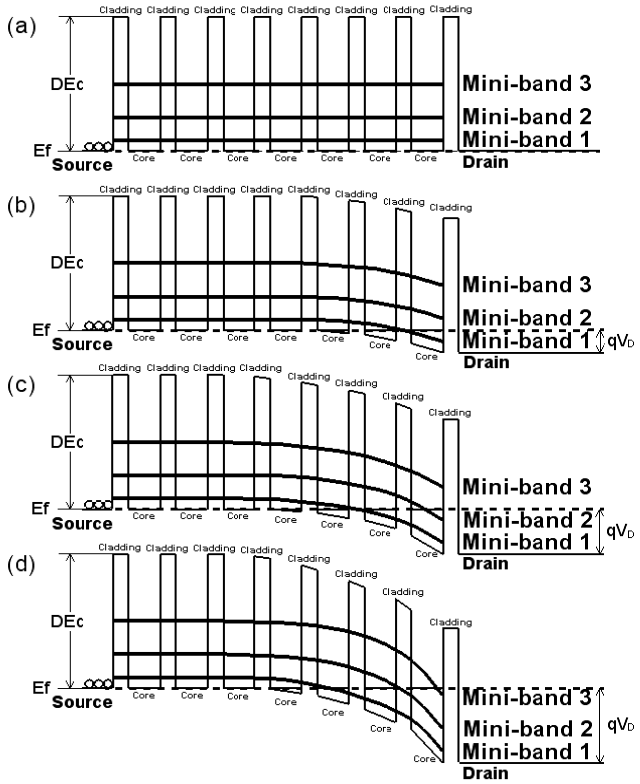

Figure 5: QDC-QDG-FET: Energy Band Diagram across Horizontal Axis

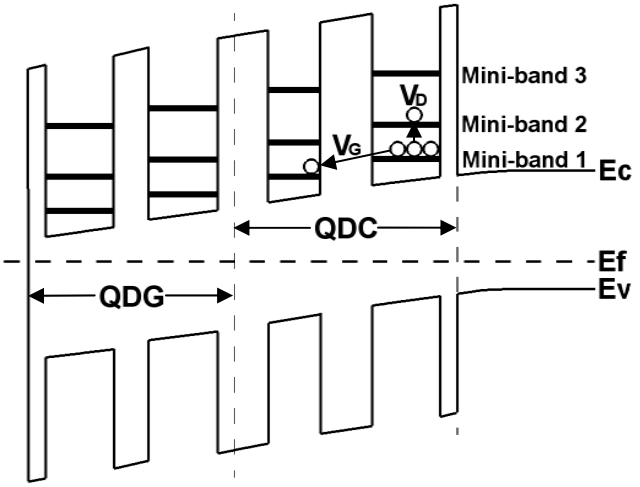

Figure 6: QDC-QDG-FET: Energy Band Diagram across Vertical Axis

3 FABRICATION

The QDC-QDG-FET was fabricated by the lithography involved in applications of four masks. They are the souce and drain mask, the gate mask, the contact mask and the interconnect mask. The source and drain Mask was used to fabricate the source and the drain. The gate mask was used to open the gate. The contact mask was used to fabricate the source and the drain contact holes. The interconnect mask was used to interconnect terminals of the source, the drain and the gate. The geometrical relationship between these four masks is shown in Figure 7. The fabrication procedures are summarized as follows [3];

3.1 Creating a recessed region under the gate

The 1250Å wet oxidation was conducted on a silicon wafer. The source and drain mask was used to fabricate source and drain windows. The phosphorus diffusion was conducted on the sample to establish the n-type source and the n-type drain in the p-type silicon substrate. A 75Å silicon nitride layer was deposited on the sample using the Plasma Enhanced Chemical Vapor Deposition (PECVD). The gate mask was used to eliminate the 1250Å oxide layer and the 75 Å silicon nitride layer above the gate region. The 250Å Dry Oxidation was conducted, and the gate mask was used to eliminate this 250Å oxide layer above the gate region to establish the 125Å depth well for two layers of silicon quantum dots.

3.2 Depositing two layers of cladded Si dots using the site-specific self-assembly

The sample was immersed into the silicon dot solution for 3 minutes for the self-assembly [2]. Then it was annealed at 750°C in Argon for 10 minutes.

3.3 Forming the gate insulator

The sample was dry oxidized at 800°C in Oxygen for 5 minutes to enhance the cladding layer thickness of deposited cladded silicon quantum dots.

3.4 Forming the gate

The second set of silicon quantum dot layers was self-assembled on the first set of quantum dot layers [2], and annealed at 750°C in Argon for 10 minutes.

3.5 Metalizing gate, source and drain contacts

The contact mask was used to partially eliminate the 75 Å silicon nitride layer to establish the electrical contact between the metal and the source, also between the metal and the drain. The 2000Å aluminum was deposited on the sample to establish source, drain and gate contacts using the high vacuum evaporator.

3.6 Pattering interconnects

The interconnect Mask was used to separate the aluminum layer to isolate source, drain and gate contacts.

4 RESULTS

The fabricated four devices are shown in Figure 8. The lower right device is the FET which showed the characteristics of QDC-QDG-FET. The left terminal is the source, the center terminal is the gate, and the right terminal is the drain. The gate length, the gate width and gate area are 60μm, 60μm and 3600μm^2.

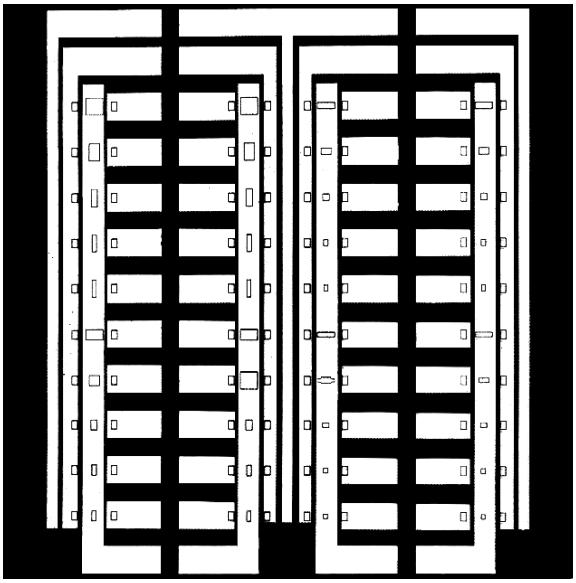

Figure 7: Geometrical Relationship between Four Masks

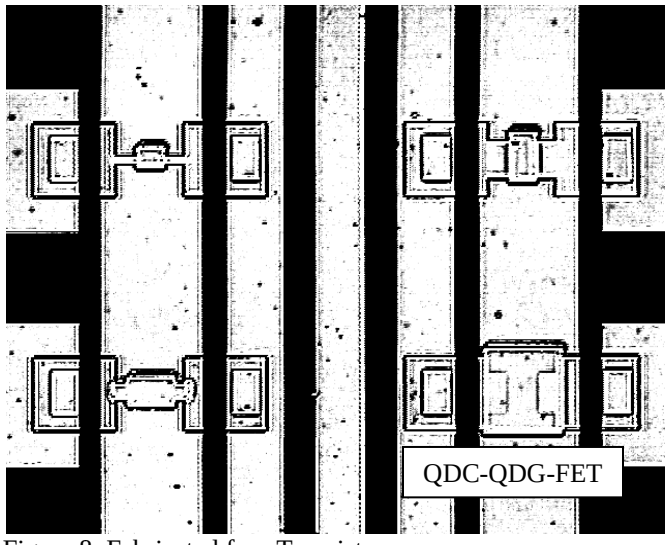

Figure 8: Fabricated four Transistors

4.1 I_D-V_G Characteristics

Figure 9 shows the I_D-V_G characteristics of the fabricated QDC-QDG-FET, and V_D of 0.5 and 1.5 volts were used. When V_D was equal to 0.5 volts, one I_D current peak was observed at 0.20 volts V_G. This I_D current peak is labeled as 1A. When V_D was raised to 1.5 volts, three I_D peaks were observed at -0.45 volts, -0.20 volts and 0.55 volts V_G (the upper left inset shows the enlarged view of the first and second peaks when V_D was equal to 1.5 volts). These three peaks are labeled as 1B, 2B and 3B. This phenomenon corresponded to the four-state characteristic (OFF, 'I_1', 'I_2', ON). V_D voltage values, peak I_D current values and corresponding V_G voltage values are shown in Table 1. As seen in Figure 9 and Table 1, I_D current peaks did not occurred at the identical V_G voltage for V_D voltages of 0.5 volts and 1.5 volts.

4.2 I_D-V_D Characteristics

The I_D-V_D characteristics of the QDC-QDG-FET are shown in from Figure 10. Seven different V_G voltages were used to measure the I_D-V_D characteristics. These V_G voltages are 0.5, 0.7, 0.9, 1.1. 1.3, 1.5 and 1.7 volts. The I_D current lines of V_G voltages of more than 0.5 volts form one group, and the I_D current line of the V_G voltage of 0.5 volts is isolated from the previous I_D current group.

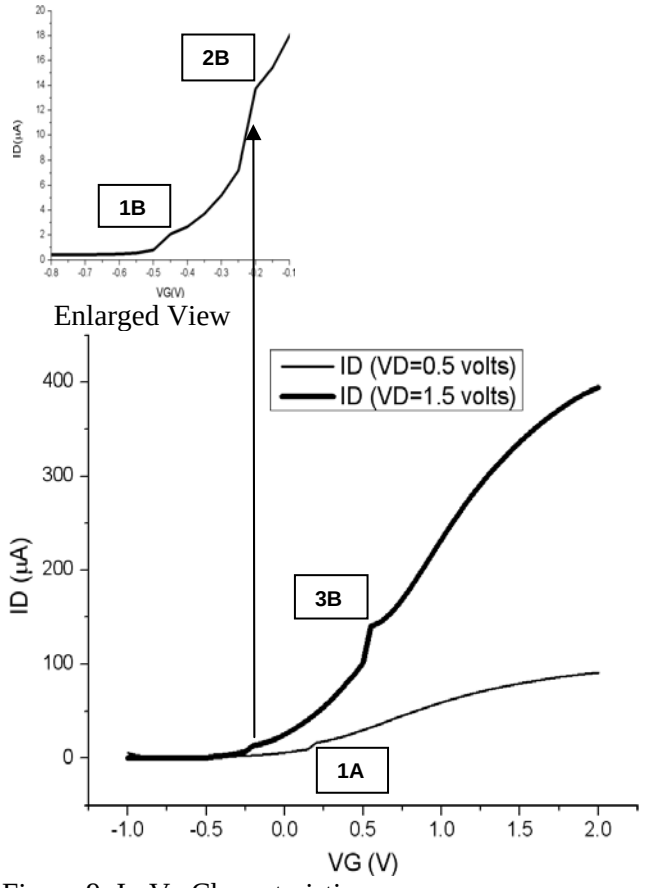

Figure 9: I_D-V_G Characteristics

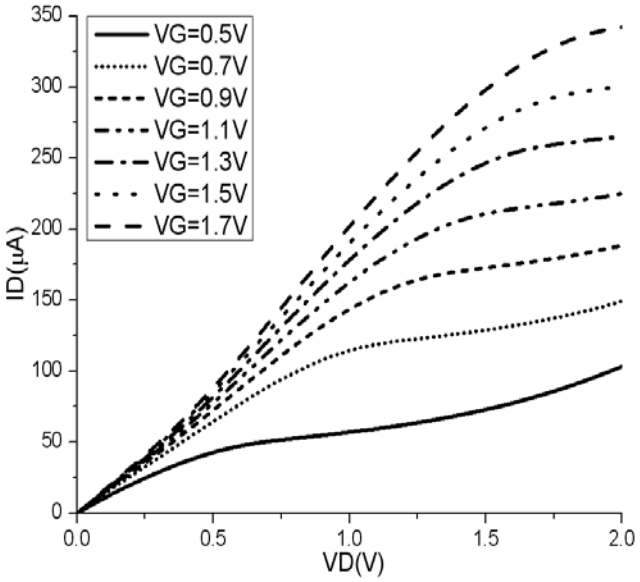

Figure 10: I_D-V_D Characteristics

V_D (V)	I_D (μA)	V_G (V)
0.5	16.555	0.20 V
1.5	140.80	0.55 V
1.5	13.745	-0.20 V
1.5	2.0835	-0.45 V

Table 1: V_D Voltage, I_D Current and V_G Voltage

5 CONCLUSION

The much higher current flow was obtained from this QDC-QDG-FET than the previous QDC-QDG-FET fabricated in 2011. One I_D current peak was observed at 0.20 volts V_G when V_D was equal to 0.5 volts. Three I_D peaks were observed at -0.45 volts, -0.2 volts and 0.55 volts V_G when V_D was 1.5 volts. This phenomenon corresponds to the four-state characteristic (OFF, 'I_1', 'I_2', ON), and this was the very first time when three current peaks were observed from the QDC-QDG-FET. Multi-state FETs are used for the multi-valued logic (MVL) which can reduce the number of gates and transistors in digital circuits [4].

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