A model to describe the hump-like feature observed in the accumulation branch of CV-characteristics of MOS capacitors with oxide-hosted Si nanoparticles

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ABSTRACT

We numerically examined electrical properties of MOS capacitors with oxide-hosted Si nanoparticles, including their frequency-dependent CV- and static IV-characteristics. A model developed for the description of such characteristics implies that charge carriers tunnel through oxide along linear nanoparticle chains in which tunnel barriers are scattered in terms of their width, so that the widest tunneling gap presents a 'bottleneck' for the tunneling charge. Using the simplest example of MOS capacitor with a planar array of oxide-embedded Si nanoparticles and monopolar injection of holes from the accumulation layer of p-type semiconductor into oxide, we explain the formation of a hump-like feature that was previously observed in the accumulation branch of CV-curves of such MOS capacitors. Numerical calculations of typical MOS capacitors are reported, and an example of experimentally measured characteristics closely resembling the curves predicted by the model is given.

Keywords: oxide-hosted Si nanoparticles, tunneling transport, MOS capacitors, CV-characteristics, double-barier structure.

1 INTRODUCTION

It is a well-known fact that the density of foreign nanoinclusions in dielectrics can be made high enough to facilitate tunneling transport of charge carriers over the system of dielectric-embedded particles. The latter is used, for instance, if one wants to organize efficient electroluminescence in film structures with dielectric-embedded Si nanoparticles. In such cases, transport of charge carriers over the nanoparticle system proceeds over rather short times, and it can therefore exert an influence on measured electrical characteristics of structures involving dielectrics with hosted Si nanoparticles, for instance, CV-characteristics of MOS capacitors, right during electrical measurements. Indeed, there are many communications stating that, in their accumulation branch, CV-characteristics of MOS capacitors with oxide-hosted Si nanoparticles often exhibit a hump-like feature emerging as a single capacitance peak or a more intricately shaped structure [1-4]. Within this feature, growing in amplitude with decreasing the measurement frequency ω, measured MOS capacitance C can be notably in excess of the accumulation capacitance C_a of a similar ideal MOS capacitor (without oxide-hosted nanoparticles). The hump emerges within a certain interval of gate voltages U, this interval being preceded by a portion of CV-curve exhibiting a capacitance value close to C_a. With increasing the voltage U, measured MOS capacitance C first increases to reach some maximum value, and then it decreases to finally reach saturation at a lower capacitance level (also close to C_a). Measurements of C within the hump were reported to be poorly reproducible, seriously suffering from hysteresis phenomena.

Previously, trying to clarify the formation of the hump-like feature of interest, we have attempted examination of a simple transport model for charge carriers injected into the MOS oxide layer with hosted Si nanoparticles [5]. In the present work we give a detailed analysis of this model as applied to the simple case of a double-barrier structure formed by a planar array of Si nanoparticles embedded in an MOS oxide layer. Interestingly, the analysis allows one to gain a better insight into the electrical properties of dielectrics with arbitrarily arranged nanoparticle systems.

Generally, the model arises on adoption of the following assumptions: (i) in a biased MOS capacitor, tunneling injection of charge carriers (electrons and/or holes) from one or both contacts into the MOS oxide with embedded Si nanoparticles takes place (for definiteness, below we consider the case of MOS capacitors formed on p-type Si substrates; in such capacitors, holes are assumed to be injected from the accumulation layer of p-Si into oxide-hosted Si nanoparticles, which in turn are assumed to be nanocrystals (nc's), to subsequently sink to the metal (see Fig. 1)); (ii) the hole transport through the oxide layer proceeds along linear nc chains in a self-consistent manner with the establishment of local electric field in the oxide; (iii) in the nc chains, tunnel barriers are statistically scattered in terms of their widths, so that the widest tunneling gap presents a 'bottleneck' for the hole current. In an nc chain, the involvement of a "bottleneck' promotes accumulation of a positive charge Q_{ox} in the oxide, which, as calculations show, is concentrated predominantly at the edge of the bottleneck from the side of the injecting contact. It is the small a.c. variations of Q_{ox} that lead to the increase of measured capacitance C in excess of C_a.

The way the above model can be arrived at can be outlined as follows. It is clear that the hump feature arises in the CV-curves of MOS capacitors due to the charge accumulated in the oxide layer. It can be therefore anticipated that the effect due to recharging of nanocrystals

will be manifested in the CV-curves of MOS capacitors the brighter the greater is the charge Q_{ox} accumulated in the oxide due to hole injection (see Fig. 1); here, we also assume that, ordinarily, the alternating component of Q_{ox} should vary in proportion to the steady-state component of the oxide charge. Suppose that the contact injection of charge carriers (hole injection out of the *p*-Si substrate) provides for some value of the local density of holes p in the immediate vicinity of the injecting contact. Further evolution of p along the coordinate x normal to MOS and directed from the injecting contact into the oxide layer is governed by the continuity equation for the hole current $j_p=qp\mu_{eff}E$: $div(j_p)=0$ (here, μ_{eff} is the effective mobility of holes in the oxide, defined by the rate of tunneling processes (i.e., by the widths of the tunneling gaps). Since the field E increases in the direction from semiconductor (S) to metal (M), a profound density of holes p deep in the oxide layer can be accumulated on the condition that $grad(\mu)<0$. The latter condition refers to a situation in which the width of tunnel barriers in between nanocrystals in the nc chains exhibits a local growth in the direction from S to M ($\delta d_i/\delta x>0$) so that at least one 'bottleneck' for the hole transport becomes involved in the nc chain. In individual nc chains, such bottlenecks can be located at one and the same distance or at different distances from the injecting contact depending on the way in which the nanoparticle system in the oxide layer was prepared (for instance, through thermally activated decomposition of Si-rich nonstoichiometric oxide with depth-uniform content of excess silicon or through decomposition of a stoichiometrically structured oxide layer).

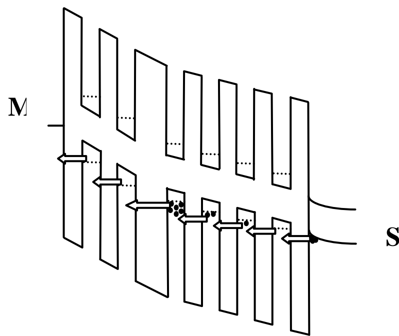

Figure 1: Charge transport through oxide in an MOS capacitor with oxide-hosted Si nanocrystals and monopolar injection of holes from the p-Si substrate.

The properties of our model can be traced considering the simplest case in which each nc chain contains just one Si nanocrystal located, in line with the above-formulated assumptions, closer to the semiconductor. On increasing the d.c. voltage U applied to MOS, the nc-trapped charge Q_{ox} grows in value together with the injection current; the increasing charge Q_{ox} leads to a growth of the oxide field predominantly in the gap adjacent to the metal. As the field in the latter gap increases, the tunneling barrier there finally becomes triangular, and the rate of tunneling emission of nc-trapped holes into the metal increases sharply, making the charge Q_{ox} decrease in value. As the charge Q_{ox} decreases, further incremental voltage changes ΔU will predominantly drop across the gap in between the injecting contact and the nc layer. This fundamental property of the model, i.e. the passage of the nc-trapped charge Q_{ox} through a maximum as a function of U is also retained in a more evolved case of nc chains involving many nanocrystals and several bottlenecks. This property of the model is an important one since it allows one to easily extend the present analysis to the case of dielectrics with arbitrary (for instance, random) distribution of embedded nanoparticles in the dielectric volume.

2 CALCULATIONS

In our calculations, we treated the case of MOS capacitors prepared on a *p*-Si substrate ($N_a=10^{15}$ cm^{-3}), with oxide-hosted Si nanocrystals forming one or more nc layers. The sheet density of nanocrystals in each of the layers was assumed to be $2.5\cdot10^{13}$ cm^{-2} (nanocrystals sized 1 nm with 1-nm lateral spacing). Along the direction normal to MOS, various arrangements of one or several bottlenecks in an nc chain formed by equidistantly spaced nanocrystals were considered. Since primary attention in the present study was focused on the electrical aspect of the problem, we chose not to treat the discrete electronic spectrum of the nc-related quantum wells, replacing it instead with a uniform energy distribution of hole states in the wells above the ground-state energy of nc-bound hole. Physically, such smearing of the discrete electronic spectrum of nanocrystals could be a result of, say, their size dispersion. For clarifying the essence of the model, injection of electrons from the metal was assumed suppressed, for instance, because of a low energy position of the Fermi level in the metal. In a schematic model, we assumed that the electric potential drops only across the tunneling gaps between nanocrystals, with no voltage drops occurring across nanocrystals themselves. It was also assumed that nc-bound holes could tunnel into downfield nanocrystals provided that empty states at the same energy level were available there. In a strong electric field, holes could also be emitted into the oxide valence band. The emitted holes were assumed to rapidly sink to the metal without contributing substantially to the oxide space charge (in the simple model, the possibility that holes emitted into the oxide valence band could be captured by downfield nanocrystals was neglected). The electric characteristics of MOS capacitors were calculated by solving the system of nonlinear equations involving the continuity equation for the hole current and the conditions of field matching across nc layers. Then, a.c. quantities could be calculated by solving the linearized equation system. Finally, MOS characteristics could be determined by assessing the total electric current (hole current + displacement current) in any cross-section in the oxide layer.

3 RESULTS AND DISCUSSION

Some data calculated for MOS capacitors with tunneling-gap widths d_1/d_2=2/3 and 1.5/3.5 nm (respectively, MOS-1 and MOS-2) are shown in Figs. 2-4 (the gaps are enumerated from the semiconductor).

The brightest consequence of the presence of oxide-hosted Si nanoparticles in the MOS capacitors is the emergence of a hump-like feature with two capacitance maxima in the accumulation branch of the low-frequency CV-curve (Fig. 2). The maxima are observed then the rate of change (increase or decrease) of the charge Q_{ox} with increasing the gate voltage U reaches a maximum (see the inset in Fig. 2). In between the two peaks, the capacitance C falls to a lower level (in a laterally uniform structure, down to C_a), the minimum of C being observed when the charge Q_{ox} reaches its highest). It can be expected that in laterally nonuniform structures the fall of C should be less pronounced due to overlap of areally non-uniform partial CV-characteristics, with the magnitude of the fall serving a measure of lateral uniformity of the electrical properties of the structure. With increasing the frequency ω, the two capacitance peaks disappear from the CV-curve, the first peak of C, i.e. the peak observed at the lower gate voltage, vanishing first. Detailed data concerning the frequency-dependent CV-characteristics of MOS capacitors with oxide-hosted Si nanoparticles will soon be reported in [6].

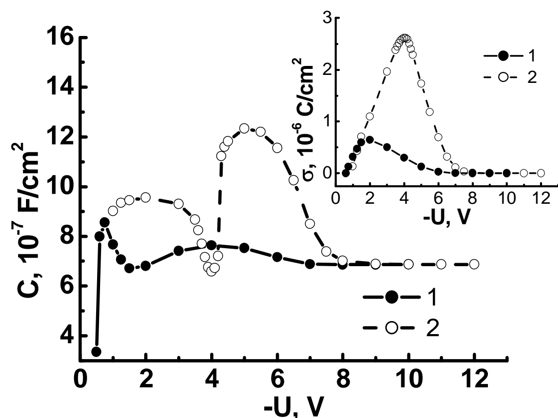

Figure 2: Low-frequency CV-characteristics of MOS-capacitors. Inset: Sheet charge accumulated in the nc layer versus U. Curve 1 – MOS-1, curve 2 – MOS-2.

The structure of the total alternating current in the two gaps of the double-barrier structure is illustrated by Fig. 3 with the example of MOS-1 (here, $C_{displ\ i} = (\varepsilon_a/d_i)\cdot(V_i^{\sim}/V^{\sim})$ is the 'capacitance' due to the displacement current in the i-th tunneling gap; the difference between C and C_{displ} gives the contribution due to the hole current).

The passage from the charge accumulation regime to the regime with the decrease of the previously accumulated charge Q_{ox} is also manifested in the change of the slope of static I-V characteristics of the MOS capacitors plotted in the coordinates $\ln(j^{-}) - U$ (see Fig. 4; other interesting relevant experimental data can be found in [7]).

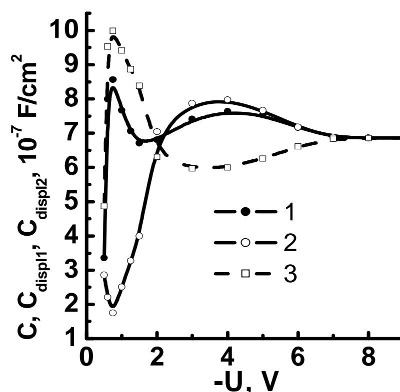

Figure 3: Structure of the total a.c. component in the two gaps of MOS-1. 1 – MOS capacitance C, 2 – $C_{displ\ 1}$, 3 – $C_{displ\ 2}$; the subscripts 1 and 2 refer respectively to gap 1 and gap 2.

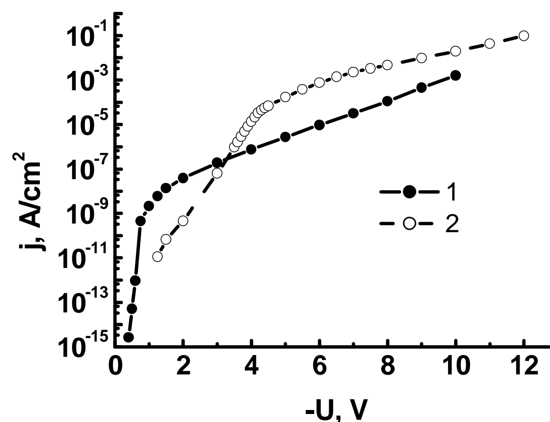

Figure 4: Current-voltage characteristic of MOS capacitors. Curve 1 – MOS-1, curve 2 – MOS-2.

Experimentally, a feature in the CV-curves of real MOS capacitors closely resembling the hump with two capacitance maxima predicted by the present model was previously observed in [1] while measuring MOS capacitors with oxide-hosted *a*-Si nanoclusters (see Fig. 5). The only difference between the situation in [1] and the case of the above-considered MOS capacitors was that, seemingly, the injecting contact in [1] was the contact with the metal while the injected carriers were electrons.

In a similar manner, more evolved situations with transport of charge carriers over nc configurations with nc chains involving many Si nanocrystals and several bottlenecks, and also over nc configurations with structurally different nc chains, can be considered. A specific feature of the latter situation is that the permeability of tunneling barriers in individual nc chains is defined, apart from the barrier widths, by the local average field E, whose value is in turn defined by the charges

accumulated at neighboring nc chains with a different structure of tunneling gaps. Calculations show that in the case of structurally identical nc chains containing several equidistantly spaced nanocrystals and one bottleneck the oxide charge Q_{ox} is ordinarily concentrated at the upfield edge of the widest tunneling gap. Here, the part of the nc system located farther in the upfield region of the bottleneck carries no substantial charge, working instead as a transporting medium. As a result, here again we encounter a situation equivalent to the above-considered case of double-barrier structure.

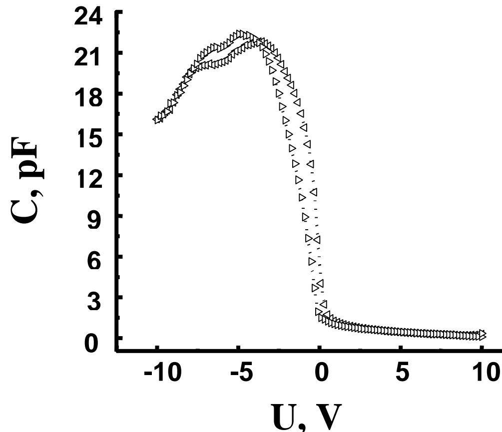

Figure 5: Measured CV-characteristics of an MOS capacitor with oxide-hosted *a*-Si clusters (d_1/d_2=20/6 nm, f=3 kHz) [1].

If several identically arranged bottlenecks are involved in each nc chain, then, due to the fact that tunneling current sharply depends on the barrier width, the conduction along identically structured chains will be defined by the least penetrable bottleneck. Here again, the charge flowing across the oxide layer will become predominantly "decelerated" in the immediate upfield vicinity of the bottleneck. As a result, we again arrive at a situation resembling the case considered above. The least trivial case here is the situation in which each of the nc chains involves two or a greater number of bottlenecks whose width increases in the direction from semiconductor to metal so that, with the growth of U, successive (with some delay over U) elimination of the bottlenecks in the oxide occurs. It can be expected that, here, each bottleneck removal will render the hole states in nanocrystals located in between the eliminated bottleneck and the bottleneck located upfield of the latter bottleneck empty of holes. Calculations show that involvement of several bottlenecks in nc chains ordinarily results in some minor modification of the shape of the curve $Q_{ox}(U)$ and, hence, only slightly distorts the general appearance of the double-peak feature in the low-frequency CV-curves of MOS capacitors.

In the case of nc chains with dissimilar tunneling structures and, especially, with dead-end chain branches located in the upfield region of the least permeable bottleneck, the charge accumulated in the oxide can be distributed more broadly across the oxide in comparison with the above-treated case of double-barrier structure. Nonetheless, the discussed general behavior of Q_{ox}, namely, its passage through a maximum as a function of U will be retained here as well, with the same outcome for the shape of the low-frequency CV-curves.

Finally, we would like to note here that the main properties of the present model are obviously insensitive to a particular mechanism of charge transport through the oxide, be that tunneling migration of charge carriers over an nc system or, say, tunneling transport of charge carriers mediated by their trapping at intermediate defect sites in the oxide. It should also be noted for generality that, in principle, involvement of a bottleneck in the model is not necessary for the model to yield the discussed feature. Indeed, calculations of MOS capacitors with equidistant arrangement of nanocrystals in nc chains show that, here again, the charge accumulated in the oxide first grows in value and, then, decreases as a function of U. Bottlenecks present in nc chains just promote accumulation of a greater charge in the oxide, thus making the hump feature in the low-frequency CV-curves of MOS capacitors more pronounced.

4 CONCLUSIONS

To summarize, we have investigated the basic properties of the model that was previously proposed to explain the electrical characteristics of MOS capacitors with oxide-hosted Si nanoparticles. The data obtained in the present study may prove useful in many applications, including characterization of dielectric layers with embedded semiconductor nanoparticles, characterization of charge transport properties of dielectric materials, creation of favorable conditions for efficient electroluminescence in film structures, etc.

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