Design of ASIC Dedicated to Thermal Analysis of Many-Core Architectures

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ABSTRACT

This paper presents Application-Specific Integrated Circuit (ASIC) designed for verification of thermal coupling analysis in many-core processors based on logic-thermal simulations. The paper contains a detailed description of the test ASIC composed of a 16x24 array of power cells which are treated as heat sources. A rectangular matrix of appropriately configured heat source can simulate the behavior of a real core. The size of the heat cell array is set in order to facilitate thermal simulations of many-core processors with different granularity. The most important electrical parameters of the power (heat) cell are presented in this paper together with layout requirements that have to be met in order to ensure proper heat distribution in the chip.

Keywords: ASIC, many-core architecture, thermal analysis, thermal coupling

1 INTRODUCTION

In recent years a new trend in the processor design has been observed. Processors consist of 2, 4 and more cores. This is connected with the constant increase in demand for computing power of computers. It is expected that computers in the near future will be equipped with hundred of cores in a single processor [1]. What is more, distance between individual cores inside a chip decreases with shrinking characteristic (feature) size of transistors in new technologies.

Growing demand on computational power causes processor cores to dissipate more power which in combination with size scaling leads to increase of power density within a chip. This, in turn, is foreseen to make the thermal coupling among cores lying close to each other a serious problem with design of future multi-core architectures [2].

Authors of the paper decided to elaborate logic-thermal simulator that will be useful in determining the value of the coefficient of thermal couplings in processors equipped with 4 and more cores. In order to verify simulation results, a special integrated circuit was designed. Although, first approach to the chip design was already described [3], authors decided to modify the project in order to improve the heat dissipation properties of the test ASIC.

The second section describes in detail the power (heat) cell. Paragraph number three contains a description of a number of simulations of the chip with particular emphasis on the current Digital-to-Analog Converter (DAC). This is a very sensitive circuit, that is why a detailed analysis of it is shown. The advantages and disadvantages of a solution chosen by the authors are drawn in the conclusions of this paper.

2 ASIC DESIGN

This section presents details of the proposed ASIC architecture with special attention put to the power cell which is the basic building block of the proposed chip. The layout of the cell needs to be considered carefully since position and size of the high voltage transistors (heat sources) plays an important role during thermal simulations. The distribution of hot spots constitutes an additional constraint which is usually not taken into account during design of the analog circuits.

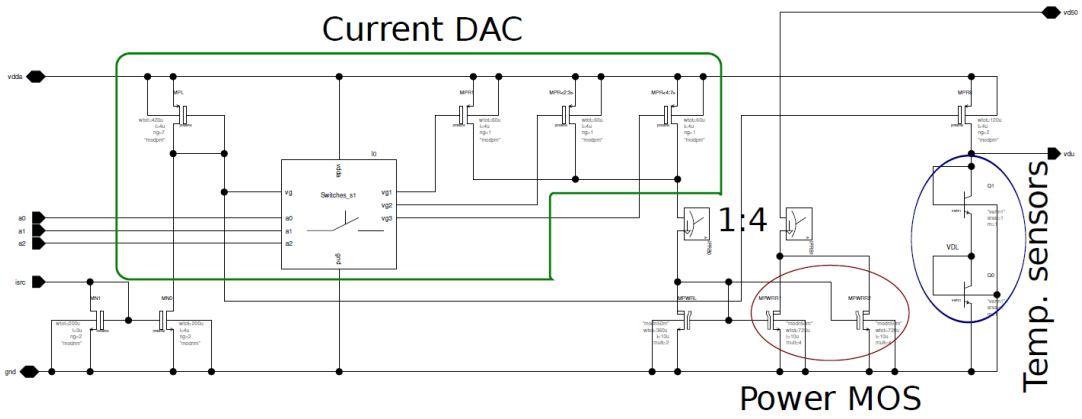

Figure 1: Electrical scheme of the power (heat) cell.

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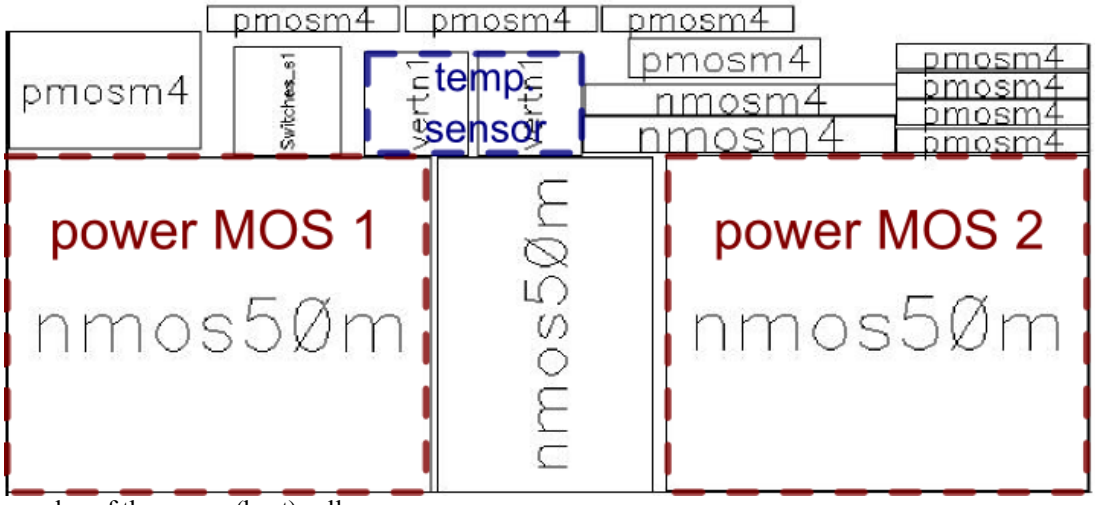

Figure 2: Floor-plan of the power (heat) cell.

The presented ASIC consists of 384 power (heat) cells which represent the power dissipation sources in real many-core microprocessors. These heat cells, having the total area of about 0.05 mm^2, create a 16x24 array. The main parts of the heat cell are the heat source and temperature sensors (see Fig. 1). The heat source is constituted by the output of a configurable current mirror – two power MOS transistors which can be seen in Fig. 1 – connected to high voltage source of 50 V. The current mirror output can sink up to 10 mA, which gives maximal power of 0.5 W per heat cell. It is assumed that power contribution of other transistors in the heat cell is negligible due to their relatively low supply voltage (3.3 V).

The actual current flowing through the power MOS transistors, and consequently the dissipated power, is set by a 3-bit Digital-to-Analog Converter (DAC) placed in every heat cell which scales reference external current using one of 8 levels according to actual configuration stored in a shift register added to each power cell. The DAC output current is than copied with ratio 4 to 1 into the power MOS transistors in order to achieve final value of dissipated power. Quality of current scaling and copying is crucial in order to obtain reliable heating conditions. Therefore the DAC and power transistors needed to be carefully designed taking into account electrical behavior as well as area constraints.

In general a DAC performance can be characterized by a set of parameters covering its static and dynamic behavior [4]. The authors found dc characteristics as the most important with regard to application with the proposed thermal simulator. Special attention was paid to linearity issue. The goal was also to minimize difference of the output current between different power cell with the same configuration taking into account gain and offset variations of the dc characteristic across the chip.

3 SIMULATION RESULTS

All simulations described in this paragraph were done in Cadence® IC/Spectre and Matlab environment. The former tools were used to verify the ASIC design against electrical requirements, while special Matlab program was used to verify temperature distribution inside chip. Next two sections show in detail all results.

3.1 Electrical Simulations

Using considerably long transient analyses, the authors were able to obtain transfer characteristic of the power cell. Values of Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) were automatically recorded with a special Verilog-A block added to the test bench.

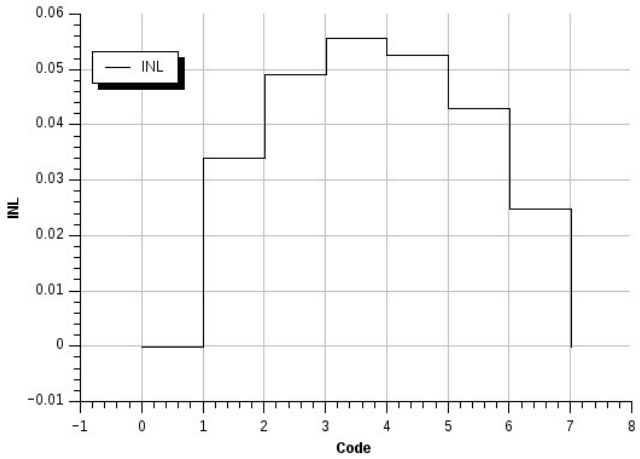

Figure 3: INL plot of the DAC.

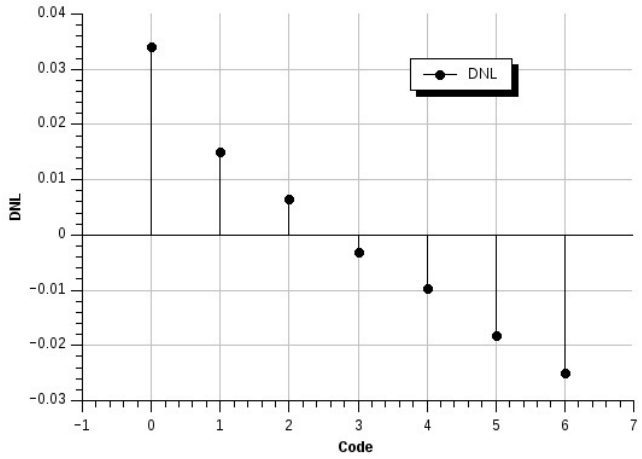

Figure 4: DNL plot of the DAC.

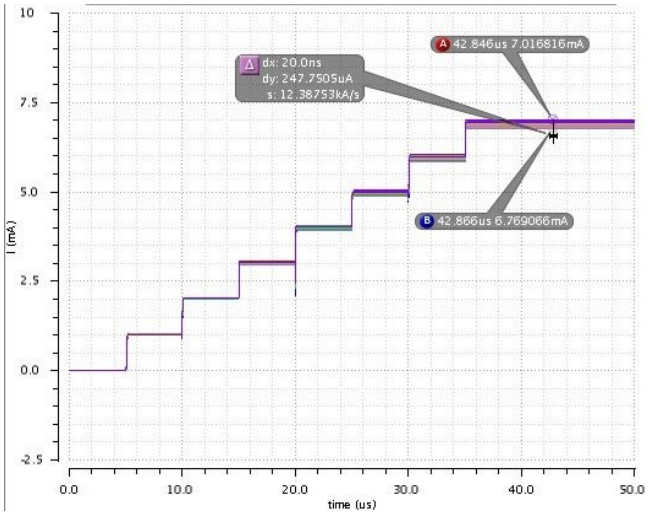

Figure 5: Results of the Monte Carlo simulations – power cell output current vs. time.

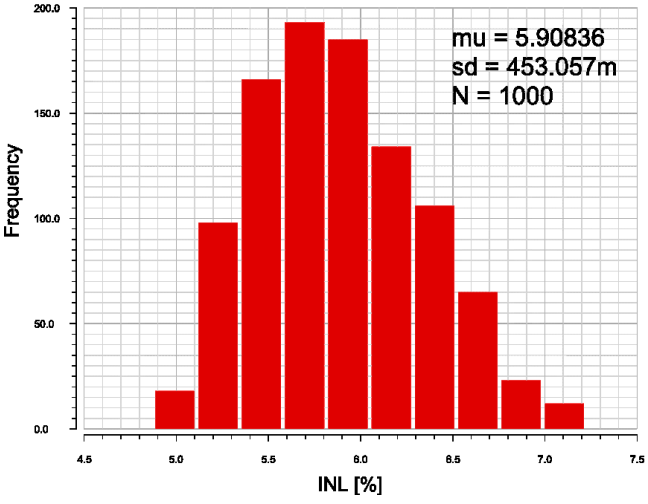

Figure 6: Results of the Monte Carlo simulations – INL histogram.

Figs. 3 and 4 present integrated and differential non-linearity simulation results of the proposed current DAC, respectively. Since the DAC input code is not expected to be changing during a thermal simulation, the former parameter is more meaningful in this application. As it can be seen from the figures, maximal INL for nominal PVT conditions is below 6 % and DNL below 4 %.

Fig. 5 presents results from Monte Carlo simulation of 1000 runs with nominal reference input current of 2 mA. As it can be seen in the figure, the spread of maximal current (at time t = 40 us) is well below half of the least significant bit value. Histogram of maximal INL value (Fig. 6) shows that in the worst case scenario, one can expect INL below 7.5 %.

Transient parameters of the output current are not imperative, since settling time below 1 µs satisfies requirements of the proposed thermal simulations method.

The power cell was also analyzed against its noise performance. One can expect power MOS transistors to be the most important noise sources due to their high transconductance (gm). In general, output noise of the current mirror can be minimized by minimizing transistors' gm by decreasing their width-to-length ratio (W/L) or increasing gate-source voltages [5]. Taking into account limited voltage headroom of the output current mirror and relatively high currents, the authors could not decrease W/L ratio of the power transistors below certain value (720 um/10 um). What is more, minimizing transistors' widths would reduce their area contribution to the power cell, which is against requirements of the thermal simulations. In fact, noise simulations performed using Cadence® Spectre® showed that noise related to two power transistor constitutes more than 96 % of the overall output noise. Consequently, it was decided that noise optimization of the DAC would not significantly improve the power cell noise performance.

Finally, layout of the power cell needs to follow requirements of the thermal simulations. The area and distribution of the power transistor need to be done in a way to avoid substantial temperature drop between heat sources in the thermal simulations. As a consequence, it was decided that power transistors should constitute no less than 50 % of the power cell area and they should not be gathered in the power cell center.

As it was mentioned, each power cell is equipped with programmable DAC. Configuration of the heat cell array is done in a serial manner. Each cell is equipped with 3 registers which hold input signal for the DAC. All the configuration registers in the heat cell array are connected in order to create one long shift register. It is possible to configure the heat cells independently in order to realize different simulation scenarios according to actual configuration bit chains. For instance, it is possible to turn on only one heat cell at the time in order to perform calibration of the temperature sensors. A heat cell can mimic the behavior of functional blocks of a

microprocessor such as Arithmetic Logic Unit (ALU). A rectangular matrix of appropriately configured heat source can simulate the behavior of a real core. The size of the heat cell array is set in order to facilitate thermal simulations of many-core processors with different granularity.

Each heat cell is equipped with diodes which perform on-chip measurement of the local temperature of silicon. Voltage signals from the diodes are multiplexed on 96 analog outputs of the presented ASIC.

3.2 Thermal Simulations

The first thermal simulations was done in Matlab using the analytical Green's function method described in [6]. The results shows that in the first version of a chip the temperature between each heat cell drops down from 23°C to 16°C (Fig. 7) which is clearly visible in the temperature rise map. This result was unacceptable, since each group of 4 cores should in theory mimic a single core in real many-core architecture. The problem lies in the relative size of the heat sources in the test ASIC. In the first version of the layout, the area occupied by the power MOS transistors was about 25 % of the total area of the heat cell which enlarged distance between heat sources.

In order to improve a heat distribution in the chip, each power transistor was rescaled. The area occupied by power MOS transistors is now more than half of the total area of the power cell. This leads to more uniform temperature distribution in the simulated chip.

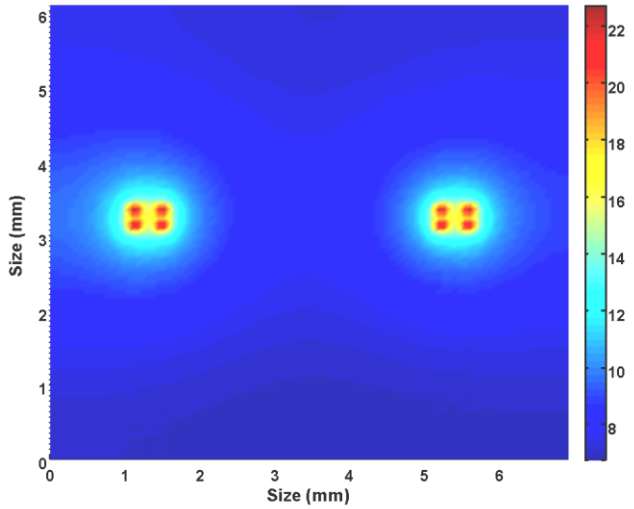

Figure 7: Temperature rise map for 2 heat sources containing 4 heat cells.

4 CONCLUSIONS

The proposed design of the analog power cell, as the most important part of the proposed ASIC, was verified using extensive simulations using software tools delivered by Cadence. The test scenario includes DAC transient analysis with different Process-Voltage-Temperature (PVT) conditions as well as Monte Carlo runs.

The area occupied by the power MOS transistor should meet the specification of heat distribution inside the ASIC. Minimal area dimension should be not less than 50 %. After meeting this condition a heat dissipation in the chip can be treated as uniform.

First thermal simulations were also done in Matlab program to evaluate steady-state behavior of the chip during operation. The thermal simulations were helpful in a determination of a heat distribution inside the chip. Authors plan to perform the transient thermal simulations which will be published in the following papers.

5 ACKNOWLEDGMENT

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