Unified Regional Approach to High Temperature SOI DC/AC Modeling

Siau Ben Chiah*, Xing Zhou*, Zuhui Chen**, Hung Ming Chen**, and Li Yuan**
*School of Electrical & Electronics Engineering, Nanyang Technological University
50 Nanyang Avenue, Singapore 629798, exzhou@ntu.edu.sg
**Institute of Microelectronics, 1 Science Park Road, Singapore Science Park II, Singapore 117685

ABSTRACT

A SOI MOSFET used in ruggedized electronics applications is measured from room temperature to 300 °C. The temperature effect on the electrical characteristics is studied. The recent unified regional model development is extended to include this effect. The extraction of the temperature coefficients used in the model and the prediction of the model to the measurement and the Medici data are included in this paper. A model that can accurately simulate and predict the electrical characteristics of a SOI MOSFET operating at elevated temperatures is useful for ruggedized electronics circuit simulations.

Keywords: MOSFET, ruggedized electronics, SOI, unified regional model, zero-temperature coefficient

1 INTRODUCTION

Integrated circuits for ruggedized electronics applications that can still operate at high temperatures may have a large market such as in automobile, military, mining and well-logging industries. Transistors operate at such elevated temperature conditions may suffer from high temperature effects, which results in I_{on}/I_{off} ratio degradation, subthreshold slope and threshold-voltage reduction [1].

A SOI MOSFET on a wafer used in ruggedized electronics is measured from room temperature to 300 °C. A gate voltage at zero-temperature coefficient point, V_{ztc} is observed from the measurement data. It has been identified by Shucair [2], Prijic *et al.* [3] and further commented by Eman *et al.* [1] that the point is a value of V_g at which the reduction of threshold voltage due to the higher operating temperature is counter-balanced by the reduction of the mobility. It is an important parameter that needs to be taken into consideration for a stable RF CMOS integrated circuit that operates with large temperature variation [4].

Unification of MOS compact models with the unified regional modeling (URM) approach [5] has been demonstrated for accurate modeling of various types of MOS devices, such as bulk, partially/fully-depleted SOI, double-gate (DG) FinFETs and gate-all-around (GAA) silicon-nanowires (SiNWs) with the surface-potential based formalism. This paper extends the recent unified regional model development to include temperature effect from room temperature to 300 °C. The extraction of the temperature coefficients used in the model and the prediction of the model accuracy to the measurement data are presented in this paper.

2 MODEL FORMULISM

The surface-potential based drain current equation with the idea of symmetric charge linearization [6] around the "mid-point potentials" is given by [5]

$$I_{ds0} = \overline{\beta_0}\left(\overline{q_i} + \overline{A_b} v_{th}\right)\Delta\phi_s\,, \tag{1}$$

$$\overline{\beta_0} = \overline{\mu_{eff0}} C_{ox}\left(W/L\right), \tag{2}$$

$$\overline{\mu_{eff0}} = \left(\mu_{eff0,s} + \mu_{eff0,d}\right)/2\,, \tag{3}$$

$$\overline{q_i} = V_{gf} - \overline{\phi_s} - \Upsilon\sqrt{\overline{\phi_s} - \overline{\phi_o}}\,, \tag{4}$$

$$\overline{A_b} = 1 + \frac{\Upsilon}{2\sqrt{\overline{\phi_s} - \overline{\phi_o}}}\,, \tag{5}$$

where W is the channel width for bulk/SOI/DG MOSFETs, $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the gate capacitance (per unit area), $\Delta\phi_s$ is the surface potential difference at the source/drain (S/D) ends, $\phi_o = 0$ is the zero-field potential for bulk or partially-depleted SOI, and

$$V_{gf} \equiv V_g - V_{FB} \tag{6}$$

is defined as the "flatband-shifted" gate voltage, with V_{FB} being the flatband voltage. $v_{th} \equiv kT/q$ is the thermal voltage at absolute temperate, T with the Boltzmann constant, k and the magnitude of the electrical charge on the electrons, q. The body is given by

$$\Upsilon = \frac{\sqrt{2q\varepsilon_{Si}N_{ch}}}{C_{ox}}\,. \tag{7}$$

$$N_{ch} = n_i e^{\phi_F/v_{th}} \tag{8}$$

is the effective channel doping with the Fermi-potential given by the well-known Kingston equation [7],

$$\phi_F = v_{th}\sinh^{-1}\left(\frac{N_A - N_D}{2n_i}\right). \tag{9}$$

$$n_i = \sqrt{N_C N_V}\, e^{-\frac{E_g}{2kT}} \tag{10}$$

is the intrinsic carrier concentration [8] with the effective density of states in the conduction band and the valence band, respectively,

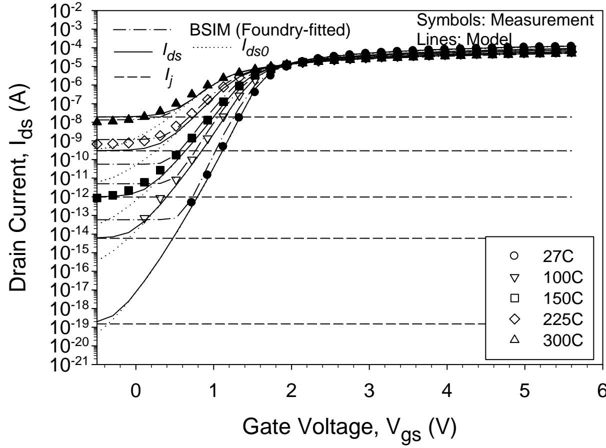

Figure 1: The temperature dependent $I_{ds} - V_{gs}$ with (I_{ds}) and without (I_{ds0}) junction leakage model. Close-symbols: data used for calibration.

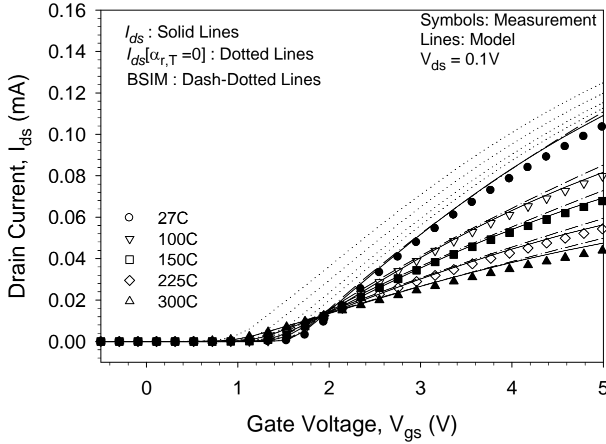

Figure 2: The temperature dependent $I_{ds} - V_{gs}$ with and without mobility degradation factor. Close-symbols: data used for calibration.

$$N_C = N_{c,300}\left(\frac{T}{300}\right)^{N_{C,F}}, \tag{11}$$

$$N_V = N_{V,300}\left(\frac{T}{300}\right)^{N_{V,F}}. \tag{12}$$

$$E_g = E_{g,300} + E_{g,alph}\left(\frac{300^2}{300 + E_{g,beta}} - \frac{T^2}{T + E_{g,beta}}\right) \tag{13}$$

is the bandgap energy, which depends on absolute temperature, T with $N_{C,F}$, $N_{V,F}$, $N_{C,300}$, $N_{V,300}$, $E_{g,alph}$ and $E_{g,beta}$ as the model parameters. $E_{g,300}$ is the bandgap energy at 27 °C.

The longitudinal-field dependent mobility in (3) is given by [5]

$$\mu_{eff\,0,c} = \frac{\mu_0}{1 + \delta_L\left(V_{c,eff} - V_r\right)/\left(LE_{sat}\right)} \quad \left(c = s, d\right), \tag{14}$$

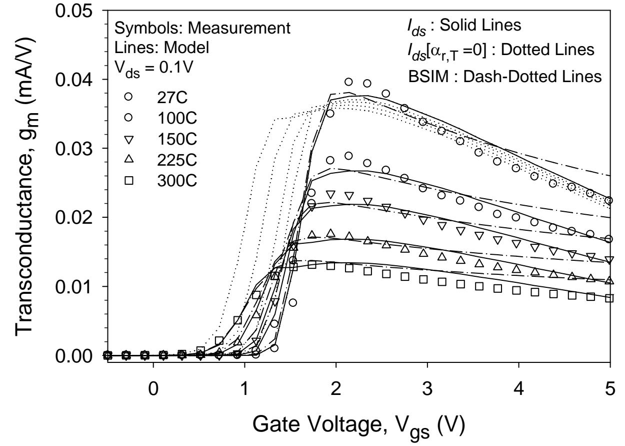

Figure 3: The temperature dependent transconductance prediction with and without mobility degradation factor.

where δ_L is a model fitting parameter. The temperature dependent transverse-field mobility is

$$\mu_0 = \frac{\mu_{1,T}}{1 + \left(\mu_{1,T}/\mu_{2,T}\right)E_{eff}^{1/3} + \left(\mu_{1,T}/\mu_{3,T}\right)E_{eff}^{v}}, \tag{15}$$

$$\mu_{r,T} = \mu_r\left(\frac{300}{T}\right)^{\alpha_{r,T}} \qquad \left(r = 1, 2, 3\right), \tag{16}$$

in which μ_r and v are the fitting parameters at room temperature and $\alpha_{r,T}$ is the mobility degradation factor. E_{eff} in (15) is the effective field, which is listed in [5].

The ϕ_s-based current equation in (1) requires the solution of ϕ_s at the S/D ends. The single-piece unified regional surface-potential solutions are given by

$$\phi_{acc} = \vartheta_r\left(V_{gf}; \sigma_a\right) + 2v_{th}\mathcal{L}\left\{\frac{\Upsilon}{2\sqrt{v_{th}}}e^{-\left(V_{gf} - V_r\right)/2v_{th}}\right\}, \tag{17}$$

$$\phi_{sub} = \phi_o + \left(-\frac{\Upsilon}{2} + \sqrt{\frac{\Upsilon^2}{4} + \vartheta_f\left(V_{gf} - \phi_o; \sigma_f\right)}\right), \tag{18}$$

$$\phi_{str,c} = \vartheta_f\left(V_{gf}; \sigma_s\right) - 2v_{th}\mathcal{L}\left\{\frac{\Upsilon}{2\sqrt{v_{th}}}e^{\left(V_{gf} - 2\phi_F - V_c\right)/2v_{th}}\right\} \quad \left(c = s, d\right), \tag{19}$$

in accumulation, depletion, and strong inversion regions, respectively, in which $\mathcal{L}\{W\}$ is the *Lambert W* function, and σ_a, σ_f, and σ_s are smoothing parameters used in the following two "complementary" smoothing functions

$$\vartheta_f\left\{x; \sigma\right\} = 0.5\left(x + \sqrt{x^2 + 4\sigma}\right), \tag{20}$$

$$\vartheta_r\left\{x; \sigma\right\} = 0.5\left(x - \sqrt{x^2 + 4\sigma}\right). \tag{21}$$

The sum of ϕ_{acc} and ϕ_{sub}

$$\phi_{sa} = \phi_{acc} + \phi_{sub} \quad (22)$$

gives a single-piece unified surface-potential solution valid from accumulation to depletion regions.

$$\phi_{ds,c} = \vartheta_{eff}\left(\phi_{sub}, \phi_{str,c}; \delta_{\phi}\right) \quad \left(c = s, d\right) \quad (23)$$

gives a single-piece unified regional solution valid from depletion to strong inversion regions with the following transition function

$$\begin{aligned}\vartheta_{eff} &= \left\{x, x_{sat}; \delta\right\} \\ &= x_{sat} - 0.5\Big[x_{sat} - x - \delta \\ &\quad + \sqrt{\left(x_{sat} - x - \delta\right)^2 + 4\delta x_{sat}}\Big]\end{aligned}, \quad (24)$$

in which δ is a smoothing parameter. A full-region single-piece unified regional surface-potential solution can be formed by adding (17) with (23), given by

$$\phi_{seff} = \phi_{acc} + \phi_{ds}. \quad (25)$$

In DC operating conditions, a MOSFET is normally biased from depletion to strong inversion regions. The "mid-point" surface-potential in (1), (4), and (5) is given by

$$\overline{\phi_{ds}} = \frac{\phi_{ds,d} + \phi_{ds,s}}{2}. \quad (26)$$

The surface-potential different at the S/D ends is

$$\Delta\phi_{ds} = \phi_{ds,d} - \phi_{ds,s}. \quad (27)$$

The final drain-current expression with junction leakage can be written as

$$I_{ds} = I_{ds0} + I_j, \quad (28)$$

in which the junction diode leakage [9] as a function of temperature is given by

$$I_j = AJ \exp\left\{\frac{E_{g,300}/v_{th,300} - E_g/v_{th} + \varphi_j \ln\left(T/T_{nom}\right)}{v_j}\right\}, \quad (29)$$

with the thermal voltage at room temperature, $v_{th,300}$. AJ, φ_j, and v_j are the model parameters.

In AC operating conditions, a full-region single-piece unified regional gate-charge expression [5] can be expressed as

$$Q_g = Q_b + Q_d + Q_s, \quad (30)$$

with a single-piece unified regional bulk-charge expression

$$Q_b = -C_{ox}\left[Q_{b,acc} + Q_{b,sub} - \frac{\left(\overline{A_b} - 1\right)\Delta\phi_{ds}^2}{12H}\right], \quad (31)$$

$$Q_{b,acc} = \vartheta_r\left(V_{gf}; \sigma_a\right) - \phi_{acc}, \quad (32)$$

$$Q_{b,sub} = \vartheta_r\left(V_{gf}; \sigma_a\right) - \vartheta_f\left(V_{gf}; \sigma_a\right) + \Upsilon\sqrt{\overline{\phi_{ds}} - V_b}. \quad (33)$$

The single-piece unified regional drain charge and source charge are given, respectively, by

$$Q_d = -\frac{C_{ox}}{2}\left[\overline{q_i} - \frac{\overline{A_b}\Delta\phi_{ds}}{6}\left(1 - \frac{\Delta\phi_{ds}}{2H} - \frac{\Delta\phi_{ds}^2}{20H^2}\right)\right], \quad (34)$$

$$Q_s = -\frac{C_{ox}}{2}\left[\overline{q_i} + \frac{\overline{A_b}\Delta\phi_{ds}}{6}\left(1 + \frac{\Delta\phi_{ds}}{2H} - \frac{\Delta\phi_{ds}^2}{20H^2}\right)\right], \quad (35)$$

$$H = \left(\overline{q_i}/\overline{A_b}\right) + v_{th}. \quad (36)$$

3 MODEL PARAMETERS EXTRACTION, RESULTS AND DISCUSSION

The model parameter extraction procedure for the drain-current model in (1) and the charge model in (30) at nominal temperature can be referred to [10] with the proposed certain set of measurement data and biasing conditions. In high temperature unified regional modeling approach, the subthreshold current behavior is physically modeled by the change of the body doping in (8) and Fermi-potential in (9) due to the change in operating temperature without any fitting parameters, which is indicated by solid-lines and dotted-lines in Fig. 1 with and without junction diode leakage, respectively.

Three temperature coefficients (AJ, φ_j, and v_j) in (29) can be calibrated by three I_{off} measurement data points or three linear region I_{ds}–V_{gs} measurement data at nominal, mid, and high temperatures (closed-symbols in Fig. 1). Together with the calibrated junction leakage solutions (dashed-lines in Fig. 1), I_{ds} solutions (solid-lines in Fig. 1) in (28) predict accurately the measurement data (open-symbols). I_{ds} simulation and prediction are close to the solutions from foundry-fitted BSIM model (dash-dotted lines in Fig. 1).

The threshold-voltage reduction at increasing temperature is indicated by the dotted-lines in Fig. 2 as a result of the temperature effects from (6)–(13) without considering mobility degradation effect ($\alpha_{r,T}$ = 0). This gives accurate subthreshold behavior but over-predicts I_{ds} current in the linear region. Together with the mobility degradation factors ($\alpha_{r,T}$) in (16), which can be extracted from three linear region I_{ds}–V_{gs} measurement data at nominal, mid, and high temperatures (close-symbols in Fig. 2), I_{ds} in (28) predicts accurately the measurement data (open-symbols in Fig. 2) and the V_{ztc} point, its transconductance in Fig. 3 and output conductance in Fig. 4 with the solid-lines, which are compared to foundry-fitted BSIM model (dash-dotted lines).

The threshold-voltage reduction at increasing temperature can also be observed in the AC Medici data (open-symbols in Fig. 5). The full-region single-piece unified regional model in (30) with the temperature effect models (6)–(13) provide accurate gate capacitance solutions (with the solid-lines in Fig. 5) to the Medici data from room temperature to 427 °C.

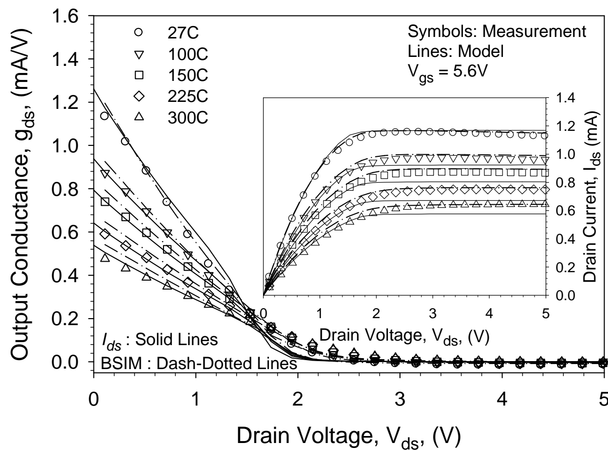

Figure 4: The temperature dependent output conductance and the drain current (inset) are compared to a foundry-fitted BSIM model and the measurement data.

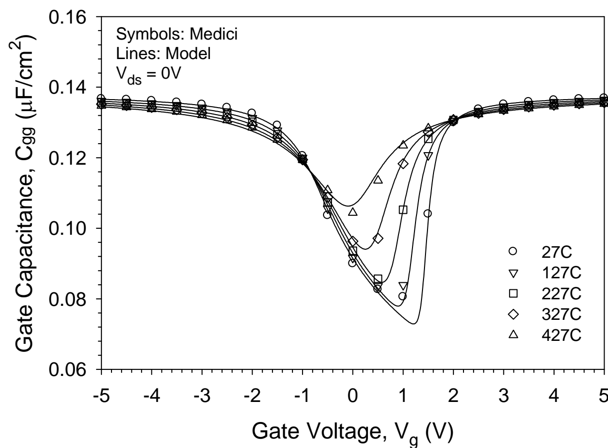

Figure 5: The prediction of the temperature dependent unified regional AC model, compared to the MEDICI simulation.

4 SUMMARY AND CONCLUSION

The recent unified regional AC/DC model development has been extended to include the temperature effects. Three junction leakage coefficients and three mobility degradation coefficients are added to the model, which can be calibrated by three I_{ds}–V_{gs} measurement data at nominal, mid, and high temperatures. The models have been validated with the measurement data from a ruggedized electronics SOI wafer and Medici simulations. Due to the limited measurement data on this wafer, the long-channel partially-depleted SOI MOSFET measurement data is used to validate the model.

***Acknowledgement**:* This work was supported in part by the Institute of Microelectronics under Agreement for Research Collaboration through the A*STAR SERC Grant No. 102 165 0085.

REFERENCES

[1] Mostafa Emam, Julio C. Tinoco, Danielle Vanhoenacker-Janvier, and Jean-Pierre Raskin, "High-temperature DC and RF behaviors of partially-depleted SOI MOSFET transistors," Solid-State Electron., Volume 52, No. 12, 1924–1932, Dec. 2008.

[2] F. S. Shoucair, "Analytical and experimental methods for zero-temperature-coefficient biasing of MOS transistors," Electron. Lett., Volume 25, 1196–1198, 1989.

[3] Z. Prijic, S. S. Dimitrijev, N. Stojadinovic, "The determination of zero temperature coefficient point in CMOS transistors," Microelectron. Reliab., Volume 32, No. 6, 769–773, Jun. 1992.

[4] I. M. Filanovsky and L. Najafizadeh, "Zeroing in on a zero-temperature coefficient point," 45th Midwest Symposium on Circuits and Systems, Volume 1, I–271–274, 2002.

[5] X. Zhou, G. Zhu, G. H. See, K. Chandrasekaran, S. B. Chiah, and K. Y. Lim, "Unification of MOS compact models with the unified regional modeling approach," (Invited Paper), J. Comput. Electron., Volume 10, No. 1, 121–135, 2011.

[6] T. L. Chen and G. Gildenblat, "Symmetric bulk charge linearization in charge-sheet MOSFET model," Electron. Lett, 791-793, 2001.

[7] R. H. Kingston and S.F. Neustadter, "Calculation of the space charge, electric field, and free carrier concentration at the surface of a semiconductor," J. Appl. Phys., 718–720, 1955.

[8] Taurus Medici, Medici User Guide, 2–10, June, 2006.

[9] W. Liu et al., BSIM4.6.4 User's Manual, University of California, Berkeley, 2009.

[10] G. H. See, "Scalable Compact Modeling for Nanometer CMOS Technology," Ph.D. Thesis, Nanyang Technological University, 2008.