

Novel MEMS-Based Diffractive Spatial Light Modulator

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ABSTRACT

The architecture, principle of operation and first fabrication of a novel MEMS-based, multi-level, phase modulating pixellated spatial light modulator is presented. The device enables a novel platform for tiny, energy-efficient video projection systems suitable for mobile consumer electronics. Challenges that arise in the design and fabrication of small-scale, highly compliant micro-electro-mechanical systems (MEMS) flexures with dimensions on the order of 200nm are discussed.

Keywords: MEMS, spatial light modulator, pixellated array devices, MEMS/CMOS monolithic integration, embedded video projection

1 BACKGROUND

Optical phase modulation using pixellated spatial light modulators has a broad range of potential applications in 2D and 3D imaging, gesture sensing, adaptive optics, optical telecommunications, and holography, among others. In this work, we extend the optical phase modulator concept to the development of a unique MEMS-based holographic spatial light modulator (H-SLM) with extremely small geometry and large stroke range, monolithically integrated on a CMOS backplane to enable a novel platform for tiny, extraordinarily energy-efficient video projection systems suitable for embedding into consumer electronics devices (Figure 1). Given the unique characteristics of the device, however, applicability beyond digital projection may emerge. Broader still, the fabrication processes developed herein forms the basis of a platform for highly-compliant MEMS structure fabrication which will become increasingly relevant to a range of MEMS devices as structure sizes and compliances scale downward driven by requirements for cost, performance and yield.

Widespread adoption of digital light projection in mobile applications is limited by high power consumption resulting primarily from the illumination power needed for acceptably bright projected images. Light Blue Optics (LBO) Holographic Light Projection (HLP) technology dramatically advances projection efficiency through the development of a dynamic illumination engine that results in three-fold improvement in brightness and efficiency compared with conventional digital projection technologies such as liquid crystal (LCD, LCOS) or MEMS (DLP, Texas Instruments) (1). In fact, HLP may provide the only practical path for offering the brightness (> 50 lumen) and efficiency (> 30-50 lumen/W) needed to achieve the performance required for mobile markets. Furthermore, HLP's diffractive approach enables the design of uniquely

compact projection modules, with very large throw angles and focus-free operation. The result is the viability for the first time of compact, high efficiency projection displays suitable for mobile devices such as camcorders and cell phones.

The HLP system (Figure 2) consists of red, green, and blue (R,G,B) lasers (collimated by lenses L1 to L3, and combined by dichroic mirrors M1 to M3) sequentially illuminating the phase-modulating microarray (H-SLM) which directs light patterns onto the imaging spatial light modulator (I-SLM) via Fourier optics L4. In this example, I-SLM is a digital micro-mirror device (such as Texas Instrument's DLP). D1 is a oscillating optical diffusing element providing speckle reduction and L5 and L6 form a projection lens assembly.

In this system, H-SLM acts as a low resolution dynamic illumination engine for a standard imaging SLM. HLP technology uses the H-SLM not instead of, but in addition to, a conventional I-SLM. As a consequence of the dual panel architecture, the resulting HLP chipset is resolution-independent, with final image resolution depending not on the H-SLM but on the companion I-SLM resolution. A single HLP chipset can therefore address a range of products and markets with different brightness and resolution specifications. HLP works with existing projection engines to improve their efficiency, rather than competing with them.

Conventional digital projection relies on a light-masking principle in which a microdisplay is uniformly illuminated by the maximum light intensity and dark pixels simply block or dump the incident light. Since average pixel intensity for a typical video image is under 20%; a standard imaging system blocks 80% of light just to form the image. In contrast, LBO's HLP system applies highly efficient diffraction to "steer" light to areas on the image that are bright and concurrently "steers" it away from areas that are dark. Low spatial frequency components of the image (representing most of the light intensity) are generated diffractively by the H-SLM, and the high spatial frequency details (containing very little light intensity) are added using a conventional I-SLM. Therefore for video, an HLP projector may be up to three times more efficient (or therefore three times brighter) than conventional projectors. In addition, because the illumination on the imaging display (I-SLM) is spatially optimized for each frame, the contrast performance of the system is also improved, typically by up to an order of magnitude.

2 MEMS H-SLM

2.1 H-SLM Architecture

Central to LBO's projection technology is the MEMS H-SLM, consisting of a 2D array of phase-modulating "pixels" monolithically fabricated on top of a CMOS backplane. Each pixel is a translational electrostatic actuator consisting of an electrode formed from the top metal of the driver chip, a cavity, a spring (the electro-mechanical actuator fabricated from silicon-germanium), and a hexagonal mirror on top of the spring (Figure 3-5). The mirror shape is hexagonal to minimize the perimeter-to-area ratio, which minimizes diffractive loss due to pixel dead space.

For any optical system, the system size scales strongly with the illuminating beam diameter since optical elements and optical path lengths also scale with the beam diameter. Since the array must be fully illuminated by beam, the array size is constrained to enable the reduction in the optical system size. At the same time, the H-SLM array resolution must be high enough to produce a spatial frequency that captures the majority of the spectral energy in the image. An optimal array size for this trade-off is around 160 x 160 pixels or 2.2 x 1.6 mm for a pixel pitch of 14 μm x 10 μm . This represents a reduction pixel count by a factor of 10-80 relative to that of imaging SLMs. A smaller array results in a smaller die size, increased die-per-wafer and device yield.

Secondly, by virtue of the holographic projection technique, the SLM performance is tolerant to pixel defectivity. In conventional projections systems, there is a 1:1 map between pixels on the panel and the pixels in the projected image – that is, a defective pixel on the panel produces a defective pixel in the projected image. In holographic projection, the projected image represents the Fourier transform of the hologram generated on the H-SLM. Therefore, a pixel defect does not result in a localized defect in the projected image, but in a distributed wavefront error over the whole image that results in global loss of contrast. Calculations indicate that random defectivity of up to 1% of the total device pixel count could be tolerated in the optimal HLP system, while defectivity requirements in standard imaging SLMs are usually three to four orders of magnitude tighter. Such tolerance to defectivity provides greater latitude in manufacturing.

Monolithic CMOS and MEMS integration is a critical advantage in advanced MEMS devices since it provides important advantages such as superior signal integrity (lower parasitic capacitance and resistance) between MEMS structures and control/readout circuitry, minimized chip footprint, with no need for complex package-level interconnects. Indeed, many advanced arrayed MEMS devices can only be fabricated in a monolithic fashion because of the high data rates needed to operate them.

Polycrystalline silicon-germanium (poly-SiGe) is a cornerstone of monolithic CMOS and MEMS integration because it possess the unique combination of CMOS compatibility and mechanical integrity. Poly-SiGe is compatible with CMOS processing from a contamination and thermal budget perspective. Aluminum-based interconnect often exhibits significant increases in line

resistance after prolonged exposure to temperatures above 425C due to alloying (2). Polycrystalline SiGe films can be deposited at temperatures as low as 385C (Figure 6) making the processing compatible with metallization. The thermal tolerance for LBO's CMOS backplane has been demonstrated with acceptably small degradation (<10%) metal line conductivity after annealing that simulates thermal exposure during poly-SiGe deposition at 400C (Figure 7); however, annealing at 450C causes unacceptable increases in metal line Rs of 30-40% which would lead to timing issues in the device.

Mechanical reliability of poly-SiGe MEMS flexure elements has been reported in the literature (3). Certainly, reliability performance cannot be generalized and is specific to the individual application and device packaging. In comparison, electroplated or sputtered metals can be deposited at low temperatures, but usually exhibit a high degree of creep and fatigue. Some metals or metal alloys can be engineered to have acceptable mechanical properties for lower-strain flexure elements; however, such applications usually do not require controlled flexure stiffness.

2.2 H-SLM Principle Of Operation

Each pixel has a stroke of approximately 400nm with 32 equally-spaced phase steps of 13nm that shift the phase of light by up to one wavelength of red, green or blue light at 45 degree incident angle. Relative phase shifts generated between pixels result in interference which allows an incident wavefront (from laser illumination) to be reshaped through diffraction with very low loss of light. As a multilevel phase device, the H-SLM has theoretical diffraction efficiencies approaching 90% or greater (4). Pixel actuation is achieved by applying a voltage between the spring (which acts as the upper electrode) and a lower electrode (the top metal layer of the CMOS backplane) which results in electrostatic attraction pulling the spring (and mirror) into the cavity (Figure 8). The spring provides an elastic restoring force acting against the electrostatic driving force. The steady-state displacement is the position where the electrostatic and elastic force are balanced.

2.3 Highly Compliant Structures

Due to pixel area constraints on high-voltage transistors and other factors, the required 400nm displacement must be achieved with an actuation voltage of under 11 V. Device modeling shows that extremely compliant spring structures (on the order of 0.1 N/m) are required to obtain the desired deflection using voltages within this budget. This compliance is achieved by fabricating MEMS spring elements that are an order of magnitude smaller and thinner than commonly employed in the industry today. LBO's design specifies springs with flexure width of 200nm, thickness of 150nm and spiral length of approximately

30 μ m. Such fine structures pose unique challenges in their fabrication (Figure 9 and 10).

While the use of poly-SiGe films in monolithic MEMS fabrication has been researched for over a decade, specific challenges arise in engineering the poly-SiGe film when the MEMS flexure elements become very small. Current implementations of poly-SiGe-based devices often have flexures that are several microns in width and thickness. When scaled to smaller sizes, out-of-plane and in-plane distortions and variations often occur due to stress and stress gradients in the film.

For out-of-plane distortions, stress gradients (the variation of film stress through the thickness of the film) inherent in the film become more important as the film thickness is reduced. Such stress gradients may arise from a few sources such as the stress difference between the seed layer and the bulk SiGe film and differential crystallization through the film thickness. Such distortions may be addressed by film tuning (Figure 11) and implementation of stress compensating layers.

In-plane distortions largely result from film stress causing distortion in structures after they are released (an example of such a mechanism is illustrated in the stress needle gauge shown in Figure 12). For low-pressure chemical vapor deposition (LPCVD) SiGe film, stress values obtained in this work are \sim 100MPa compressive.

The MEMS release process remains one of the most challenging and unique aspects of surface micro-machined MEMS fabrication. In the release process, sacrificial films are isotropically etched to free MEMS structures such that they are free-standing and often moveable. The vapor HF (VHF) process is a promising release method for compliant devices because its gas-phase nature allows residue-free etching of sacrificial oxide films in high-aspect ratio, closely-spaced, compliant structures without stiction. Furthermore, VHF etching is selective against many of the materials used in MEMS element fabrication including SiGe and many metals. Also, the silicon oxide film used as a sacrificial material is well-characterized in semiconductor processing and tolerates high-temperature exposure.

VHF etching is catalyzed by adsorbed hydroxyl groups (in the form of water or alcohol) on the surface of the oxide which allows the adsorbed HF to ionize. The ionized HF then reacts with oxide to form water and a volatile fluoride that moves to the gas phase. Although alcohol is depicted here mediating the ionization of HF, the product water can also catalyze the reaction. This can create a run-away reaction where the product water catalyzes further reaction which in turn generates more water. Once the reaction rate becomes uncontrolled, excessive water builds up, and bulk water condensation results (5). For moveable structures, water droplets may bridge narrow gaps and pull them together by surface tension. This is a particular issue with very compliant and thin flexures.

Therefore, careful management of water generation and removal is critical to minimize the potential for stiction during release. Stiction may be controlled by reducing

water on surfaces by tuning the process to drive it off. While such a direction reduces condensation, it also reduces the release etch rate since reactant and alcohol adsorption reduced. Indeed, current processes optimized to minimize stiction have low etch rates which result in long process times (\sim 6 hours for some LBO structures). Furthermore, such process reside near the regime where etching stops altogether because of insufficient adsorption of the reactants. The preferred conditions used for release of LBO spring structures are reduced pressure, elevated temperature, anhydrous HF chemistry. Such parameters are available with commercial equipment such as that made by Primaxx Inc. (SPTS).

In addition to release process tuning, there are specific design considerations to improve the stiction-free window. Narrow gaps designed in MEMS structures are particularly prone to condensation since the transport away of reaction product water is constrained. In LBO's specific structure, clear distinction in stiction performance can be observed between designs with 0.20 μ m gaps and 0.30 μ m gaps (Figure 13); therefore, when design allows, the gaps between moveable flexures and other surfaces should be as large as possible. Furthermore, where possible, MEMS flexure geometry should be designed with high stiffness in the direction of travel that would cause stiction.

3 CONCLUSIONS

The successful design and first fabrication of a novel MEMS-based, multi-level, phase modulating pixelated spatial light modulator enables a novel platform for small, energy-efficient video projection systems suitable for mobile consumer electronics. The fabrication techniques for high-compliance MEMS structures over CMOS explored in this work has a scope well beyond display applications. High compliance MEMS structures are becoming important because device development programs will increasingly face similar limitations as device geometries shrink and driving voltage decrease to improve performance and reduce size and cost.

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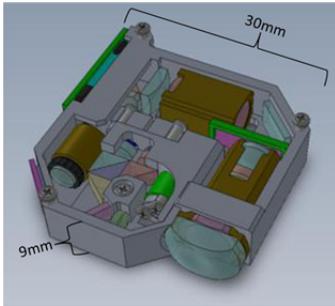


Figure 1 Schematic of HLP system

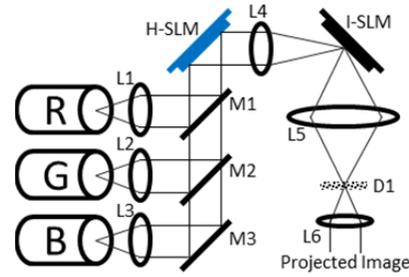


Figure 2 Schematic of HLP projection system

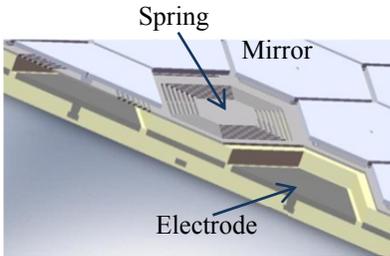


Figure 3 Diagram of pixel

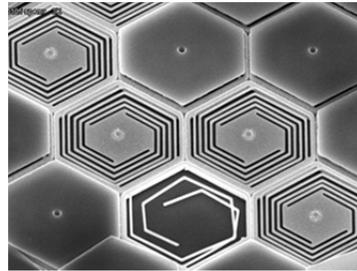


Figure 4 SEM image of pixels with mirror peeled off by tape

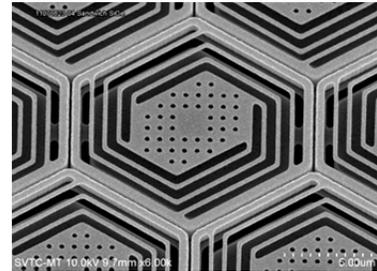


Figure 5 SEM image of spring integrated on backplane

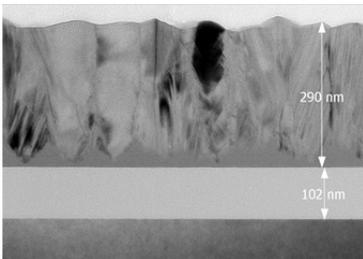


Figure 6 TEM image of polycrystalline SiGe deposited at 385C

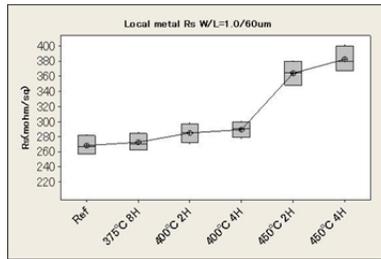


Figure 7 Metal line Rs mean and range (reference and after anneal)

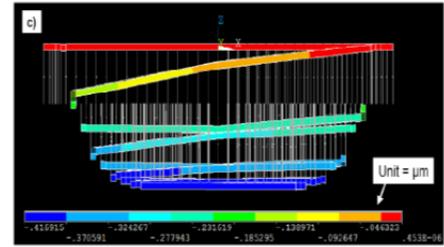


Figure 8 Model showing deflection mode of spring

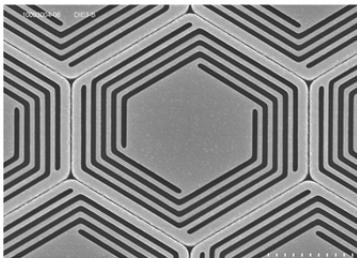


Figure 9 A less compliant structure (0.200N/m) with 0.30µm dimensions

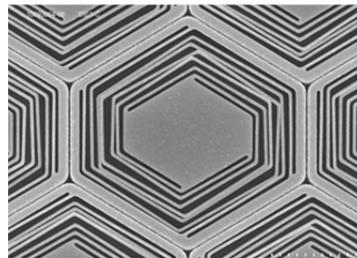


Figure 10 A more compliant (0.069N/m) spring with 0.20µm dimensions

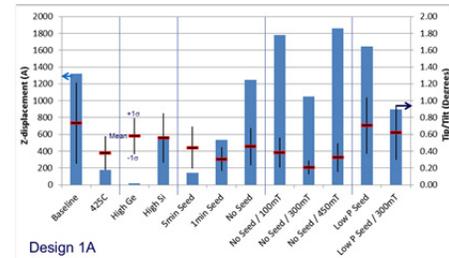


Figure 11 Parameters that improve distortions in flexures

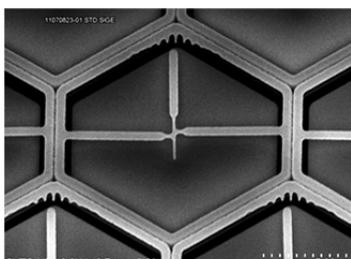


Figure 12 In-plane stress gauge indicating compressive stress

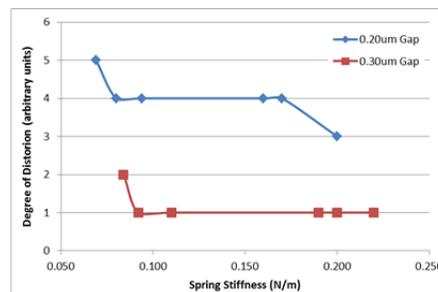


Figure 13 Degree of stiction vs stiffness for 0.20µm and 0.30µm spring gaps