Linearity evaluation of Silicon Nanowire Surrounding Gate MOSFET for high performance ULSI applications

Nishant Aggarwal*, Kshitij Sikka*, Ishan Gupta*, Rishu Chaujar*
*Microelectronics Research Laboratory, Applied Physics Department, Delhi Technological University, Shahbad Daulatpur, Main Bawana Road, Delhi-110042, India, ishangupta1991@gmail.com

ABSTRACT

The search for high performance ICs has led to scaling of MOSFETs down to sub-50nm regime, thus surrounding gate SNW MOSFETs offer a promising solution for realizing CMOS technology. Linearity is an important figure of merit in all RF and wireless applications to guarantee minimum signal distortion in modern communication systems.

In this paper, an extensive study on the effect of variation in gate/channel length (L_g) of a novel Silicon Nanowire (SNW) MOSFET with surrounding gate on linearity evaluation metrics namely V_{IP2}, V_{IP3}, *IIP3* and transconductance coefficients: g_{m1}, g_{m3} has been discussed using TCAD simulations. Simulation results reveal that linearity of SNW MOSFETs decreases as L_g increases.

Keywords: Linearity, TCAD, ATLAS, SNW MOSFET, IIP3.

INTRODUCTION

Linearity behaviour of MOSFETs is imperative for low-noise applications [1]. In the nanometre regime, SNW MOSFET is a propitious contender for CMOS applications [2, 3]. Linearity is determined by transconductance coefficients (g_{m1} and g_{m3}) and metrics V_{IP2}, V_{IP3}, *IIP3*. g_{m1} represents transconductance of the SNW MOSFET, g_{m3} is the third order derivative of drain-source current (I_{ds}) with respect to gate bias (V_{gs}) and represents third order harmonic, V_{IP2} represents extrapolated input voltage at which first and second-order harmonic voltages are equal; V_{IP3} represents extrapolated input voltage at which first and third-order harmonic voltages are equal; *IIP3* represents extrapolated input power at which first and third-order harmonic powers are equal. For high linearity g_m, V_{IP2}, V_{IP3}, *IIP3* should be as high as possible and g_{m3} should be low.

DEVICE STRUCTURE

The simulated SNW MOSFET structure (Fig1) consists of a surrounding metal gate with work function Φ_m=5.5 V. The source/drain length, width, height are 8nm, 4nm, 4nm respectively. The L_g variations used are 25nm, 30nm, 35nm, oxide permittivity, ε_{OX}=3.9. Substrate doping, $N_A=6\times10^{19}cm^{-3}$, source/drain doping, $N_D^+=1\times10^{20}cm^{-3}$.

EQUATIONS

The realization of a highly efficient linearized amplifier has emerged as a paramount issue in the RFIC design and wireless communication systems. Distortion and Linearity are key issues in the design of many types of circuits. The Volterra series has long been used to analyze distortion in analog circuit. The Volterra series is a Taylor series that simplifies to a power series when the system is memoryless. It describes a signal as a summation of the linear behaviour, the second order behaviour, the third order behaviour, and so on. Taylor series are usually used for weakly nonlinear circuit analysis because it is simple. However, it is not applicable to highly nonlinear applications such as power amplifiers. Unlike numerical simulations which give no information about the source of the distortion, closed form expressions for distortion components in terms of circuit parameters can be found using Volterra series. Unfortunately, the method of presenting the Volterra series analysis is complex and often intimidating to the uninitiated. Consequently, the Volterra series is often under-utilized by circuit designers. Circuit designers prefer to work with linear models of circuits but more accurate models which take into account the nonlinearities in a circuit are often required. Many practical circuits can be assumed to behave in a weakly nonlinear way, and under this condition, closed form expressions for the nonlinearity can be obtained using the Taylor series. In this paper, the basic of linearity analysis is presented by employing Taylor-series expansion and the expansion coefficients are extracted from the ATLAS device simulator [4].

The drain current in Taylor expansions [5] can be expressed as follows:

$$I_{DS}(V_{GS},V_{DS}) = I_O + G_M.V_{GS} + G_D.V_{DS} + G_{M2}.V^2 + G_{MD}.V_{GS}.V_{DS} + G_{D2}.V^2 + G_{M3}.V^3 + G_{M2D}.V^2.V_{DS} + G_{MD2}.V_{GS}.V^2 + G_{D3}.V^3 + \ldots\ldots\ldots\ldots \quad (1)$$

Assuming that the drain is shorted at a signal frequency, all output-conductance terms (g_d, g_{d2}, g_{d3}, ...) and cross modulation terms (g_{md}, g_{m2d}, g_{md2}, ...) are vanished and only transconductance terms (g_m, g_{m2}, g_{m3}, ...) remain.

The transconductance coefficients g_{mn} (g_{m1} and g_{m3} have been used in this paper) and device linearity analysis metrics V_{IP2}, V_{IP3} and *IIP3* are defined as :

$$g_{mn} = \frac{1}{n!}\frac{\partial^n I_{DS}}{\partial^n V_{GS}} \quad \ldots(2)$$

Thus,

$$g_{m1} = \frac{\partial I_{DS}}{\partial V_{GS}} \quad \ldots(3)$$

$$g_{m3} = \frac{1}{3!}\frac{\partial^3 I_{DS}}{\partial^3 V_{GS}} \quad \ldots(4)$$

$$V_{IP2} = 4 * \frac{g_{m1}}{g_{m2}} \quad \ldots(5)$$

$$V_{IP3} = \sqrt{24 * \frac{g_{m1}}{g_{m3}}} \quad \ldots(6)$$

$$IIP3 = \frac{2}{3} * \frac{g_{m1}}{g_{m3} * R_S} \quad \ldots(7)$$

R_S = 50 Ω for most RF applications.

To compare the linearity and intermodulation distortion performance of SNW MOSFETs, all devices are optimized at a threshold voltage (Vth) of 0.25 V, which thus accounts for a meaningful comparison.

LINEARITY ANALYSIS

To compare the linearity performance of SNW MOSFETs, all devices are optimized at a threshold voltage (V_{th}) of 0.25 V, which thus accounts for a meaningful comparison. The TCAD device simulations performed incorporate Bohm Quantum Potential (BQP) Model is illustrated [6].

Second order nonlinearity results in second order intermodulation and linearity and third order nonlinearity results in third order intermodulation and linearity. In MOS circuits, harmonic distortion is present due to the nonlinearity exhibited by higher-order derivatives of I_{DS}-V_{GS} characteristics. In the circuits using balanced topologies, even-order harmonics are cancelled out. The third order harmonic which is represented by 'g_{m3}', thus, determines a lower limit on the distortion and therefore, the amplitude of g_{m3} should be minimized. Infact, radio distortion is determined by the third order derivative of drain current to gate voltage i.e. g_{m3}.

Thus, reducing g_{m3} and increasing the transconductance (g_{m1}) acts as a viable solution to improve device linearity. Value of g_{m3} particularly determines a lower limit on distortion and, therefore, amplitude of g_{m3} should be minimized. At the same time, V_{IP2}, V_{IP3} and *IIP3* should be as high as possible. It is clearly observable from Fig5 and Fig6 that g_{m1} decreases and g_{m3} increases as L_g gradually increases .i.e. g_{m1} is maximum and g_{m3} is minimum for L_g=25nm. It is observed from Fig2 and Fig3 that SNW MOSFET with L_g=25nm has higher V_{IP2} and V_{IP3} as compared to other gate length variations (30nm, 35nm). This is because as L_g increases, threshold voltage increases. This weakens gate control over the channel, thereby degrading g_{m1} and hence, V_{IP2} and V_{IP3}. In Fig4, with increasing gate bias, *IIP3* increases to a maximum value (i.e. g_{m3}=0) followed by a minima. Fig4 clearly reflects a significant enhancement in *IIP3* in SNW MOSFET with L_g=25nm in comparison to its variations (30nm, 35nm). This is due to increase in carrier transport efficiency and gate control over the channel, thereby enhancing the gain (i.e. g_{m1}) and hence, *IIP3*.

CONCLUSION

The work presents a vital module of technological design process to build a distortion resistant device design, exhibiting enhanced analog performance for the use in ULSI technology. Intensive 3-D simulations have been performed to scrutinize the role of gate electrode workfunction engineering in Surrounding Gate Silicon Nanowire MOSFETs. A comparison of the figures of merit for analog and large signal performance of gate length variations (25 nm, 30 nm, 35 nm), it is found that the performance enhancement in SNW MOSFETs is through enhanced gate control that improves the device efficiency and speed to power dissipation performance .i.e. linearity decreases as gate/channel length increases.

The work therefore SNW MOSFET design as a promising contender and opens up the door to single-chip solutions for low-power telecommunication applications.

Thus all the parameters used (g_{m1}, g_{m3}, V_{IP2}, V_{IP3}, *IIP3*) indicate that SNW MOSFET is a promising contender for high performance ULSI application.

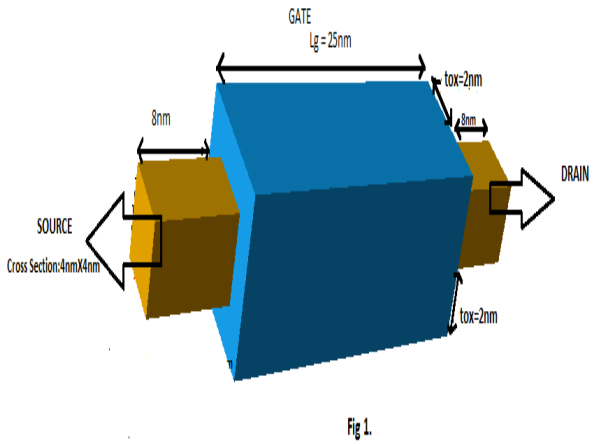

Fig. 1 Simulated Device Structure

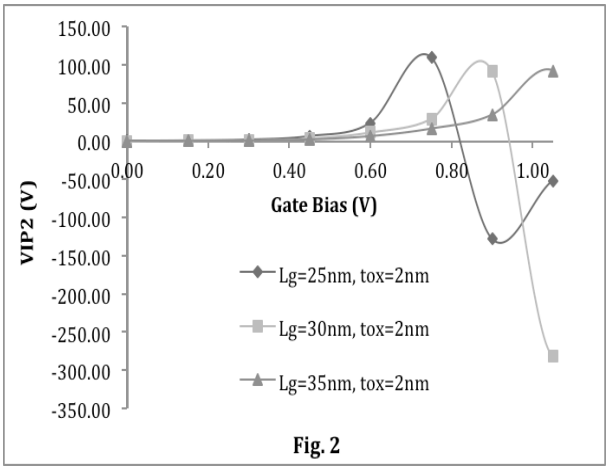

Fig2. Simulated VIP2 characteristics of SNW MOSFET (t_{ox}=2nm, V_{ds}=0.05V) with varying L_g, Device optimized at V_{th}=0.25V.

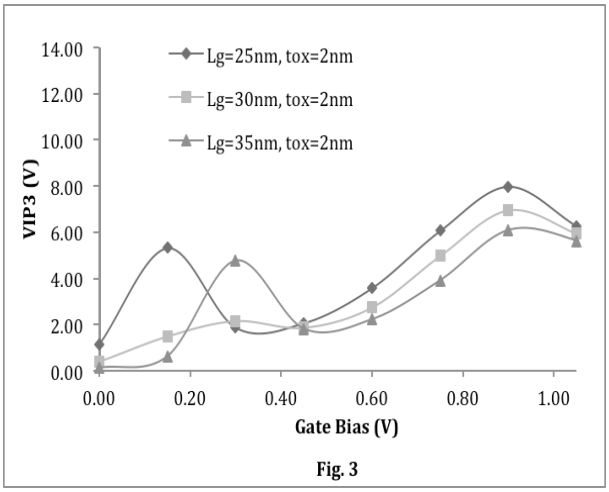

Fig3. Simulated VIP3 characteristics of SNW MOSFET (t_{ox}=2nm, V_{ds}=0.05V) with varying L_g, Device optimized at V_{th}=0.25V

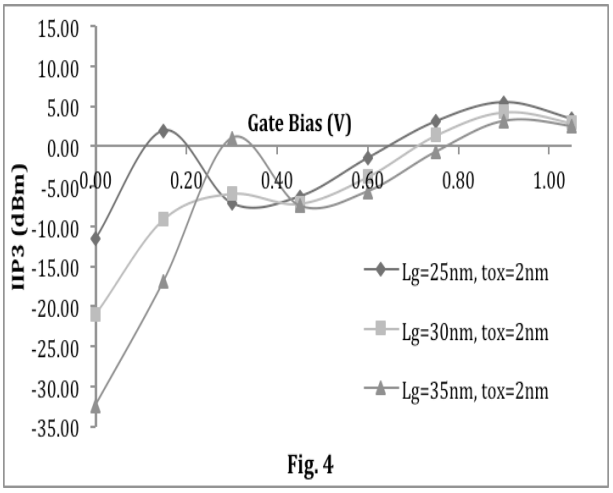

Fig4. Simulated IIP3 characteristics of SNW MOSFET (t_{ox}=2nm, V_{ds}=0.05V) with varying L_g, Device optimized at V_{th}=0.25V.

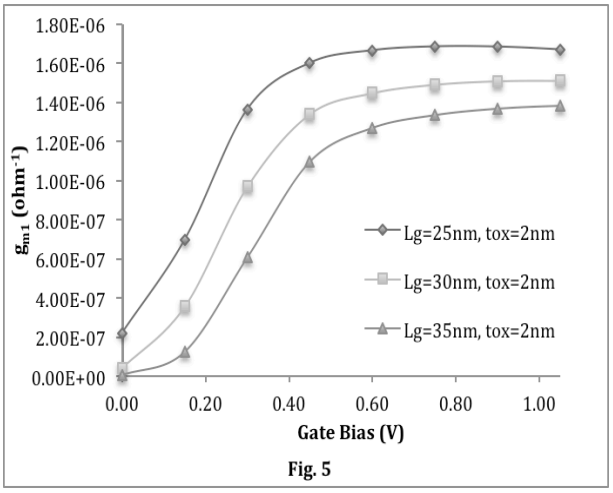

Fig5. Simulated g_{m1} characteristics of SNW MOSFET (t_{ox}=2nm, V_{ds}=0.05V) with varying L_g, Device optimized at V_{th}=0.25V.

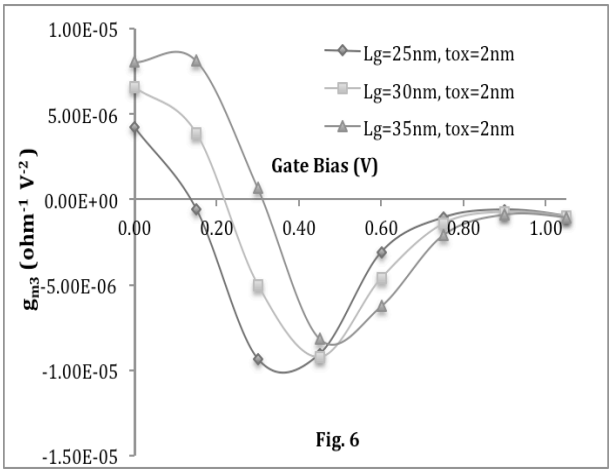

Fig6. Simulated g_{m3} characteristics of SNW MOSFET (t_{ox}=2nm, V_{ds}=0.05V) with varying L_g, Device optimized at V_{th}=0.25V.

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