Design Methodology for Ultra Low-Power Analog Circuits using Next Generation BSIM6 Compact Model

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ABSTRACT

The recently proposed BSIM6 bulk MOSFET compact model is set to replace the hitherto widely used BSIM3 and BSIM4 models as the de-facto industrial standard. Unlike its predecessors which were threshold voltage based, the BSIM6 core is charge based and thus physically continuous at all levels of inversion and from linear region to saturation region. Hence, it lends itself conveniently for the use of a design methodology suited for low-power analog circuit design based on the inversion coefficient (IC) that has been extensively used in conjugation with the EKV model and allows to make simple calculations of, for example, transconductance efficiency, gain bandwidth product etc. This methodology helps to make a near-optimal selection of transistor dimensions and operating points even in moderate and weak inversion regions. This paper will discuss the IC based design methodology and its application to the next generation BSIM6 compact MOSFET model.

Keywords: design methodology, BSIM6, low power, RF integrated circuit design

1 INTRODUCTION

Analog circuit design is a complex exercise involving multiple tradeoffs, e.g. between power consumption and speed, and several degrees of freedom like the drain current and transistor aspect ratio. Design with advanced deep-submicron technology nodes is further complicated because of the short channel effects [1]. The importance of accurate device models which stems from the fact that analog design has special modeling needs has long been recognized [2], and is all the more emphasized with the aggressive scaling of the CMOS technology and the short channel effects becoming dominant.

The requirement that a model be accurate as well as computationally fast makes the state-of-the-art compact models quite complex. The modern circuit simulators coupled with sophisticated compact models are powerful tools for design and analysis of circuits with advanced technology nodes, yet most experienced analog designers would still rely on their design intuition and do 'hand calculations' before performing any simulations. For this pre-simulation phase the designer should be able to use a stripped-down version of the model which is simple enough for initial design guidance, yet accurate enough to minimize trial-and-error simulations.

The new BSIM6 bulk MOSFET model scores on all these fronts. Adopting a charge based approach it is more physics oriented; it is not only more accurate than its predecessors but also faster than the surface potential based models [3]. Even though the full compact model includes most of the real-device effects to model the advanced bulk CMOS technologies, the core model is based on simple analytical equations which are continuous in all regions of operation. This exempts the designer to use asymptotic approximations that may be valid in weak and strong inversion regions but are inaccurate in moderate inversion (the preferred operating region for low-power analog and RF circuits [4]) and do not account for short channel effects.

The charge based BSIM6 model would extend elegantly as a design methodology too. The inversion coefficient (IC) based design methodology [5] that has been extensively used in conjugation with the charge based EKV model [6] for the design of low power analog and RF circuits [4, 7] can now also be used with the new BSIM6 model.

2 CHARGE BASED ANALYSIS

The basic charge equation in a MOSFET is given by [6]

$$2q_{\rm i} + \ln q_{\rm i} = v_{\rm p} - v. \tag{1}$$

where $q_{\rm i}$ is the normalized inversion charge density ($q_{\rm i} = Q_{\rm i}/Q_{\rm spec}$), normalized using specific charge $Q_{\rm spec}$

$$Q_{\rm spec} \triangleq -2nU_{\rm T}C_{\rm ox}. \tag{2}$$

$v_{\rm p}$ and v are the pinch-off and channel voltages respectively, normalized to thermal voltage $U_{\rm T}(= kT/q)$. The normalized drain current, normalized using the specific current $I_{\rm spec}$ [6]

$$I_{\rm spec} \triangleq 2n\mu_0 C_{\rm ox} U_{\rm T}^2 \frac{W}{L} \tag{3}$$

with μ_0 being the constant low-field mobility, is given by [8]

$$i_{\rm d} = 2q_{\rm i}\frac{u\,e}{\lambda_{\rm c}} - u\frac{{\rm d}q_{\rm i}}{{\rm d}\xi}. \tag{4}$$

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In (4) u is the effective mobility normalized to low-field surface mobility μ_0, e is the longitudinal electric field normalized to critical electric field E_c and λ_c is defined as

$$\lambda_c \triangleq \frac{2\upsilon_{sat}U_T}{\mu_0 L} \tag{5}$$

where υ_{sat} is the saturation velocity.

The inversion coefficient IC is the measure of the level of channel inversion and is equal to the drain current in forward saturation:

$$IC \triangleq \frac{I_D}{I_{spec}} = i_d\Big|_{saturation} = i_{dsat}. \tag{6}$$

As discussed in section 1, the short channel effects become prominent at sub-micron channel lengths. Two of the especially important effects are velocity saturation (VS) and mobility reduction due to the vertical field (VFMR). Both these effects are related to the mobility of the carriers. To maintain sufficient accuracy these two effects should be accounted for even in the simplistic model for hand calculations because they affect not only the magnitude but also the slopes of I_D vs. V_G and G_m/I_D vs. IC curves [6]. To include the velocity saturation effect we choose the simple piecewise linear velocity-field model for its simplicity [6] which gives the normalized effective mobility as

$$u_{eff} \triangleq \frac{\mu_{eff}}{\mu_z} = \begin{cases} 1 & \text{for } e < 1 \\ 1/e & \text{for } e \geq 1 \end{cases}, \tag{7}$$

where μ_z includes the mobility reduction due to the vertical electric field and is related to the low field mobility μ_0 by [6]

$$\frac{\mu_z}{\mu_0} = \frac{1}{1+\theta\left(q_b + q_i/2\right)} = \frac{1}{k_1 q_i + k_2} \quad \text{for } e < 1, \tag{8}$$

where

$$\theta = \frac{Q_{spec}}{\epsilon_{Si} E_0}, \tag{9a}$$

$$k_1 = \theta\left(\frac{1}{2} - \frac{1}{1+\frac{2}{\gamma_b}\sqrt{\psi_p}}\right), \tag{9b}$$

$$k_2 = 1 + \frac{\theta\psi_p}{1+\frac{2}{\gamma_b}\sqrt{\psi_p}}, \tag{9c}$$

E_0 is the electric field intensity at which the mobility starts to decrease significantly, γ_b is the normalized body factor and ψ_p is the normalized pinch-off surface potential (corresponding to $q_i = 0$). In (4) u is the effective mobility normalized to low-field surface mobility:

$$u = \frac{\mu_{eff}}{\mu_0} = \frac{\mu_{eff}}{\mu_z}\,\frac{\mu_z}{\mu_0}. \tag{10}$$

Therefore, from (7) and (8),

$$u = \begin{cases} \frac{1}{k_1 q_i + k_2} & \text{for } e < 1 \\ \\ 1/e & \text{for } e \geq 1 \end{cases}. \tag{11}$$

Following the derivation in [8] for VS and in [6] for VFMR, we obtain the drain current

$$i_{dsat} = \frac{4\left(q_s + q_s^2\right)}{2 + \lambda_{ck} + \sqrt{4\left(1+\lambda_{ck}\right) + \lambda_{ck}^2\left(1+2q_s\right)^2}}, \tag{12}$$

where

$$\lambda_{ck} = \frac{\lambda_c}{k_2} \tag{13}$$

accounts for VFMR and is slightly bias dependent because of the gate bias dependent parameter k_2 given by (9c).

The normalized source transonductance

$$g_{ms} = \frac{G_{ms}}{G_{spec}} = \frac{n\,G_m}{G_{spec}}\Big|_{saturation} \quad \text{with} \tag{14}$$

$$G_{spec} \triangleq \frac{I_{spec}}{U_T}, \tag{15}$$

can then be calculated as

$$g_{ms} \triangleq -\frac{\partial i_d}{\partial q_s}\frac{\partial q_s}{\partial v_s} = \frac{2q_s}{\sqrt{4\left(1+\lambda_{ck}\right) + \lambda_{ck}^2\left(1+2q_s\right)^2}}, \tag{16}$$

equivalently expressed in terms of i_d ($= i_{dsat} = IC$) as

$$g_{ms} = \frac{\sqrt{i_d^2\lambda_{ck}^2 + 2i_d\lambda_{ck} + 4i_d + 1} - 1}{i_d\lambda_{ck}^2 + \lambda_{ck} + 2}. \tag{17}$$

3 FIGURES-OF-MERIT FOR LOW-POWER DESIGN

In addition to the inversion coefficient, (17) serves as a main ingredient of the IC based design methodology [5, 9]. G_m/I_D, called the transonductance efficiency serves as a figure of merit for the dc operation of a MOSFET and is used as a design tool to determine the operating region and to eventually size the device. It can also be used to characterize a CMOS technology over all levels of inversion. The normalized $G_m/I_D - g_{ms}/i_d$, is equal to 1 in weak inversion and decreases on moving towards strong inversion. In strong inversion it varies as $1/\sqrt{IC}$ if no velocity saturation is present, otherwise it tends asymptotically to $1/\left(\lambda_c IC\right)$. The parameter λ_c defined in (5) is an important parameter for short channel devices that have strong velocity saturation effects. λ_c, called the velocity saturation factor, is a measure of velocity saturation effect. For a given technology it depends only on the channel length; the shorter the channel, the higher the value of λ_c and the higher the velocity saturation effect. In Fig. 1, the asymptote $1/\left(\lambda_c IC\right)$ intersects the weak inversion asymptote $g_{ms}/i_d = 1$ at $IC = 1/\lambda_c$ which can be interpreted as the demarcation between weak inversion and velocity saturated strong inversion region.

The transit frequency f_t, defined as the frequency at which the extrapolated small-signal current gain of the transistor in common-source configuration falls to unity, is defined as the ratio of the gate transconductance to the total

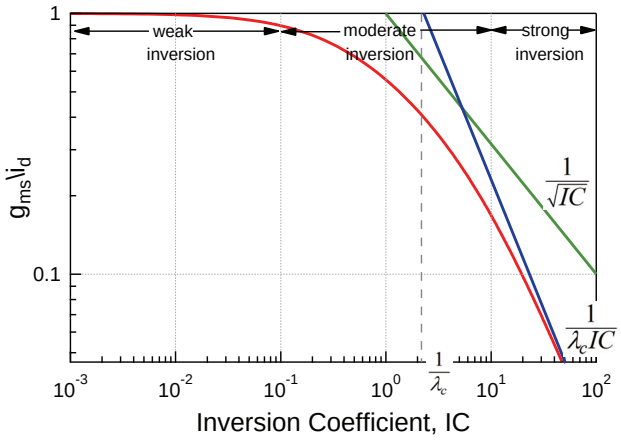

Fig. 1: $g_{\rm ms}/i_{\rm d}$ versus inversion coefficient. The asymptotes at $1/\sqrt{IC}$ and $1/\left(\lambda_{\rm c} IC\right)$ are shown.

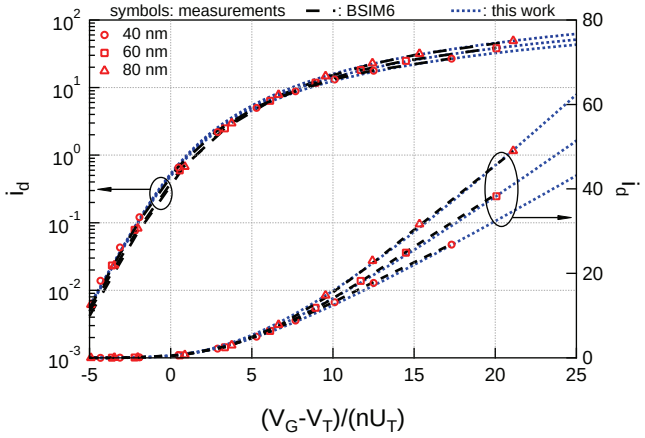

Fig. 2: $i_{\rm d}$ versus pinch-off voltage.

gate capacitance and in the normalized form is given as:

$$f_{\rm t} = \frac{g_{\rm m}}{c_{\rm G}}, \tag{18}$$

where $g_{\rm m}$ is the normalized gate transconductance and $c_{\rm G}$ is the normalized total gate capacitance (normalized to $C_{\rm OX} = C_{\rm ox}WL$). It is evident that (17) is also pertinent for RF design. The normalized gate capacitance $c_{\rm G}$ is a bias dependent parameter [6] but can be approximated by a constant value accounting not only for overlap and other extrinsic capacitances (such as fringing capacitances, which are becoming increasingly important in deep-submicron devices), but also for bias dependent intrinsic capacitances. Although this simplification obviously comes at the expense of accuracy (especially in strong inversion), it is acceptable for simple hand calculations.

$g_{\rm ms}/i_{\rm d}$ and $f_{\rm t}$ are two of the very important metrics as they account for various tradeoffs, such as, between d.c. gain, noise, offsets, linearity, gain at RF and power consumption. The input referred thermal noise and offset voltage are inversely proportional to $g_{\rm ms}/i_{\rm d}$. Because $g_{\rm ms}/i_{\rm d}$ is maximum in weak inversion, it is advantageous to bias the devices in this region from the point of view of d.c. gain, noise, d.c. offsets and, power consumption. However, the linearity of the devices degrades in this region. Moreover, $f_{\rm t}$, which is related to the gain at RF, is maximum in strong inversion. So, the devices should be biased in strong inversion to obtain significant gain at RF, and better linearity, which would be at the cost of a higher current consumption.

A new FoM that combines these tradeoffs into a single metric was introduced in [10]. It is defined as the product of $G_{\rm m}/I_{\rm D}$ and $f_{\rm t}$ and in its normalized form is given as [8]:

$$FoM \triangleq \frac{g_{\rm ms}}{i_{\rm d}} f_{\rm t}. \tag{19}$$

Since this FoM combines the two quantities which have their maxima in opposite directions of the IC axis, it is particulary suited for low-power RF design serving as a tool to locate the optimum operating point (IC) of the device. This optimum operating point (inversion coefficient) can be rapidly located by plotting the FoM as a function of inversion coefficient using (15), (17) and (18). Interestingly, for short channel devices, this FoM has a maxima in moderate inversion [8, 10] indicating that the optimum operating point lies in this region. This corroborates the advantageous use of moderate inversion for low-power RF circuits as already mentioned in section 1. The use of this FoM for RF design in moderate inversion region has been demonstrated in [11].

4 COMPARISON WITH BSIM6 AND MEASUREMENTS

Figures 2, 3 and 4 show a comparison of the analytical plots of the transfer characteristics, the transonductance efficiency and the FoM respectively, with measurements on 40, 60 and 80 nm channel length NMOS transistors fabricated in standard bulk 40 nm CMOS technology. The BSIM6 fitting results for the dc characteristics at the same channel lengths are also shown (the RF fitting of BSIM6 was not available at the time of writing). It can be seen that the simple analytical models are reasonably close to the measurements and the BSIM6 model) but, as expected, not fully accurate.

In Fig. 3 we see that for the 40 nm device, $g_{\rm ms}/i_{\rm d}$ starts degrading as $1/(\lambda_{\rm c} IC)$ already around $IC = 3$ and there is practically no region with $1/\sqrt{IC}$ dependence. For shorter devices this point would only move towards $IC = 1$ or lower. This again brings out fact that short channel devices would increasingly need to be biased in moderate inversion, substantiated by Fig. 4 where we see the peaks of the FoM, discussed in section 3, lying in this region.

5 CONCLUSION

Accurate MOSFET compact models like BSIM6, integrated with sophisticated circuit simulators, place powerful tools in the hands of analog circuit designer to design circuits using the state-of-the-art technology nodes. However,

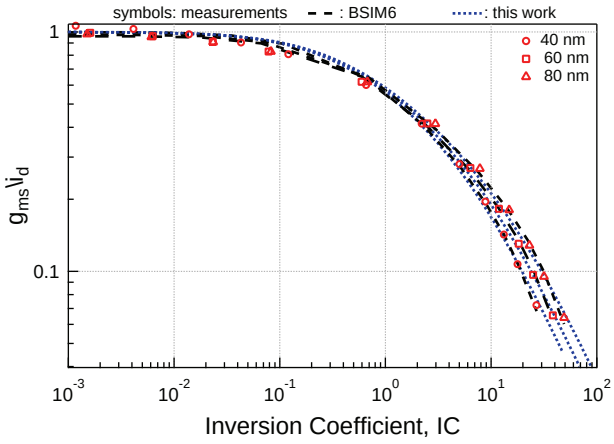

Fig. 3: $g_{\rm ms}/i_{\rm d}$ versus inversion coefficient.

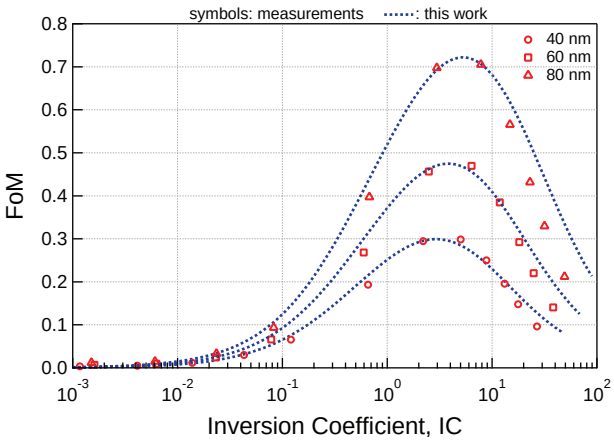

Fig. 4: FoM versus inversion coefficient.

most analog design cycles begin with simple hand calculations where tradeoffs (like that between power consumption and operating frequency) are evaluated and first-cut approximations about the operating points and dimensions of the transistors are made. Simple yet sufficiently accurate models are needed at this stage of the design cycle.

This paper summarized a set of equations and figures-of-merit especially suitable for low-power analog and RF design derived from the charge based core of the BSIM6 model, that are simple enough for use with basic numerical tools, yet accurate enough to yield a good first-order approximation of the operating point, viz., inversion coefficient IC. Using the new RF FoM it was shown that the the optimum operating point for low-power RF circuits lies in the moderate inversion region emphasizing the importance of accuracy of the model in this region.

A comparison with full BSIM6 compact model and measurements on NMOS devices fabricated with 40 nm standard bulk CMOS technology was also presented. The comparison points out to the advantage of the charge based approach adopted in BSIM6: it can be used both as a full featured compact model and as a pre-simulation design methodology.

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