Critical review of CNTFET compact models

M. Claus[1], M. Haferlach[1], D. Gross and M. Schröter[1,2]
Chair for Electron Device and Integrated Circuits (CEDIC)
[1]Technische Universität Dresden, 01062 Dresden, Germany
[2]UC San Diego, La Jolla, CA 92093, USA

ABSTRACT

This review focuses on the suitability of current physics-based carbon nanotube (CNT) field effect transistor (FET) compact models for the design and simulation of RF analog applications. The most critical deficiencies are the lack of (i) a smooth description of small-signal transistor characteristics, (ii) a verification of the charge and intrinsic capacitance models, and (iii) a proper Schottky barrier description for compact modeling purposes. In addition, the review sketches the essential physics which are necessary to understand and to classify the different compact modeling approaches published so far. A short review of state-of-the-art production-like multi-tube CNTFETs points out the compact modeling challenges. For the latter a semi-empirical approach presently appears to be the only viable option for analog circuit design studies.

Keywords: CNTFET, compact model, experimental results, analog circuit, high-frequency

1 INTRODUCTION

The demand for power efficiency and speed in mobile communication systems drives existing conventional semiconductor process technologies such as CMOS, SiGe-BiCMOS and III/V technologies to their performance limits. One option for meeting the stringent system specifications is the exploration of emerging revolutionary technologies which may provide fundamental advantages. Suitable device models are an important part of the circuit design and process development process as they reduce the risk of fabricated circuits not meeting their specifications. While sophisticated compact models are available for conventional technologies, they are still at an experimental level for emerging technologies such as CNT and graphene FETs, which are being discussed in the research community for succeeding CMOS.

The one-dimensional (1D) transport and the related low scattering rate of charge carriers in CNTs promise low noise, low power dissipation, and especially low signal distortion due to the inherent high linearity of the relevant current-voltage characteristics. Thus, CNTFETs should be ideally suited for communication systems [1]. The very recent progress in manufacturing carbon nanotube transistors (CNTFETs) [2],[3] makes these transistors attractive for analog circuit applications [4] which require very accurate compact models describing the transistor behavior.

So far, most CNTFET compact models have been developed for digital circuit design, employing ideally single-tube (ST) transistors. For analog circuit design, a feasible compact model needs to fulfill a number of stringent requirements such as high-order continuity of all bias-dependent model equations and smooth geometry scaling. Also, parameter extraction is typically more demanding. A complete list of requirements can be found in [5]. Moreover, for RF applications, multi-tube (MT) CNTFETs are required for several reasons (see below). Most MT CNTFET compact models are based on ST models by proper scaling and inclusion of MT related effects.

Therefore, a critical review of current CNTFET compact models is needed to evaluate their suitability for RF analog circuit design. Special focus lies on the mismatch between state-of-the-art CNTFET technologies and the assumptions underlying the models. To support the discussion, compact model results are compared with experimental data of high-performance CNTFETs and with device simulation results of a Schrödinger-Poisson solver.

2 STATE-OF-THE-ART DEVICE STRUCTURES

Three types of CNTFETs exist: ST, MT and thin-film (TF) CNTFETs. The anticipated nanoscale dimension of ST CNTFETs makes them ideally suited for digital applications where a high packing density is mandatory. However, since the maximum current delivered by a ST is at best in the tens of μA range, STs are unsuitable for RF applications where load impedances in the range of 50 Ohm and output power in the mW range are required. MT CNTFETs with many CNTs in parallel address this issue since they can be easily scaled to meet the above specifications. In contrast, TF CNTFETs are not feasible for RF analog applications due to their low carrier mobility across the percolation CNT network.

As it is typical for an emerging technology, CNTFETs are still mostly fabricated in research labs, but there are already a few companies trying to develop production-type processes. While deliberate placement of ST CNTFETs is still impossible, it is not true for MT CNTFETs. As a consequence, the main focus for developing a production-type CNTFET technology is on analog MT CNTFETs for which adequate compact models are thus needed.

A schematic cross-section of a planar MT CNTFET is shown in Fig. 1a. To individually connect the CNTFETs in a circuit and to minimize capacitive parasitics, top gate device structures are necessary. The CNTs are grown on an insulating substrate and connect S and D directly in contrast to TF CNTFETs. The middle region of the CNT is controlled by the top gate which is separated from the tube by a thin gate oxide. The source and drain contact metal covers the CNTs. The non-gated tube portions between the gate and the source/drain metal (called spacers here) may be doped. In addition, due to cost constraints, only relaxed device dimensions of about 0.5µm to 1µm channel length are currently feasible for production-type processes.

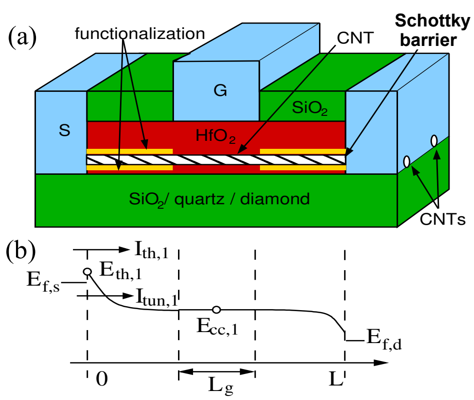

Fig. 1: (a) Cross-section of a planar top gate MT CNTFET and (b) conduction band $E_{c,1}$ of the first subband for $V_{GS} > 0$ and $V_{GS} > 0$.

Several methods are known for manufacturing CNTs. An attractive and increasingly found method is to grow CNTs from a catalyst directly on a wafer using CVD. Depending on the substrate, control of the tube growth direction can be challenging. Misalignment on SiO2 eventually lead to intertube crossings forming potential barriers at the intersection points. Unfortunately, CNT growth on a substrate also yields metallic tubes in addition to the semiconducting tubes with statistically distributed properties. Many methods for minimizing the number of metallic tubes in MT CNTFETs have been studied but no method has been successfully employed in a production-type process so far leading to undesired parasitic current paths in MT CNTFETs.

In addition, Schottky barriers between the contact metal and the CNTs are typically formed with significant impact on the device behavior. To minimize the effect of the Schottky barriers, the spacers should be doped as highly as possible while the tube region under the gate should be left intrinsic for maximizing current modulation by the gate and minimizing scattering. However, current production type technologies do not include intentional doping of the spacers due to temperature stability issues of existing dopant materials. Thus, the impact of Schottky barriers is not negligible in current production-type technologies. In addition, most manufactured CNTFETs show hysteresis and self-heating effects which further complicate model verification.

In summary, compact models for state-of-the-art CNTFETs need to consider long channels with non-negligible scattering effects, non-ohmic contacts and tunneling phenomena due to Schottky barriers at the metal-CNT interfaces, parasitic metallic CNTs within the channel, tube-tube interactions due to intertube crossings as well as hysteresis effects and self-heating. In addition to the phenomena listed above, experiments suggest that ambipolarity may be important in undoped devices [6] while for highly doped spacers, several current carrying subbands may have to be considered [7].

3 Theory

In spite of the relaxed device dimensions of present production-type technologies, the transport regime may still be in between ballistic and scattering dominated due to the 1D transport and the related low scattering probability. Predicting the resulting non-equilibrium charge distribution and drain current requires an appropriate description of the charge injection from the contacts and proper assumptions concerning the scattering events.

According to a quasi-ballistic approach, the electron charge of the υ^{th} subband in a CNT comprises left and right injected carriers and is generally given by

$$n_{\upsilon} = \int g_{\upsilon}^{+}(E)dE + \int g_{\upsilon}^{-}(E)dE = n_{\upsilon}^{+} + n_{\upsilon}^{-} \tag{1}$$

where g_{υ}^{+} and g_{υ}^{-} are the energy-dependent non-equilibrium carrier distribution of the left and right injected carriers. (Similar equations hold for the hole carrier concentration and the hole current.) Ignoring all quantum ballistic mechanisms such as tunneling and quantum reflections, an often found approximation (called *pseudo-bulk approximation*) for the carrier density is

$$n_{\upsilon} = \frac{4}{3}\frac{1}{\pi a_{cc} t_{cc}} \int_{E_{c,\upsilon}} D(E, \psi)(f(E, E_{f,s}) + f(E, E_{f,d}))dE \tag{2}$$

where $E_{c,\upsilon}(x) = 0.5E_{g,\upsilon} - q\psi(x)$ is the subband dependent conduction band edge, ψ is the electrostatic potential, $E_{g,\upsilon}$

be the subband-dependent CNT band gap, a_{cc} is the carbon-carbon distance (0.142 nm) and t_{cc} is the tight-binding energy between carbon atoms (3 eV). Furthermore,

$$D(E, \psi) = \frac{E + q\psi}{\sqrt{(E + q\psi)^2 - \frac{1}{4}E_{g,\upsilon}^2}} \quad (3)$$

is the density of states of the CNT, f is the electron Fermi function, and $E_{f,s}$ and $E_{f,d}$ are the Fermi levels in the source and drain contact.

Electron current flow in nanoscale devices is commonly related to its transmission properties. A suitable description for the current through a subband υ is given by the Landauer-Büttiker formula [8]

$$J_\upsilon = \frac{4q}{h}\int_{-\infty}^{\infty} T_\upsilon(E)(f(E, E_{f,s}) - f(E, E_{f,d}))dE \quad (4)$$

where T_υ is the energy-dependent transmission probability describing tunneling as well as scattering effects. In general, T_υ is closely related to the non-equilibrium charge distribution. However, models for T_υ and g_υ which are computationally acceptable for compact modeling purposes do not yet exist and several approximations are necessary for closed-form solutions.

4 Compact Modeling Concepts

A general large signal equivalent circuit for an intrinsic ST CNTFET is shown in Fig. 2. I_D is the drain current source, $\dot{Q}_{qs}$ and $\dot{Q}_{qd}$ are current sources related to the time-derivative of the terminal charges, and R_{cs} and R_{cd} are contact and access resistances.

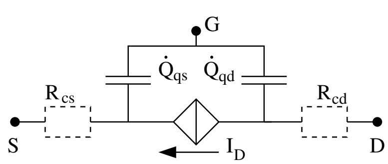

Fig. 2: Large signal equivalent circuit for an intrinsic ST CNTFET (R_{cs} and R_{cd} are optional).

Four steps guide the development of a compact model for ST CNTFETs: (*i*) definition of a *current control energy* $E_{cc,\nu}$ and simplified description of (*ii*) the transmission probability $T_\upsilon(E)$, (*iii*) the carrier distributions g_υ^+ and g_υ^-, and (*iv*) the electrostatic potential determining the bias dependence of $E_{cc,\nu}$. Note that the reduction of the conduction band profile to a single current control point was originally proposed by Natori [9] for Si MOSFETs.

In general, the lower current integration limit is fixed by the minimum energy $E_{cc,\nu}$ for which the transmission through the device is non-zero

$$T_\upsilon(E) = \begin{cases} T_\upsilon(E) & \text{for } E \geq E_{cc,\upsilon} \\ 0 & \text{for } E < E_{cc,\upsilon} \end{cases}. \quad (5)$$

This energy is called current control energy and x_{cc} fulfilling $E_{c,\upsilon}(x_{cc}) = E_{cc,\upsilon}$ is the *current control point*. In a electrostatically well balanced transistor (flat and drain bias independent conduction band under the gate), the current control point is generally in the middle under the gate as shown in Fig. 1b.

4.1 Electrostatics and charge calculation

Since the electrostatic potential generally depends on the charge density and on the electrostatic coupling between the tube and the terminals, the value of $E_{cc,\nu}$ is bias- (and in general also position-) dependent. Note that the definition of $E_{cc,\nu}$ does not exclude tunneling or scattering mechanisms.

Simplified expressions describing the coupling between the tube potential ψ_{cc} and the charges on both tube and contacts are proposed in the literature. The most accurate one is given by

$$Q_q(\psi_{cc}) = C_{e,s}V_s + C_{e,d}V_d + C_{e,g}\overline{V_g} - \sum C_e\psi_{cc} \quad (6)$$

where ψ_{cc} is implicitly given and requires an iterative solution. Moreover, equation (6) calls for a proper description of the tube charge $Q_q = q\sum n_{cc,\upsilon}$ at x_{cc}. Only in the thermionic limit (see below), a calculation based on the pseudo-bulk approximation (2) is reasonable. So far, a physics-based analytical closed-form description of Q_q is still missing. Other approaches propose to directly fit the bias dependence of ψ_{cc} by polynomial [10] or rational [11] fit functions. However, the related fit parameters are difficult to adjust to experimental data. In addition, a smooth description of the small-signal transistor characteristics such as the transconductance $g_m = dI_{ds}/dV_{gs} = n_g(dI_{ds}/d\psi_{cc})$ with the gate coupling coefficient $n_g = d\psi_{cc}/dV_{gs}$ requires a smooth description of n_g which is not ensured in [10],[11].

Fig. 3a shows the carrier distribution from (1) calculated with a ballistic Schrödinger-Poisson (SP) solver [12] in the middle of a 50 nm long CNTFET for V_{gs}=0.8 V and V_{ds}=0.2 V. A comparison with the semi-classical carrier distribution (i.e. the product of the density of states and the Fermi function) reveals a significant deviation. In [13] similar results are shown for quantum simulations including scattering effects.

In order to model the transient and small-signal response of a CNTFET, current sources modeling the time-dependent changes of Q_q are included in the equivalent circuit. A partitioning of $Q_q = Q_{qs} + Q_{qd}$ into source Q_{qs} and drain Q_{qd} related charge portion is required to properly assign the dynamic currents to the terminals.

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In [14] and [15], Q_{qs} and Q_{qd} are identified with the carriers injected from source $Q_{qs} = qL_g n_{cc}^{+}$ and drain $Q_{qd} = qL_g n_{cc}^{-}$ where n_{cc}^{+} and n_{cc}^{-} are pseudo-bulk carrier concentrations. In addition, the proposed charge partitioning is questionable at least in the presence of Schottky barriers. However, an experimental verification of the charge partitioning in ST CNTFETs is very challenging due to the problems associated with the high impedance mismatch between the tube and the measurement equipment. For a verification based on simulation results, a time-dependent transport model is required capturing both scattering and quantum effects. This seem to be reasons why neither [14] nor [15] show an experimental verification of their approach.

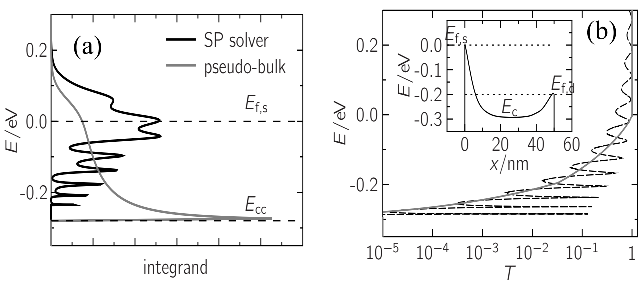

Fig. 3: (a) Sample carrier distribution (black) in the mid of a 50 nm long Schottky barrier CNTFET calculated with a ballistic SP solver. For comparison, the pseudo-bulk carrier distribution (grey) is also shown. (b) Transmission probability calculated with a ballistic SP solver and a WKB method. The inset shows the conduction band profile used for the calculations.

4.2 Thermionic Transport Limit

Let $E_{th,\nu}$ be defined as the maximum of $E_{c,\nu}$ along the channel (e.g. the top the source Schottky barrier, cf. Fig. 1). Hence, $E_{th,\nu}$ splits the current distribution into a tunneling current component $I_{tun,\nu}$ for $E_{cc,\upsilon} \le E \le E_{th,\upsilon}$ and a thermionic current component $I_{th,\nu}$ for $E > E_{th,\upsilon}$. Each current component is then characterized by an individual transmission probability.

Most often in the literature, the energy-dependent thermionic transmission probability $T_{th,\nu}$ is replaced with an energy-independent averaged transmission probability $T_{th,avg,\upsilon}$ for which the thermionic current integral has a closed form solution

$$I_{th,\upsilon} = \frac{4q^2}{h} V_T T_{th,avg,\upsilon}(\zeta(E_{th,\upsilon}, E_{f,s}) - \zeta(E_{th,\upsilon}, E_{f,d})) \quad (7)$$

where ζ is given by

$$\zeta(E_{th,\upsilon}, E) = \ln\left[1 + \exp\left(-\frac{E_{th,\upsilon} - E}{k_b T}\right)\right]. \quad (8)$$

Note that $T_{th,avg,\upsilon} < 1$ even in the quantum ballistic limit due to momentum mismatch [16].

If tunneling through the Schottky barriers and all quantum ballistic mechanisms are neglected, the thermionic current exclusively defines the total current. This restriction is also known as the *thermionic limit*. There, the current control energy $E_{cc,\nu}$ is identical to $E_{th,\nu}$. These assumptions are not realistic for state-of-the-art CNTFET technologies.

Due to its simplicity, the thermionic limit has been assumed in several compact models, e.g. in [10][14][15]. These thermionic transport models comprise (*i*) the thermionic transport equation depending on ψ_{cc}, (*ii*) a pseudo-bulk description of the tube charge Q_q and (*iii*) a simplified Poisson equation describing the bias dependence of ψ_{cc}. Most models either differ in the description of the bias-dependence of ψ_{cc} (e.g a polynomial fit as in [10]) or in the approximation of the non-explicitly solvable semi-classical charge density [15]. However a detailed analysis of these models reveals a poor description of the small-signal quantities compared to both numerical device simulations and experimental data. Fig. 4 shows experimental results [17] for the transconductance of an 50 nm long CNTFET and the simulated transconductances according to [18].

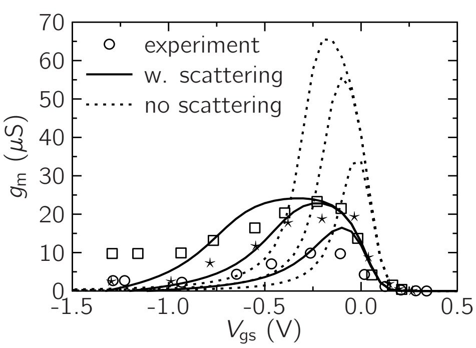

Fig. 4: Measured [17] and simulated transconductance of an ST CNTFET with and without scattering for V_{DS}/V = -0.1, -0.2, -0.3 . (The bias dependence of ψ_{cc} was adjusted to match the $\max(g_m)$).

To improve the agreement between measurements and model prediction, scattering mechanisms due to acoustic and optical phonons are considered. It was found [14] that incoherent scattering processes can be considered in equation (4) by a suitably defined energy-dependent transmission probability $T_{scat}(E) = l_{eff}(E)/(l_{eff}(E) + L_{ch})$ where L_{ch} is the length of the CNT and l_{eff} is an effective mean-free path which depends on the mean-free paths due to optical and acoustic phonons. However, the energy-dependent T_{scat} demands a numerical evaluation of the integral in (4) which is not an option for compact models. To reduce the computational burden, an averaged scattering transmission probability $T_{scat,avg}$ such as proposed in [18] can be used (see Fig.

4). In this approach, the bias-independent contact resistances R_{cs} and R_{cd} are often used to match experimental results instead of a more detailed description of channel and contact physics.

However, even if scattering slightly improves the DC characteristics, the impact of scattering on the charge distribution and thus delay times has not been considered by compact models so far although the impact is expected to be significant as shown in [19].

The physical basis on which a suitable compact model should rely on has not been clarified so far. Thus, it is not astonishing that the experimental results [17] for an 50 nm long ST CNTFET are taken as a reference for several contradicting modeling approaches. The comparison with experimental data reveals the compact models based on the thermionic transport limit to inadequately represent current CNTFETs. Especially the simplified charge calculation and the assumption of fully transparent metal contacts appear to be doubtful, which motivates to extend the transport models towards tunneling phenomena.

4.3 Tunneling based transport models

To match simulation results to experimental data even for relaxed device dimensions and non-intentionally doped spacers, the contribution of the tunneling current component $I_{tun,\upsilon}$ through the Schottky barriers (see Fig. 1b) and thus the tunneling transmission probability $T_{tun,\upsilon}$ needs to be modeled. The methods published so far can be classified into the integral approach, the integrand approach and the transmission approach.

1. The *integral approach* is the most physics-based level to develop a model. A suitable description of the energy-dependent transmission probability T_{υ}, for example by using the WKB approximation, is established in order to gain an analytical expression for the integrand of the tunneling current component in (4). Yet, the expression does not allow an analytical solution of the integral and, thus, has to be solved numerically which is not an option for compact models. However, most transmission based models published so far, such as [20][21], pursue this approach. Fig. 3b compares the transmission probability calculated with a ballistic Schrödinger-Poisson solver and the results of the WKB approximation. The deviations are obvious (more information can be found in [12]). In addition, for a semi-analytical description, the Schottky-barrier related potential is very often approximated with an exponential or a triangular shape. Both approximations are shown to be valid only for idealized coaxial or back gate CNTFETs. Since the transmission probability and, thus, the current are highly sensitive to the shape, the application of these results to current CNTFET structures is questionable.

2. The *integrand approach* deals with the simplification of the complete integrand in such a way that the whole integral can be solved analytically. A rather accurate but very complicated approach is given in [22] while a crude step-function approach was published in [23][24][25] which leads to discontinuities in the small-signal transistor characteristics. Note also that the approach proposed in [22] is incomplete and a verification at the transistor level is still missing.

3. In the *transmission approach*, the energy dependent transmission probability is replaced by an energy independent averaged transmission probability which allows for an analytical solution of the tunneling current integral. While the integral and the integrand approach are rather physics-based, the transmission approach may be used for a semi-empirical model.

Simulations suggest that tunneling based models potentially better match the experimental results for the DC current. However, none of the physics-based models proposed so far has been verified for the small- and large-signal transistor characteristics which are essential for analog circuit simulation. In addItion, the impact of Schottky barriers on the carrier distribution has commonly been ignored. In [25], a first attempt to include tunneling related phenomena in the charge calculation is sketched but the approximations are too crude and lead to kinks in the small-signal quantities.

4.4 Semi-empirical models

Due to the difficulties physics-based approaches are currently faced with, improved model formulations or even new approaches need to be found that are suitable for analog RF applications. Therefore, semi-empirical models such as the one published in [3] have to be used for circuit design. Compared to the compact models discussed above, the agreement to experimental results is significantly improved. Especially the description of the small-signal characteristics is quite good. Selected comparisons are shown in Fig. 5 for a ST CNTFETs with 800 nm channel length.

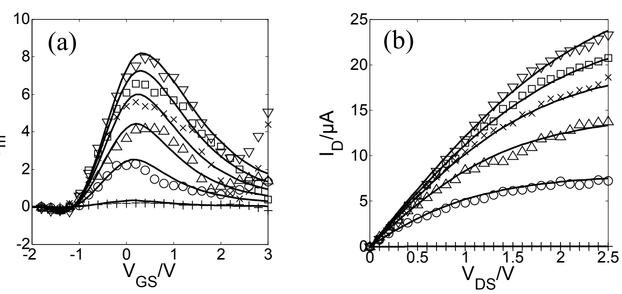

Fig. 5: Experimental results of an 800 nm long ST CNTFET: (a) g_m for V_{DS}/V = 0.05, 0.4, 0.75, 1, 1.45, 1.8 and (b) output characteristic for V_{GS}/V = -1, 0.5, 1, 1.5, 2, 3 .

4.5 Extension towards MT CNTFETs

Due to the deficiencies of current physics-based compact models, it is not feasible to apply these models to MT CNTFETs where even more non-ideal phenomena need to be considered. Even so an extension of [14] towards MT transistors (as needed for analog HF circuits) was proposed in [26], it is restricted to aligned identical tubes. A physical description of production-type MT CNTFETs is challenging due to the MT related phenomena described earlier. A large-signal geometry scalable semi-empirical model for MT CNTFETs, which has already successfully been employed for RF analog circuit design and which shows excellent agreement with experimental results, was sketched in [3] along with experimental results for MT transistors.

4.6 Conclusion

Most compact models for CNTFETs are dedicated to digital circuit design. In this paper, their applicability to analog circuit design was studied and deficiencies were pointed out. However, since a suitable compact model for MT CNTFETs is required for evaluating and exploring the performance of production-like CNTFET processes, semi-empirical models appear presently to be the only viable option for analog circuit design.

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