Simulation of Removal of Surface-State-Related Lag and Current Slump in GaAs FETs

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ABSTRACT

Two-dimensional transient analysis of field-plate GaAs MESFETs is performed by considering surface states in the region from the gate toward the drain. Quasi-pulsed current-voltage curves are derived from the transient characteristics. It is shown that drain lag and current slump due to surface states are reduced by introducing a field plate longer than the surface-state region. Dependence of lag phenomena and current slump on field-plate length and SiO_2 passivation layer thickness is also studied, indicating that the lags and current slump can be completely removed in some cases.

Keywords: GaAs FET, current slump, surface state, drain lag, gate lag

1 INTRODUCTION

In compound semiconductor FETs, slow current transients are often observed even if the drain voltage or the gate voltage is changed abruptly [1,2]. This is called drain lag or gate lag, and undesirable for circuit applications. Slow transients indicate that dc and RF current-voltage (*I-V*) curves become quite different, resulting in lower RF power available than that expected from dc operation [3]. This is called current slump. These phenomena occur due to surface states and/or bulk traps [1-5]. Experimentally, the introduction of field plate like Fig.1 is shown to reduce the lags and current slump [3,6,7]. However, few simulation studies on field-plate structures have been made, although GaN-based FETs with bulk traps are studied [8]. In previous works [9,10], we made two-dimensional simulation of field-plate GaAs MESFETs including surface states, and found that surface-related lags and current slump can be reduced by introducing a field plate. In this work, we have further studied the field-plate effects and found that in some cases surface-state-related lags and current slump could be completely removed.

2 PHYSICAL MODELS

Figure 1 shows a device structure analyzed in this study. The gate length L_G is typically set to 0.3 μm. The gate electrode extends on to SiO_2 passivation layer. This is called a field plate. The field-plate length L_{FP} is varied as a parameter. The thickness of SiO_2 layer d is also varied. Relatively high densities of surface states are considered only at the drain edge of the gate region. This situation can occur after the device has been stressed or due to device degradation. Here the length of surface-state region L_S is set to 0.4 μm from the gate edge toward the drain. As a surface-state model, we adopt Spicer's unified defect model, and assume that the surface states consist of a pair of a deep donor and a deep acceptor. The surface states are assumed to distribute uniformly within 5 Å from the surface, and their densities (N_{SD}, N_{DA}) are typically set to 6×10^{19} cm^{-3} (3×10^{12} cm^{-2}). As for their energy levels, the following case based on experiments is considered as in a previous work [11]: E_{SD} = 0.87 eV, E_{SA} = 0.7 eV, where E_{SD} is the energy difference between the bottom of conduction band and the deep donor's energy level, and E_{SA} is the energy difference between the deep acceptor's energy level and the top of valence band. In this case, the deep-acceptor surface state mainly determines the surface Fermi level, and it acts as a hole trap.

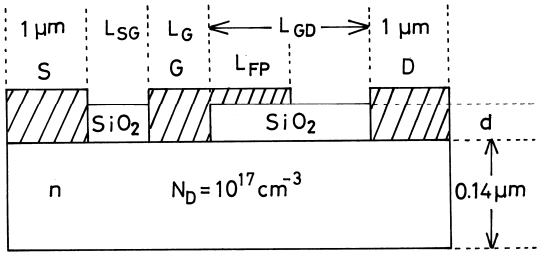


Figure 1: Device structure analyzed in this study.

Basic equations to be solved are Poisson's equation including ionized deep-level terms, continuity equations for electrons and holes which include carrier loss rates via the deep levels, and rate equations for the deep levels [10-12]. These are expressed as follows.

1) Poisson's equation

$$\nabla^2\psi = -\frac{q}{\varepsilon}(p - n + N_D + N_{Di} + N_{SD}^{+} - N_{SA}^{-}) \qquad (1)$$

2) Continuity equations for electrons and holes

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \bullet J_n - (R_{n,\mathrm{SD}} + R_{n,\mathrm{SA}}) \quad (2)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \bullet J_p - (R_{p,\mathrm{SD}} + R_{p,\mathrm{SA}}) \quad (3)$$

where

$$R_{n,\mathrm{SD}} = C_{n,\mathrm{SD}} N_{\mathrm{SD}}^{+} n - e_{n,\mathrm{SD}} (N_{\mathrm{SD}} - N_{\mathrm{SD}}^{+}) \quad (4)$$

$$R_{n,\mathrm{SA}} = C_{n,\mathrm{SA}} (N_{\mathrm{SA}} - N_{\mathrm{SA}}^{-}) n - e_{n,\mathrm{SA}} N_{\mathrm{SA}}^{-} \quad (5)$$

$$R_{p,\mathrm{SD}} = C_{p,\mathrm{SD}} (N_{\mathrm{SD}} - N_{\mathrm{SD}}^{+}) p - e_{p,\mathrm{SD}} N_{\mathrm{SD}}^{+} \quad (6)$$

$$R_{p,\mathrm{SA}} = C_{p,\mathrm{SA}} N_{\mathrm{SA}}^{-} p - e_{p,\mathrm{SA}} (N_{\mathrm{SA}} - N_{\mathrm{SA}}^{-}) \quad (7)$$

3) Rate equations for the deep levels

$$\frac{\partial}{\partial t}(N_{\mathrm{SD}} - N_{\mathrm{SD}}^{+}) = R_{n,\mathrm{SD}} - R_{p,\mathrm{SD}} \quad (8)$$

$$\frac{\partial}{\partial t} N_{\mathrm{SA}}^{-} = R_{n,\mathrm{SA}} - R_{p,\mathrm{SA}} \quad (9)$$

where N_{SD}^{+} and N_{SA}^{-} are ionized densities of surface deep donors and surface deep acceptors, respectively. C_n and C_p are electron and hole capture coefficients of the deep levels, respectively, e_n and e_p are electron and hole emission rates of the deep levels, respectively, and the subscript (SD, SA) represents the corresponding deep level.

These equations are put into discrete forms and are solved numerically. We have calculated the drain-current responses when the drain voltage V_{D} (and the gate voltage V_{G}) is changed abruptly.

3 SLOW CURRENT TRANSIENTS (DRAIN LAG)

Figure 2 shows calculated drain-current responses of GaAs MESFETs considering surface states when V_{D} is lowered abruptly from 10 V to V_{Dfin}, where V_{G} is kept constant at 0 V. Here, the surface-state density is 3×10^{12} cm^{-2}, and the surface-state length L_{S} is 0.4 μm.. Fig.2(a) shows a case without a field plate, and Fig.2(b) shows a case with a field plate (L_{FP} = 1 μm). The thickness of SiO_2 layer d is 0.1 μm. In both cases, the drain current I_{D} remains at a low value for some periods (10^{-10} – 10^{-1} s) and begins to increase slowly, showing drain lag behavior. It is understood that the drain current begins to increase when the deep-acceptor surface states begin to capture holes [12] or emit electrons. It is clearly seen that the change of drain current is smaller for the case with a field plate when comparing for the same V_{Dfin}, indicating that the drain lag is smaller for the field-plate structure. Without a field plate, a barrier for electrons is formed at the gate-to-drain region during the transients [10], and hence I_{D} becomes very low. On the other hand, with a field plate, the potential under the field plate is almost flat and a small barrier is seen at the field-plate edge, and hence I_{D} becomes larger, resulting in smaller drain lag.

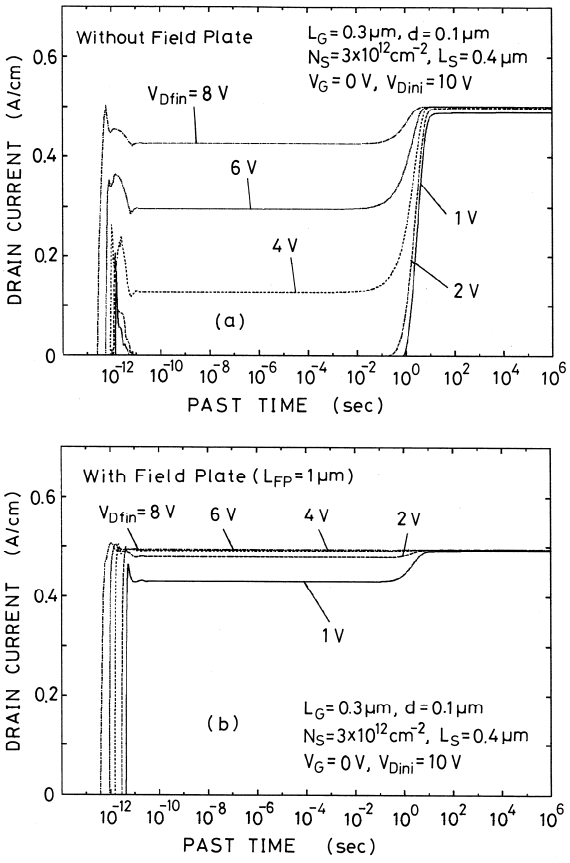
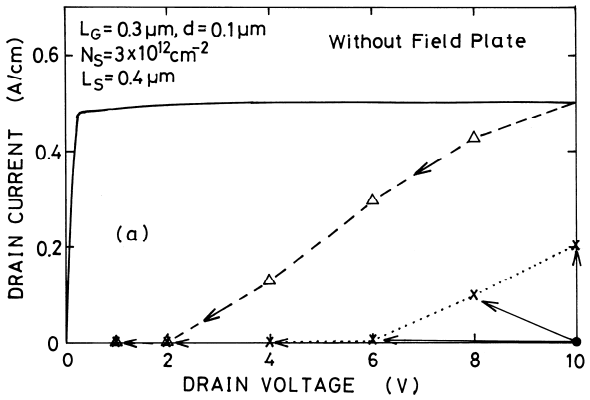


Figure 2: Calculated drain-current responses of GaAs MESFETs when V_{D} is lowered abruptly from 10 V to V_{Dfin} and V_{G} is kept constant at 0 V. d = 0.1 μm. N_{S} = 3×10^{12} cm^{-2} and the surface-state layer length L_{S} is 0.4 μm. (a) Without field plate, (b) with field plate (L_{FP} = 1 μm).

4 PULSED *I-V* CURVES AND CURRENT SLUMP

Next, we have calculated a case when V_{G} is also changed from an off point. V_{G} is changed from the threshold voltage V_{th} to 0 V, and V_{D} is lowered from 10 V to V_{Don} (on-state drain voltage). V_{th} is defined here as a gate voltage where the drain current I_{D} becomes 5×10^{-3} A/cm. The characteristics (not shown here) become similar to those shown in Fig.2, although some transients arise when only V_{G} is changed (gate lag). From these turn-on characteristics, we obtain a quasi-pulsed *I-V* curve.

In Fig.3, we plot by (x) the drain current at $t = 10^{-8}$ sec after V_{G} is switched on, with V_{Don} (V_{D}) as a parameter. Fig.3(a) shows the case without a field plate, and Fig.3(b) shows the case of the field-plate structure (L_{FP} = 1 μm, d = 0.1 μm). These curves are regarded as quasi-pulsed *I-V* curves with pulse width of 10^{-8} sec. Without a field plate,



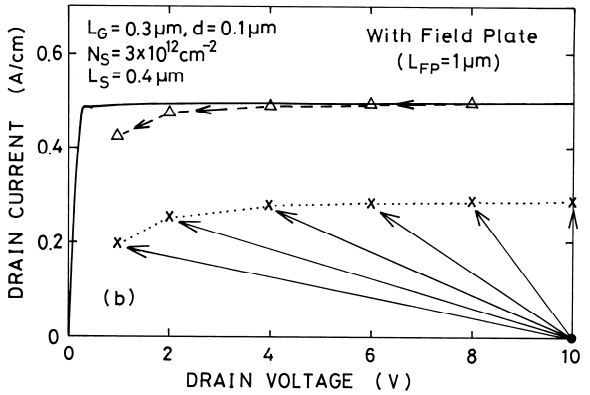


Figure 3: Steady-state *I-V* curves (V_G = 0 V; solid lines) and quasi-pulsed *I-V* curves (Δ, x) of GaAs MESFETs. d = 0.1 μm. N_S = 3x10^{12} cm^{-2} and L_S is 0.4 μm. (a) Without field plate, (b) with field plate (L_{FP} = 1 μm). (Δ): Only V_D is changed from 10V (t = 10^{-8} s), (x): V_D is lowered from 10 V and V_G is switched on from V_{th} to 0 V (t = 10^{-8} s).

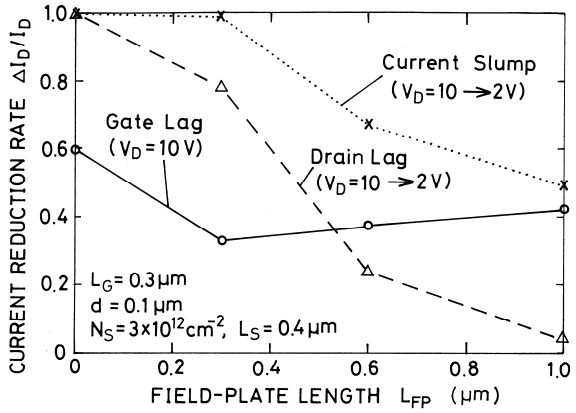


Figure 4: Current reduction rate $\Delta I_D/I_D$ due to current slump, drain lag or gate lag, with field plate length L_{FP} as a parameter. d = 0.1 μm. N_S = 3x10^{12} cm^{-2} and L_S = 0.4 μm.

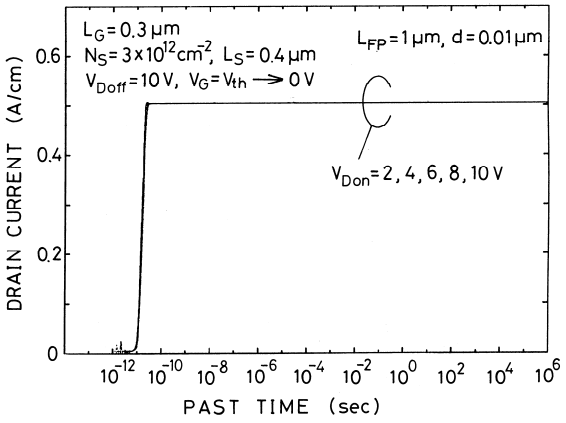


Figure 5: Calculated turn-on characteristics for L_{FP} = 1 μm and d = 0.01 μm when V_D is lowered abruptly from 10 V to V_{Don} and V_G is changed from V_{th} to 0 V. N_S = 3x10^{12} cm^{-2} and L_S = 0.4 μm.

the pulsed *I-V* curve lies significantly lower than the steady-state *I-V* curve (solid line), indicating current slump and gate lag behavior. In Fig.3, we also plot another pulsed *I-V* curve (Δ), which is obtained from Fig.2 (when only V_D is changed), indicating large drain lag without a field plate. However, from Fig.3(b), we can definitely say that by introducing a field plate, the current slump and drain lag are greatly reduced, although the gate lag is not so reduced. The reduction in drain lag is contributing to reducing the current slump in this case.

5 FIELD-PLATE PARAMETER DEPENDENCE AND REMOVAL OF CURRENT SLUMP

We have next studied dependence of lag phenomena and current slump on the field-plate length L_{FP} and on the SiO_2 layer thickness d.

Figure 4 shows drain current reduction rate $\Delta I_D/I_D$ (ΔI_D: current reduction, I_D: steady-state current) due to current slump, drain lag or gate lag, with L_{FP} as a parameter. Here, d = 0.1 μm. The values of current slump and drain lag are taken from the case when V_D is lowered from 10 V to 2 V. Here the length of surface-state region is set to 0.4 μm from the gate edge toward the drain. It is seen that when L_{FP} becomes longer than the length of surface-state region, the drain lag and current slump decrease. They become smaller for longer L_{FP} However, the gate lag is not so dependent on L_{FP}.

Figure 5 shows calculated turn-on characteristics when L_{FP} = 1 μm and d is very thin (0.01 μm). Here, V_D is lowered from 10 V to V_{Don} and V_G is changed from V_{th} to 0 V. Surprisingly, the slow current transients disappear, indicating that the lags and current slump are completely removed in this case.

Figure 6 shows current reduction rates $\Delta I_D/I_D$ due to current slump, drain lag, or gate lag, with d as a parameter. As d becomes thin, the lags and current slump are reduced, and they are completely removed when d becomes thinner

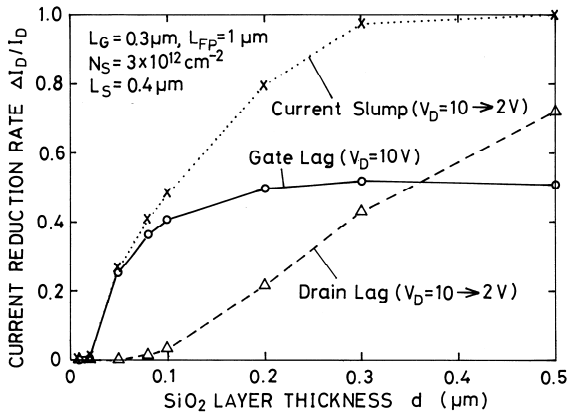


Figure 6: Current reduction rate $\Delta I_D/I_D$ due to current slump, drain lag or gate lag, with SiO_2 layer thickness d as a parameter. L_{FP} = 1 μm. N_S = 3x10^{12} cm^{-2} and L_S = 0.4 μm.

than 0.02 μm. This may be because surface-state effects are completely masked by the field plate. When d is thin, the gate parasitic capacitance becomes a problem, but this removal of current slump is still a very interesting result.

6 CONCLUSION

Two-dimensional transient simulations of the field-plate GaAs MESFETs have been performed by considering surface states. Quasi-pulsed *I-V* curves have been derived from the transient characteristics.

We have studied the case where relatively high densities of surface states exist only at the drain edge of the gate region. It has been shown that the drain lag and current slump due to surface states are reduced by introducing a field plate. The current slump has been shown to become smaller for a longer field-plate length.

It has also been shown that the lags and current slump can be completely removed when the field-plate length becomes longer than the surface-state length and the SiO_2 layer becomes very thin, because in this case the surface-state effects are completely masked by the field plate.

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