

Investigation of Frequency Dependent Noise Performance Metrics for Gate Electrode Work function Engineered Recessed Channel MOSFET

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ABSTRACT

This paper discusses the noise assessment, using ATLAS device simulation software, of a gate electrode work function engineered recessed channel (GEWE-RC) MOSFET involving an RC and GEWE design integrated onto a conventional MOSFET. Furthermore, the behavior of GEWE-RC MOSFET is compared with that of a Recessed Channel(RC) MOSFET having the same device parameters. This paper thus optimizes and predicts the feasibility of a novel design, i.e., GEWE-RC MOSFET for high-performance applications where device scaling and noise reduction are a major concern. The noise metrics taken into consideration are: minimum noise figure, optimum source impedance and noise conductance. The statistical tools auto correlation and cross correlation are also analysed owing to the random nature of noise.

Keywords: ATLAS device simulator, minimum noise figure, optimum source impedance, noise conductance, GEWE-RC MOSFET, correlation

1 INTRODUCTION

To achieve higher speeds and packing densities, the world has witnessed the miniaturization of the basic MOS device structure. Today, CMOS technology has an established place in the design of multi-gigahertz communication circuits. This is due to the continuing down-scaling of MOS devices, which improves their RF performance characteristics. As the MOSFET is shrunk, some unwanted effects are observed such as punchthrough, hot carrier injection, noise in RF range, dependence of threshold voltage on channel dimensions, DIBL and other short channel effect(SCEs) which affect the performance of the device in a negative manner. As MOSFET device sizes and signal levels are aggressively scaled down, the low-frequency noise (LFN) properties become increasingly important. This is because the signals are no longer significantly higher than the LFN, especially since the LFN level increases significantly as the device's size is scaled down. As the issue of noise becomes increasingly important in deep-submicron MOSFETs, it is necessary to be able to accurately measure and model the noise parameters of MOSFET to fully characterize its noise performance.

2 ANALYSING GEWE-RC MOSFET

Recessed MOSFETs are known to alleviate many of the SCEs[1,2]. This has been achieved by separating the source and drain(S/D) regions by a groove. Several studies have reported that the potential barrier formed at each recess corner is responsible for suppressing the SCEs, hot-carrier effects and punch-through. It is also responsible for the degradation of current driving capability and threshold voltage. The recessed MOSFET, however, in conjunction with dual material gate (DMG) architecture [3,4], named as Gate electrode work function engineered recessed channel (GEWE-RC) MOSFET, as shown in figure 1, enhances drain current characteristics, average carrier velocity and suppresses SCEs, thereby proving superior to the recessed channel(RC) MOSFET. GEWE-RC MOSFET has the work function of metal gate1 towards the source i.e. controlling gate (M1) greater than that of metal gate 2 towards the drain i.e. screening gate (M2) i.e. $\phi_{M1} > \phi_{M2}$. With this DMG architecture, the step potential profile, due to different work functions of two metal gates, ensures reduction of SCEs and screening of the channel region under the controlling gate from the drain potential variations. Thus, the average electric field in the channel is enhanced, improving the electron velocity near the source and, hence, the carrier transport efficiency. Some past works on this device such as RF analysis[5] and linearity analysis[6] have been done before and they suggest the feasibility[7] of this model. The work has been complied in Chaujar *et al.* The GEWE-RC MOSFET [8] (figure 1) considered in this study which integrates the potential benefits of Recessed MOSFETs with DMG architecture also enhances the noise performance of scaled devices in comparison to the RC MOSFET.

For the purpose of the above mentioned noise analysis, structural design parameters, such as gate length, junction depth, substrate doping, gate metal work function and thickness of the oxide layer are tuned in GEWE-RC MOSFET to attain the best performance. The noise metrics examined are the minimum noise figure, NF_{min}, and optimum source admittance, Y_{opt}, or impedance, Z_{opt}, as they are important in the design of low noise RF circuits such as low noise amplifiers (LNA) and mixers. But as noise is a random phenomenon, the statistical tools auto correlation and cross correlation are also analysed to support the simulation results obtained.

All simulations have been performed using ATLAS device simulation software. The models activated in simulation comprise the inversion layer Lombardi CVTmobility model along with the Shockley– Read–Hall (SRH) and Auger recombination models for minority carrier recombination. Furthermore, we adopt the hydrodynamic energy transport model which includes the continuity equations, momentum transport equations, energy balance equations of the carriers and Poisson’s equation [9]. It can model the non-local transport phenomenon, and hence presents a higher accuracy than the drift–diffusion method. The quantum corrections have not been taken into account because the quantum mechanical effects become significant when the gate oxide thickness is below 30 Å or 3 nm. In our study, since the gate oxide thickness is 3 nm, the quantum corrections are ignored [10].

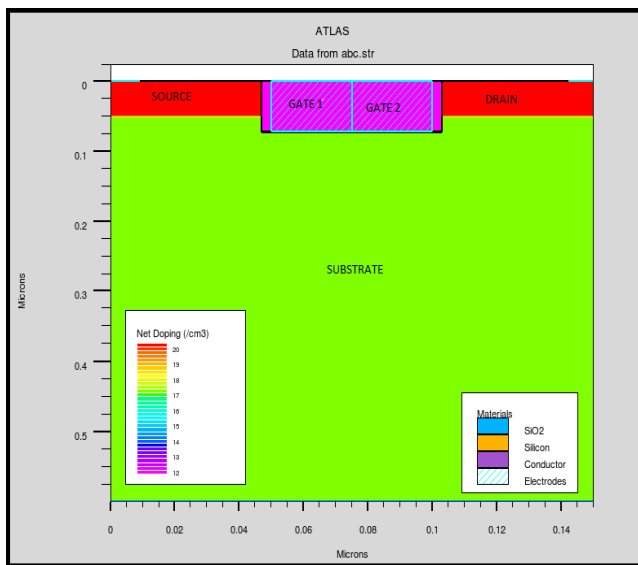


Figure 1: The architecture of GEWE-RC MOSFET made using ATLAS device simulator. Device width (W)= 1 μm , Groove depth (d)= 70 nm, $N_A = 1 \times 10^{17} \text{ cm}^{-3}$, Source/Drain doping, $N_D = 1 \times 10^{20} \text{ cm}^{-3}$, $t_{\text{ox}} = 3 \text{ nm}$, $\epsilon_{\text{ox}} = 3.9$. Work function (ϕ_{M2}) = 4.1eV for GEWE-RC and for RC, (ϕ_{M2}) = 4.77eV and (ϕ_{M1}) = 4.77eV for both. Effective channel length for both is 96nm. Source/Drain junction depth is 50nm.

3 NOISE ANALYSIS

Noise performance of a modern small-area MOS devices is dominated by random telegraph signal (RTS) fluctuations[11],[12]. Their origin is the capture and subsequent emission of charge carriers at discrete trap levels near the Si–SiO₂ interface[13],[14]. For deep-submicrometer devices, the number of traps with energy within a few kT close to the surface Fermi level is small[12]. Both, the number of traps and their position over the channel are random variables[13],[14]. Traps located in the gate oxide near the interface to the silicon capture and reemit some of the carriers responsible for the current

flowing between the source and the drain of the device[14]. Hence, the carrier transport efficiency is hampered. Now let us see the individual parameters taken into consideration.

3.1 Minimum noise figure

The Figure 3 explains the effect of frequency on the noise behavior of GEWE-RC MOSFET and the RC MOSFET designs (with the same specifications), in terms of minimum noise figure. Results clearly reveal that noise figure for the both of these MOSFETs increases with the increasing frequency. Although, it is noteworthy that the noise figure for the RC MOSFET and GEWE-RC MOSFET at 1000Hz is 0.275065dB and 0.000212794dB respectively. Although, at higher frequencies the value of NFmin for both the devices is almost the same. This observation can be mainly attributed to the work function difference of the gates in the GEWE-RC architecture, due to which a step-potential is introduced in the channel[15]. There exists a screening of the channel region from the drain induced variations due to which the number of carriers entering the channel remains comparatively less varied[15]. Also, the vertical electric field is reduced due to which the trapping of the carriers near the Si-SiO₂ reduces, which results in the improved carrier transport efficiency[16].

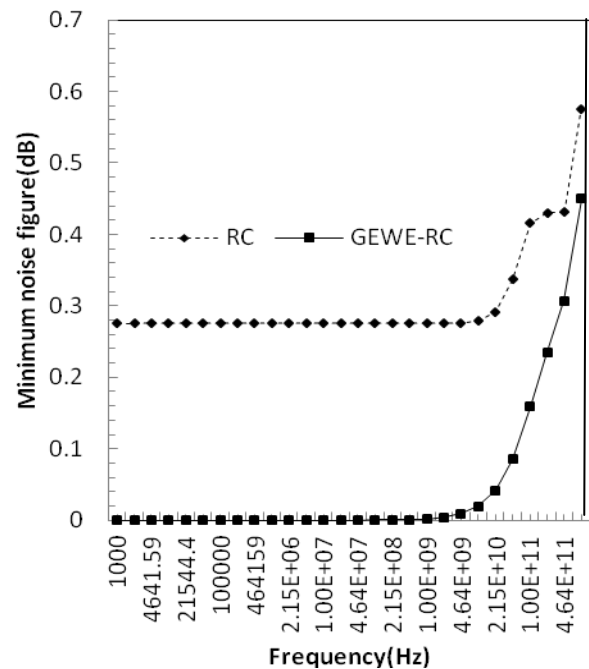


Figure 3: Minimum Noise Figure

3.2 Optimum source impedance

The Figure 4 gives the behavior of optimum source impedance ($Z_{\text{OPT}} = R_{\text{OPT}} + jX_{\text{OPT}}$) with respect to frequency.

Because the oxide layer acts as a dielectric, there is essentially never any current between the gate and the channel during any part of the signal cycle[17]. As the oxide thickness is being continuously shrunk due to the scaling of the MOSFET, the MOSFET should have a large source impedance to avoid destruction by electrostatic charges. In the Figure 3 it can be vividly seen that optimum impedance for GEWE-RC MOSFET is much higher than that of the RC MOSFET.

3.3 Noise Conductance

Spectral density of a noise current generator is measured in conductance units at a specified frequency. It can be seen from Figure 5 that the noise conductance for GEWE-RC is less than that of RC MOSFET. This can be mainly attributed to the lower DIBL in the DMG structure incorporated along with RC in GEWE-RC MOSFET.

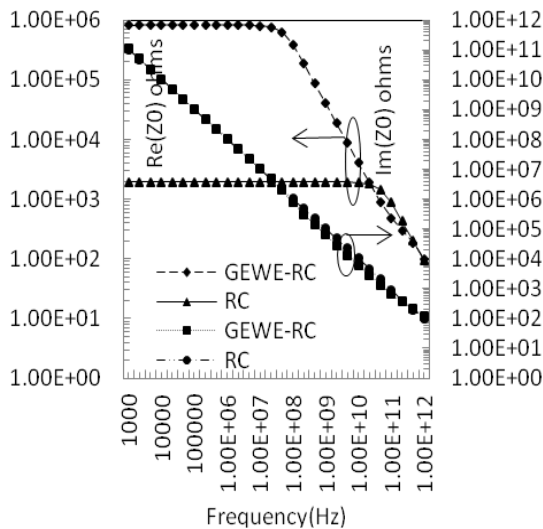


Figure 4: Optimum source Impedance

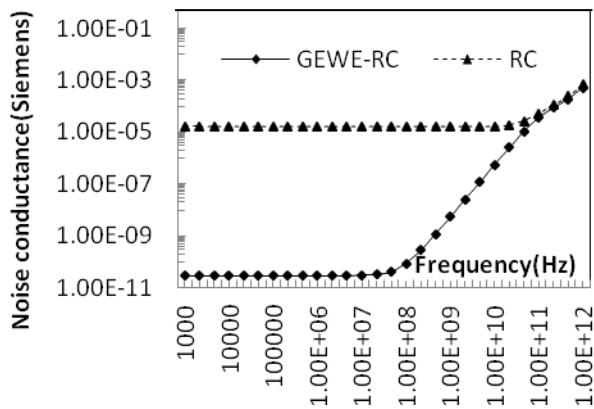


Figure 5: Noise Conductance

3.4 AutoCorrelation and CrossCorrelation

The MOSFET is considered as a two port device(Figure 6) i.e. the noise induced at the gate is separated from the MOSFET and is depicted by V1 and the noise received at the output is replaced by a voltage V2[18]. Since noise is a random phenomenon, some statistical analysis is indispensable for this research. Thus, the autocorrelation and cross correlation of the voltages at the two ports of the devices are compared. From the above analysis it can be inferred that surface scattering with the Si-SiO₂ gate interface is noticeably reduced in the GEWE-RC MOSFET because of a lower vertical electric field. Therefore, isotropic scatterings present a reduced prevalence in this device[19]. Thus it can be concluded that the mean free path (λ) of carriers crossing the channel as a function of the frequency is much larger than in the conventional transistor[15]. This reduced influence of isotropic scatterings implies that the scattering mechanisms are not so effective in breaking the correlation between gate and drain current, which leads to higher cross correlation(i.e. V1.V2*) between them[20]. Figure 7 depicts such behaviour. Auto correlation is the cross correlation of a signal with itself. As can be seen by Figure 8, there is higher auto correlation between the input(i.e. V1.V1*) and output voltages(i.e. V2.V2*) in GEWE-RC MOSFET than the RC MOSFET depicting lesser intrinsic noise in the former than the latter.

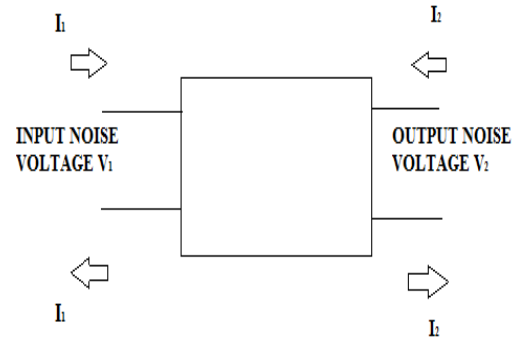


Figure 6: MOSFET as a two port device where the input noise is replace by a voltage V1 and the the noise received at the output is replaced by V2

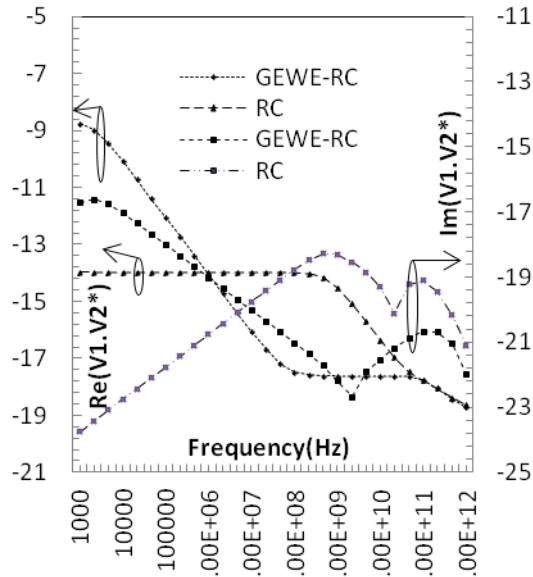


Figure 7: Cross Correlation

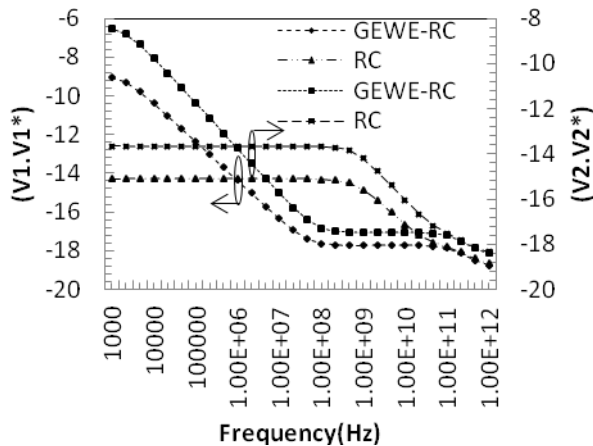


Figure 8: Auto Correlation

4 CONCLUSION

As shown in this work, from the analysis of the microscopic noise sources and dynamic performance of the devices; GEWE-RC MOSFET exhibits superior noise performance in comparison to its RC counterpart. It can be concluded that the reduced induced gate noise and stronger cross correlation are responsible for the noticeable improvements observed in the intrinsic minimum noise figure. Hence, proving its potency for low power, low noise and low supply voltage applications. Lower noise figure and higher optimum source impedance pertained by the

GEWE-RC architecture strengthens the idea of using it for such applications, thereby giving a new opening for usage in RF applications.

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