Understanding and Modeling Quasi-Static Capacitance-Voltage Characteristics of Organic Thin-Film Transistors

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ABSTRACT

We have investigated the quasi-static capacitance-voltage (C-V) characteristics of pentacene-based organic thin-film transistors (OTFTs). Beside the hysteresis which is in accordance with previously reported I-V characteristics of OTFTs, the measured C-V characteristics include a plateau which cannot be observed in the C-V characteristics of the well-known metal-oxide-semiconductor (MOS) capacitor. In order to explain this phenomenon, the measured structure is investigated as a combination of three parts, each with particular C-V characteristics: i) C_{ox} is the oxide capacitance due to the Au electrode deposited on the gate oxide, ii) C_{MOS} is the MOS capacitance of the sandwich structure made of Si^{++}, gate oxide, pentacene and Au electrode, iii) C_{peri} is the capacitance of the peripheral pentacene film. We speculate that the observed plateau stems from surface charges with a density of 2.87 x 10^{12} cm^{-2}. Using this conception we developed a behavioral circuit model in PSpice which can be dimensioned according to the actual geometry of the device. The model is improved with an RC network in order to take into account the dynamic behavior as well as hysteresis effects. Simulation results obtained with this model are in very good accordance with the measurements.

Keywords: modeling, pspice, organic thin-film transistors, quasi-static capacitance-voltage characteristics, hysteresis

1 INTRODUCTION

Operation principles of organic thin-film transistors (OTFTs) have been shown to be similar to conventional TFTs made from inorganic semiconductors, except some important differences such as, for example, charge carrier injection, formation of the conducting channel and charge carrier conduction [1]. Although further insight into these phenomena can be gained through capacitance-voltage (C-V) analysis of OTFTs, such investigations are scarce in the literature. Consequently, in this communication, we report a detailed study on the quasi-static C-V characteristics of OTFT structures. In addition, a PSpice behavioral circuit model for C-V characteristics of OTFTs will be presented which contributes to the efforts to develop a compact model for organic thin-film transistors.

2 MIS DEVICE FABRICATION

Figure 1 shows the cross-section of a typical bottom-gate top-contact OTFT. Since the structure is symmetric with respect to the A-A' axis, for the sake of simplicity, C-V analyses are performed on MIS (metal-insulator-semiconductor) devices which represent one half of the OTFT structure (Fig. 2). Devices are fabricated on highly doped Si^{++} wafers with 300 nm thermally grown oxide, which act as gate electrode and gate oxide, respectively. The organic semiconductor pentacene is purchased from Sigma–Aldrich and a 50 nm thin-film is thermally evaporated at 10^{-6} mbar through a shadow mask. A 20 nm gold (Au) layer is sputtered through another shadow mask to finish the fabrication.

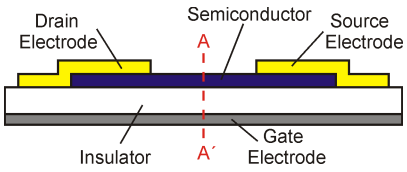

Figure 1: Cross-section of a bottom-gate top-contact OTFT.

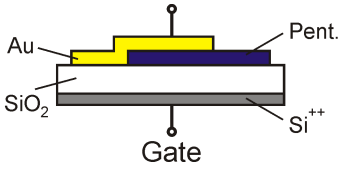

Figure 2: Cross-section of the MIS structure fabricated for C-V measurements (not to scale).

3 QSCV CHARACTERISTICS

Quasi-static C-V measurements are performed in air with an Agilent 4156C semiconductor parameter analyzer. Slow voltage sweep rates in the range of 100 mV/s are utilized to conduct reproducible C-V measurements which fulfill quasi-static characterization requirements. The characteristics show a clear hysteresis behavior (Fig. 3a). This is in accordance with the previously reported I-V characteristics from different research groups where

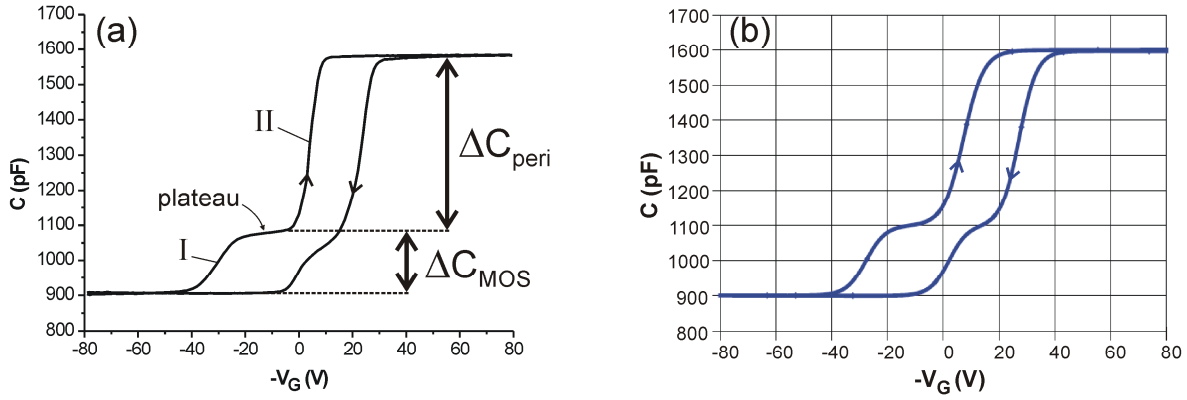

Figure 3: C-V characteristics of the MIS structure in Fig. 2. a) Measured, b) simulated in PSpice.

measurements are performed on OTFT structures fabricated similar to Fig. 1 [2]. However, unlike the C-V characteristics of well-known metal-oxide-semiconductor (MOS) capacitor, the curve in Fig. 3a includes a plateau. In order to explain this phenomenon, the MIS device in Fig. 2 is investigated as a combination of three parts, each with particular C-V characteristics: i) C_{ox} is the oxide capacitance due to the Au deposited on the gate oxide (Fig. 4a), ii) C_{MOS} is the MOS capacitance of the sandwich structure made of Si^{++}, gate oxide, pentacene and Au (Fig. 4b), iii) C_{peri} is the capacitance of the peripheral pentacene film which does not have any contact to the Au electrode (Fig. 4c). Since these partial capacitances are in parallel, the C-V characteristic of the overall structure is the sum of the individual characteristics of C_{ox}, C_{MOS} and C_{peri} [3]. C_{ox} is not voltage-dependent and it remains constant during a gate voltage (V_G) sweep (Fig. 4a). C_{MOS} has its maximum when the semiconductor film (SF) is in accumulation ($-V_G > V_{th}$) and its minimum when the SF is depleted ($-V_G < V_{th}$) (Fig. 4b). And C_{peri} depends on the gate voltage as follows. When the SF is not in accumulation ($-V_G < V_{th}$), there are not any mobile charge carriers in the SF and the capacitance is equal to zero (Fig. 4c). However, when the SF is in accumulation ($-V_G > V_{th}$), capacitance increases since charge carriers accumulate at the SF-insulator interface. In order to check the validity of the above assumptions and to determine how the C-V characteristics depend on the physical device dimensions, devices with different SF thicknesses (d_p) and peripheral SF lengths (l_p) are fabricated. Results given in Fig. 5 reveal that ΔC_{peri} causes the increase in the C-V characteristics which is marked with II in Fig. 3a. Similarly, Fig. 6 shows that the plateau in the C-V characteristics stems from ΔC_{MOS}. It should be noted that the plateau is observable due to the fact that the increase of C_{MOS} (marked with I in Figs. 3a and 4b) occurs at a voltage $V_{th\_MOS} \approx 40$ V which differs from the voltage $V_{th\_peri} \approx 0$ V at which C_{peri} increases (marked with II in Figs. 3a and 4c). Although these voltages (V_{th_MOS}, V_{th_peri}) are expected to be approximately the same, we speculate that the shift of the gate voltage in the C-V characteristics stems from surface charges [4]. According to the Ref. 4 we have calculated that a surface charge density of 2.87 x 10^{12} cm^{-2}, which is in the order of the densities reported in the literature [5], suffices to cause the 40 V shift in the C-V characteristics of C_{MOS}.

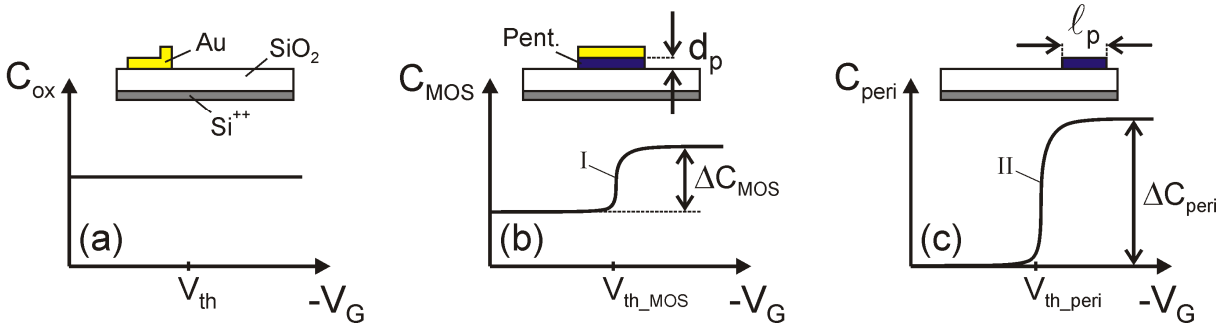

Figure 4: C-V characteristics of the partial capacitances of the structure given in Fig. 2. a) Oxide capacitance C_{ox}, b) MOS capacitance C_{MOS}, c) capacitance of the peripheral pentacene film C_{peri}, where d_p is the thickness of the pentacene film, l_p is the length of the peripheral pentacene film and V_{th} is the threshold voltage.

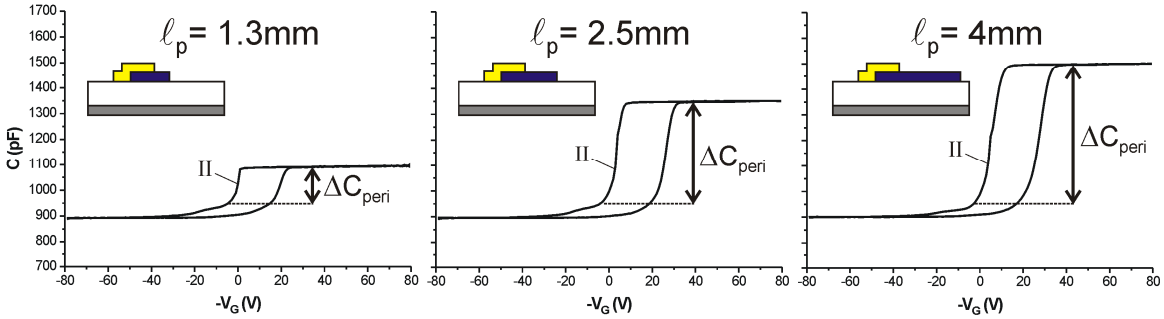

Figure 5: Measured C-V characteristics of test structures with different peripheral pentacene film lengths (l_p). With increasing l_p, the maximum of the overall capacitance increases due to the increasing ΔC_{peri}. However, the minimum capacitance which is proportional to the area of the Au electrode and inversely proportional to the pentacene film thickness is constant.

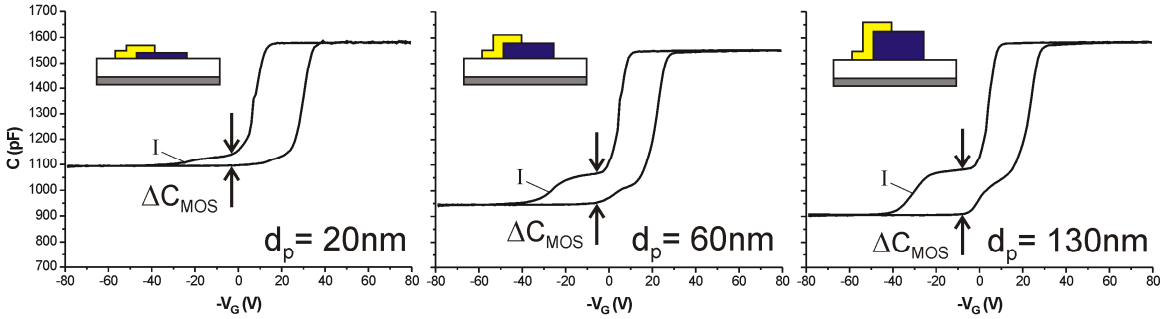

Figure 6: Measured C-V characteristics of test structures with different pentacene film thicknesses (d_p). With increasing d_p, the minimum of the overall capacitance decreases due to the decreasing ΔC_{MOS}. However, the maximum capacitance which is proportional to the area is constant. The little fluctuation in the maximum capacitance value is caused by shadow mask tolerances.

4 BEHAVIORAL MODELING

Understandings of the previous section are utilized to implement an analog behavioral PSpice model of the observed C-V characteristics. In order to reproduce the different C-V characteristics given in Fig. 4, the model basically consists of three tunable capacitances (C_{ox}, C_{MOS}, C_{peri}) in parallel where each capacitance can be dimensioned according to the actual geometry of the device to be simulated (Fig. 7). C_{ox} is voltage-independent, therefore, its implementation is straightforward. Yet, C_{MOS} and C_{peri} are voltage-dependent nonlinear capacitances which are not found in the standard PSpice libraries. A voltage-controlled current-source (VCCS) can be employed for this purpose (Fig. 8) where the current is set to be proportional to the derivate of the voltage as in the well-known capacitance equation

$$I = \frac{dQ}{dt} = C\frac{dV}{dt}. \qquad (1)$$

In order to attain the correct capacitance behavior, the equation of the VCCS is manipulated with a nonlinear

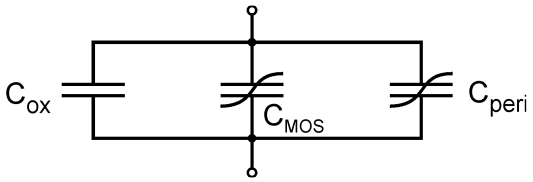

Figure 7: Block diagram of the behavioral model for the C-V characteristics of the MIS structure given in Fig. 2

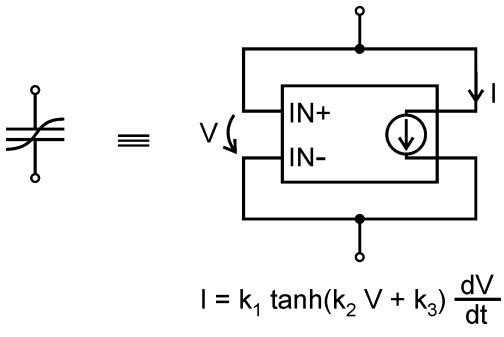

Figure 8: Nonlinear capacitor behavior is modeled with a VCCS in PSpice. See manuscript for details. k_1, k_2, k_3 are constants which are used as fit parameters.

multiplier. A hyperbolic tangent function is used for this purpose since this function resembles to a good extent the measured C-V behavior. In order to take into account the dynamic behavior as well as hysteresis effects, the model is improved with an RC network in accordance with Refs. 6 and 7 (Fig. 9). A comparison between the measured and the simulated C-V characteristics in Fig. 3 validates the introduced PSpice model.

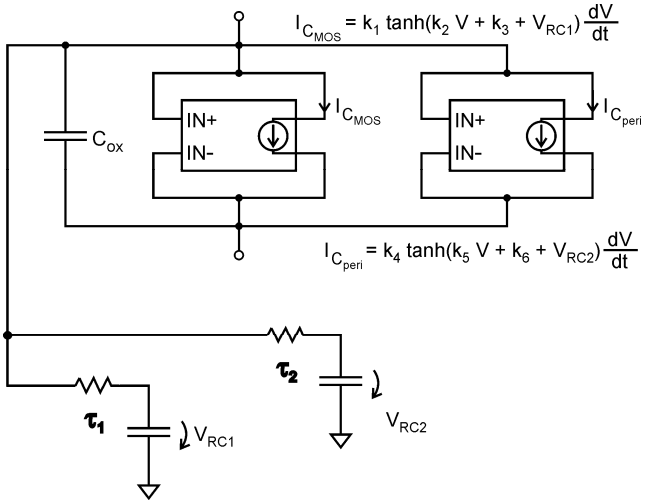

Figure 9: PSpice behavioral model for the C-V characteristics of the MIS structure given in Fig. 2

5 CONCLUSION

In this report we have presented an investigation on the quasi-static C-V characteristics of organic thin-film transistors. We have shown that irregularities such as hysteresis and threshold voltage shift in the I-V characteristics of OTFTs can be further investigated and better understood through C-V characterization. We have introduced a PSpice behavioral model which allows the C-V characteristics of OTFTs to be simulated including transient effects. An important advantage of the model is its ability to be dimensioned according to the actual geometry of the device to be simulated - e.g. C_{MOS} can be excluded for bottom-contact devices. This is an important contribution to develop a compact model for organic thin-film transistors which is a prerequisite for the realization of more complex OTFT circuitry.

REFERENCES

[1] H. Sirringhaus, Adv. Mater. 17, pp. 2411-2425, 2005.

[2] M. Egginger, S. Bauer, R. Schwödiauer, H. Neugebauer and N. S. Sariciftci, Monatshefte für Chemie - Chemical Monthly 140, pp. 735-750, 2009.

[3] K. D. Jung, C. A. Lee, D. W. Park, B. G. Park, H. Shin and J. D. Lee, Device Research Conference 64th, pp.139-140, Jun. 2006.

[4] S. M. Sze and K. Ng. Kwok, Physics of Semiconductor Devices, pp. 223-225, Wiley, New York, 2007.

[5] C. S. Suchand Sangeeth, P. Stadler, S. Schaur, N. S. Sariciftci and R. Menon, J. Appl. Phys. 108, 113703, 2010.

[6] C. Ucurum, H. Siemund and H. Goebel, IEEE Portable-Polytronic 2008, vol., no., pp.1-3, Aug. 2008.

[7] C. Ucurum, R. M. Meixner and H. Goebel, WCM, NSTI Nanotech Conference, Houston, May 2009.