On Statistical Variation of MOSFETs Induced by Random-Discrete-Dopants and Random-Interface-Traps

Yiming Li*, Hsin-Wen Su, Chieh-Yang Chen, Hui-Wen Cheng, Yu-Yu Chen, and Han-Tung Chang

Parallel and Scientific Computing Laboratory, Department of Electrical and Computer Engineering,
National Chiao Tung University, 1001 Ta-Hsueh Road, Hsinchu 300, Taiwan
*Tel: +886-3-5712121 ext. 52974; Fax: +886-3-5726639; E-mail address: ymli@faculty.nctu.edu.tw

ABSTRACT

In this work, we statistically study characteristic fluctuation of 16-nm-gate high-κ/metal gate (HKMG) MOSFETs by random-discrete-dopants (RDDs) inside silicon channel and random-interface-traps (RITs) at high-κ/silicon interface. Randomly generated devices with three-dimensional (3D) RDDs inside device channel and 2D RITs at HfO_2/Si interface are incorporated into quantum-mechanically corrected 3D device simulation. Device characteristics, as influenced by different degrees of fluctuation, are discussed in relation to RITs near the source and drain ends, and RDDs near the device channel surface and silicon substrate. Characteristic fluctuations are affected to different extents by the random combinatorial RDDs and RITs. Nonlinearly correlated RDDs and RITs further violate the statistical assumption of independent identical distributions between the RDDs- and RITs-induced random variables. Consequently, for the studied 16-nm-gate HKMG MOSFETs, the threshold voltage fluctuation induced by the combined RDs and ITs is less than their statistical sum due to local interaction of surface potentials resulting from the RDDs and RITs simultaneously. In contrast to RDDs fluctuation, the screening effect of device's inversion layer cannot effectively screen potential's variation resulting from RITs; thus, devices still have noticeable gate capacitance characteristic fluctuation under high gate bias.

Keywords: Drain-induced barrier lowering; Subthreshold swing; Random-interface-traps; random-discrete-dopants; near source; near channel surface; random position effect; fluctuation; MOSFETs

1 INTRODUCTION

Process variation and random fluctuation are severe challenges [1-3] in scaling down silicon-based devices continuously according to Moore's law. Emerging fluctuation sources [4-5] consists of random dopant fluctuation (RDF) [6-8] and interface trap fluctuation (ITF) [9-11] which degrade device characteristic significantly.

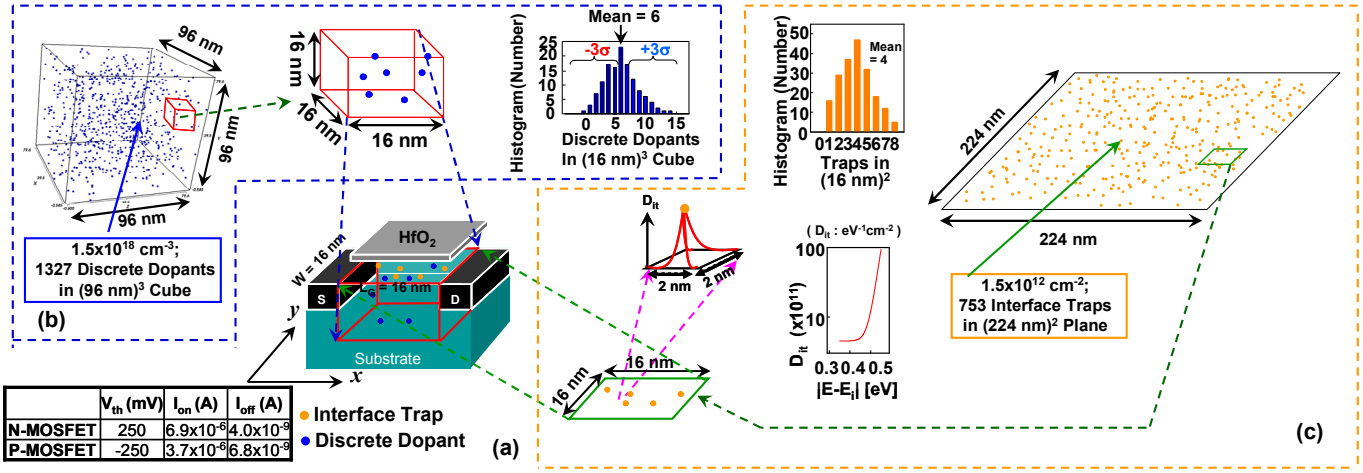
In this work, characteristic fluctuations, induced by RDDs and RITs, of 16-nm-gate HKMG MOSFET device are studied by using an experimentally calibrated 3D device simulation. Because RITs exhibit a spike of local energy barrier and trap majority carriers, for the N-MOSFETs, electrons are trapped by acceptor-like traps and result in high V_{th}, all fluctuated drain current-gate voltage (I_D-V_G) curves are thus shifted right. The fluctuation of drain current is pronounced resulting from random ITs at sub-threshold regions; however, it is reduced as V_G increases due to inversion charges filling the interface states and minimizing their impact; nevertheless, the existing RITs at the HfO_2/Si interface weaken the screening effect, in contrast to RDF. For the same number of RDDs (or RITs), simulated device samples indicate that RDDs near the channel surface (or RITs near the source end), respectively, locally alter potential barrier significantly; consequently, devices possess rather different drain-induced barrier lowering (DIBL) fluctuations. The finding further indicates: $\sigma V_{th,\text{"RDDs and RITs"}} < (\sigma^2 V_{th,RDDs} + \sigma^2 V_{th,RITs})^{0.5}$, where the $\sigma V_{th,\text{"RDDs and RITs"}}$ is the combined "RDDs and RITs"-induced threshold voltage fluctuation, $\sigma V_{th,RDDs}$ and the $\sigma V_{th,RITs}$ are only the RDDs- and ITs- induced threshold voltage fluctuations, respectively. Such overestimation on the threshold voltage fluctuation is the basic statistical assumption of independent identical distributions for only the RDDs- and RITs-induced random threshold voltages does not hold at all. Similarly, the impact of combined RDDs and RITs on the σI_{on}, σI_{off}, and σC_G is estimated and discussed.

2 STATISTICAL 3D DEVICE SIMULATION

To assess the most critical impact of RDDs and RITs on device's characteristics, the studied devices have the same channel length and device width of 16 nm, a TiN/HfO_2 gate stack, and an effective oxide thickness of 0.8 nm, as shown in Fig. 1(a). The nominal DC characteristic of the devices is calibrated with ITRS roadmap for low operating power, where the threshold voltage of the 16-nm-gate N-MOSFETs is equal to 250 mV. Note that all adopted material properties, device settings, and mobility model follow our recent experiment and simulation studies [1-2,4]. Figures 1(b) and (c) illustrate the simulation settings of RDDs and RITs on the tested device. The simulation method of RDF and ITF follows the details appearing in our earlier work [1-2]. Hundreds device samples are generated for statistical variation calculations.

3 RESULTS AND DISCUSSION

Figure 2 shows the off-state (V_D = 0.8 V and V_G = 0 V) potential distributions and on-state (V_D =V_G = 0.8 V)



	V_{th} (mV)	I_{on} (A)	I_{off} (A)
N-MOSFET	250	6.9×10^{-6}	4.0×10^{-9}
P-MOSFET	-250	3.7×10^{-6}	6.8×10^{-9}

Figure 1. (a) The quantum mechanically simulated 3D device structure with the settings of (b) RDDs and (c) RITs for statistical variations.

current densities over the channel surface of the simulated devices; as shown in each lower left plot, the devices are fluctuated by 8 RDDs locating inside the silicon channel below the channel surface (Fig. 2(a)), 4 random RITs at HfO_2/silicon interface (Fig. 2(b)), and 12 combined RDDs and RITs (Fig. 2(c)).

As shown in the upper plots of surface potentials from the source (S) to drain (D), the RDDs, RITs, and "RDDs and RITs" possess different spikes of barrier owing to their local interactions. The locally generated spike of barriers may reduce transport carrier's velocity and energy, and thus obstruct their conduction, where the corresponding current densities are shown in the lower right plots. The combined RDDs and RITs even complicate the nonlinear interaction of surface potentials.

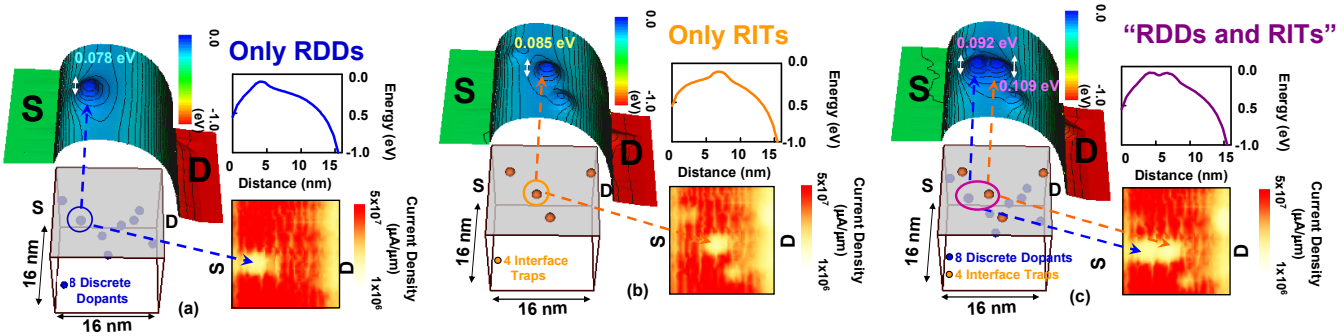


Figure 2. The fluctuated surface potential and current density induced by only (a) RDDs, (b) RITs, and (c) the combined RDDs and RITs.

The impacts of space charge and interaction between RD and IT are also explored. For example, the potentials in the case <1'>, the case <2'>, and the case <3'> are fluctuated by 1 IT locating at HfO_2/silicon interface, 1 RD and 1RD at 2 and 4 nm below the surface, respectively, as shown in Fig. 3(a). If we consider the effect of combined <1'> and <2'> (denoted as <1'> + <2'>) with a line-up location at near the channel surface , the potential difference is increased due to the interaction between RD and IT, as shown in Fig. 3(b), where the difference values of corresponding potential are summarized in Table 1. Replaced the IT by a RD at very similar place near the channel surface, the increment of potential difference is more obvious owing to the increase of space charges, as shown in the combined <2'> and <3'> (denoted as <2'> + <3'>). It implies that the coupling effect induced by RD and RD is larger than the interaction between RD and IT. Besides, the calculated V_{th} of the cases <1'> + <2'> and <2'> + <3'> are 0.312 and 0.362 V which are different from their statistical sum: the case of <1'> and <2'> is: $(0.196^2+0.304^2)^{0.5} = 0.362$ V and the case of <2'> and <3'> is $(0.304^2+0.298^2)^{0.5} = 0.426$ V. It confirms that the fluctuation sources should be considered at the same time in order to get proper fluctuation estimations.

Figures 4(a) and (b) show the DIBL versus the number of RDDs and RITs, respectively. For devices having the same number of RDDs or RITs; Fig. 4(c) shows that RDDs away from the channel surface have relatively smaller DIBL degradation, compared with the RDDs near the channel surface, as shown in Fig. 4(e). Figure 4(d) shows that RITs away from the source end have relatively smaller DIBL degradation, compared with RITs near the source end (Fig. 4(f)).

Figure 5 reports the asymmetric and skewed gate capacitance-gate voltage (C_G-V_G) induced by only RDDs, only RITs, and the combined RDDs and RITs. Figure 6(a) lists the σV_{th} of N- and P-MOSFETs, where the relative errors indicate individual estimation on RDDs or RITs is

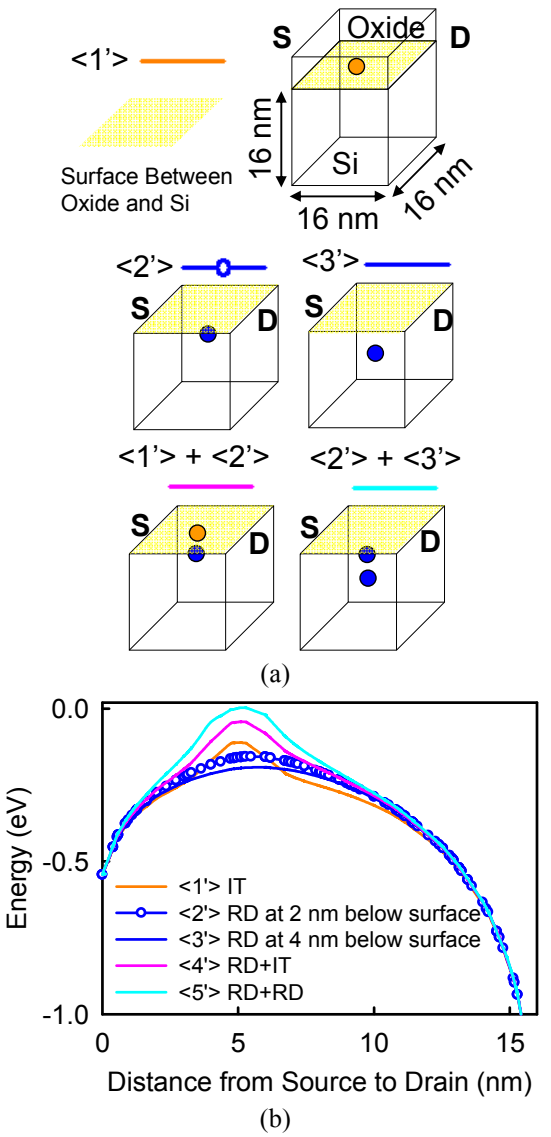


Figure 3. (a) The schematics of channel and (b) corresponding potentials fluctuated by 1 IT at the interface (the case <1'>), 1 RD located 2 (the case <2'>) and 4 (the case <3'>) nm below the surface, the combined case of <1'> + <2'>, and the case of <2'> + <3'>, respectively. All surface potentials are extracted from the source end to the drain end, where the RDs and/or IT are locating at x = 5 nm.

insufficient to explain the σV_{th}. Plot of the I_{off}-I_{on} of the N- and P-MOSFETs is shown in Fig. 6(b), where each symbol indicates the result induced by the combined RDDs and RITs. The inset shows the scatter relationship. Plot of the σC_G of the N-MOSFETs induced by RDDs, RITs and combined RDDs and RITs under V_G = 0.4 V and 0.8 V are shown in Fig. 6(c).

4 Conclusions

We have explored the local interaction of surface potentials among the RDDs, RITs, and combined RDDs and RITs for the 16-nm-gate CMOS devices. Due to randomly positioned charges resulting from the RDDs and RITs in the 16-nm-gate CMOS devices, the "RDDs and RITs" has an enlarged peak of localized spikes compared with the results of individual RDDs and RITs, respectively. It implies that the local interaction and nonlinear coupling effects should be considered simultaneously for the RDF and ITF in emerging HKMG CMOS devices.

Acknowledgement

This work was supported in part by Taiwan National Science Council (NSC) under Contract NSC-100-2221-E-009-018 and by tsmc, Hsinchu, Taiwan under a 2011-2012 grant.

References

[1] Y. Li, H.-W. Cheng, Y.-Y. Chiu, C.-Y. Yiu, and H.-W. Su, "A Unified 3D Device Simulation of Random Dopant, Interface Trap and Work Function Fluctuations on High-κ/Metal Gate Device," in: *IEEE International Electron Devices Meeting Technical Digest*, pp. 5.5.1 - 5.5.4, 2011.

[2]H.-W. Cheng, F.-H. Li, M.-H. Han, C.-Y. Yiu, C.-H. Yu, K.-F. Lee, and Y. Li, "3D Device Simulation of Work-Function and Interface Trap Fluctuations on High-k/Metal Gate Devices," in: *IEEE International Electron Devices Meeting Technical Digest*, pp. 379-382, 2010.

[3] X. Wang, A. R. Brown, B. Cheng, A. Asenov, "Statistical variability and reliability in nanoscale FinFETs," in: *IEEE International Electron Devices Meeting Technical Digest*, pp. 5.4.1 - 5.4.4, 2011.

[4]Y. Li, C.-H. Hwang, T.-Y. Li, and M.-H. Han, "Process-Variation effect, Metal-Gate Work-Function fluctuation, and random-dopant fluctuation in emerging CMOS technologies," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 437-447, 2010.

[5] Y. Li, C.-H. Hwang, and M.-H. Han, "Simulation of Characteristic Variation in 16-nm-Gate FinFET Devices Due to Intrinsic Parameter Fluctuations," *Nanotechnology*, vol. 21, no. 9, 095203, 2010.

Table 1. Summary of V_{th} and potential difference induced by 1 IT at the interface (the case <1'>), 1 RD located at 2 nm (the case <2'>) and 4 nm (the case <3'>) below the surface, the combined case of <1'> + <2'>, and the case of <2'> + <3'>, respectively.

	<1'> 1 IT at the interface	<2'> 1 RD at 2 nm below the surface	<3'> 1 RD at 4 nm below the surface	<1'> + <2'>	<2'> + <3'>
V_{th} (V)	0.196	0.304	0.298	0.312	0.362
Potential Difference (eV)	0.4332	0.3845	0.3522	0.5392	0.5433

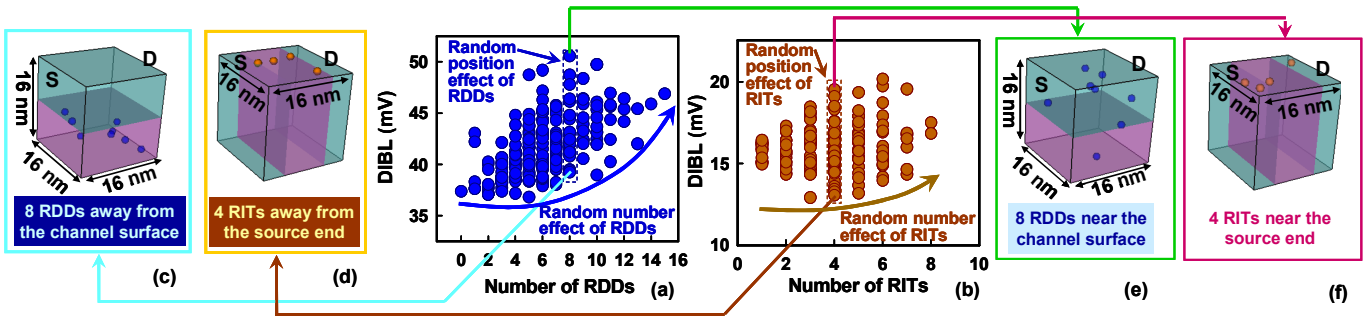


Figure 4. DIBL vs. the number of (a) RDDs and (b) RITs. (c) RDDs away from the channel surface or (d) RITs away from the source end has relatively smaller DIBL degradation, compared with the (e) RDDs near the channel surface or (f) RITs near the source end, for devices having same number of RDDs or RITs.

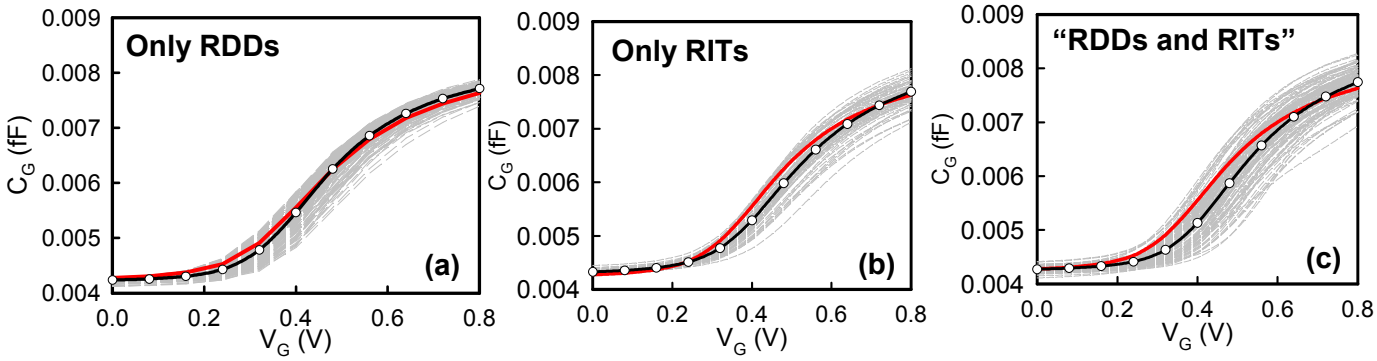


Figure 5. The gate capacitance-gate voltage (C_G-V_G) of N-MOSFETs induced by only (a) RDDs, (b) RITs, and (c) "RDDs and RITs".

	$\sigma V_{th,RDDs}$ mV	$\sigma V_{th,RITs}$ mV	$\sigma V_{th,"RDDs and RITs"}$ mV
N-MOSFETs	43	26.3	45.4
P-MOSFETs	41	27.1	45.1

	$(\sigma^2 V_{th,RDDs}+\sigma^2 V_{th,RITs})^{0.5}$ mV	Error (%)
N-MOSFETs	50.4	+11%
P-MOSFETs	49.1	+8.9%

$$\text{Error (\%)} = \frac{(\sigma^2 V_{th,RDDs}+\sigma^2 V_{th,RITs})^{0.5} - \sigma V_{th,"RDDs and RITs"}}{\sigma V_{th,"RDDs and RITs"}} \times 100\%$$

(a)

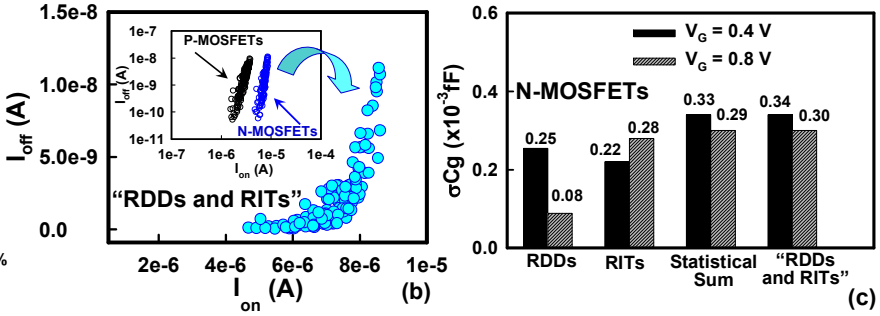


Figure 6. (a) The σV_{th} and (b) the I_{off}-I_{on} induced by "RDDs and RITs" of the N- and P-MOSFETs. (c) The σC_G of N-MOSFETs.

[6] Y. Li, C.-H. Hwang, and H.-M. Huang, "Large-Scale Atomistic Approach to Discrete-Dopant-Induced Characteristic Fluctuations in Silicon Nanowire Transistors," *Physica Status Solidi* (a), vol. 205, no. 6, pp. 1505-1510, 2008.

[7] Y. Li and C.-H. Hwang, "High-Frequency Characteristic Fluctuations of Nano-MOSFET Circuit Induced by Random Dopants," *IEEE Trans. Microwave Theory and Techniques*, vol. 56, no. 12, pp. 2726-2733, 2008.

[8] Y. Li, C.-H. Hwang, and T.-Y. Li, "Discrete-Dopant-Induced Timing Fluctuation and Suppression in Nanoscale CMOS Circuit," *IEEE Trans. Circuits and Systems Part II: Express Briefs*, vol. 56, no. 5, pp. 379-383, 2009.

[9] Y. Li, H.-W. Cheng, and Y.-Y. Chiu, "Interface Traps and Random Dopants Induced Characteristic Fluctuations in Emerging MOSFETs," *Microelectronic Engineering*, vol. 88, no. 7, pp. 1269-1271, 2011.

[10] N. Ashraf, D. Vasileska, G. Wirth, and P. Srinivasan, "Accurate Model for the Threshold Voltage Fluctuation Estimation in 45-nm Channel Length MOSFET Devices in the Presence of Random Traps and Random Dopants," *IEEE Electron Device Letters* , vol. 32, no. 8, 1044-1046, 2011.

[11] Y. Li and H.-W. Cheng, "Random Interface-Traps-Induced Electrical Characteristic Fluctuation in 16-nm-Gate High-κ/Metal Gate Complementary Metal–Oxide–Semiconductor Device and Inverter Circuit," *Jpn. J. Appl. Phys*. vol. 51, 04DC08 (6 pages), 2012.