Random Work Function Induced DC Characteristic Fluctuation in 16-nm High-κ/Metal Gate Bulk and SOI FinFETs

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ABSTRACT

This work studies the metal gate's work function fluctuation induced DC characteristic fluctuation in the 16-nm bulk and silicon-on-insulator (SOI) fin-type field effect transistor (FinFET) devices using an experimentally calibrated 3D device simulation. The method of localized work function fluctuation simulation enables us to estimate local fluctuations including the nanosized grain's random effects of FinFET with TiN/HfO_2 gate stacks. The result of this study shows characteristic fluctuation strongly depends upon the size of localized nanosized metal grains. The shape of grains does have marginal influence on device's variability.

Keywords: metal gate; random work function; bulk / SOI FinFET; characteristic fluctuation; 3D device simulation.

1 INTRODUCTION

Devices with vertical channel are fascinating and the high-κ metal gate (HKMG) [1-4] stacked fin-type field-effect-transistor (FinFET) is promising technology in sub-22-nm device era. However, metal gate may introduce a random source, so-called the work function fluctuation (WKF) [5-7], due to different surface density in the polarization charges [8-9]. Such uncontrollable grain orientations result in a random work function of metal during growth period. Recently, an average WK technique was reported for sub-65-nm MOSFETs [10-11] and 3D device simulation of localized work function fluctuation (LWKF) has also been reported for the 16-nm planar MOSFETs [5]. Investigation of WKF on characteristic fluctuation of devices with vertical channel is interesting for us to explore FinFET's variability. In this study, based on the experimentally calibrated 3D device simulation, the WKF of emerging TiN/HfO_2 gate stack bulk and SOI FinFETs with AR = 2 is presented and discussed.

2 THE LWKF SIMULATION TECHNIQUE

The devices we studied are the 16-nm-gate FinFETs with amorphous-based TiN/HfO_2 gate stacks and an EOT of 0.8 nm, where both the bulk and SOI FinFETs are with AR = 2, as shown in Fig. 1(a) Different from the average WKF (AWKF) method and compact model approach [10-11], we directly partition the metal gate's area into 80 sub-regions following Gaussian distribution, where the number of generated grains in the top and lateral gates is 16 and 32, respectively. Note that the variation range of TiN grain's size is dozens of nanometers and we first assume it is equal to 4x4 nm^2 according to experimental data [12]. These randomly generated small squares approximate arbitrary shape of grains well. According to metal material's property listed in the table of Fig. 1(b), the TiN has two different orientations: <200> and <111> orientations with 60% and 40% generated probabilities, where the associated probability of WKs are 4.4 eV (blue color) and 4.6 eV (green color) for the n-channel FinFETs [11]. As shown in Fig. 1(b), the average number of total generated <200> orientations are 48 for devices with AR = 2. The studied structures of bulk and SOI FinFETs with each randomly generated 4x4 nm^2 grain orientation from realistic structures are implemented. All generated cases are mapped into the device's gate area of bulk and SOI FinFETs with AR = 2 for the 3D device simulation, respectively, where the V_{th} of nominal case is calibrated to 250 mV for low power applications. For the 3D simulation, a set of 3D quantum-mechanically corrected transport equations are solved numerically [1,5,13]. The accuracy of 3D simulation was experimentally validated in our early work [13]. The adopted DC characteristics of nominal cases of the 16-nm bulk and SOI FinFETs with AR = 2 are shown in the inset table of Fig. 1(b) according to ITRS projection.

3 RESULTS AND DISCUSSION

As shown in Fig. 2(a), the σV_{th} is as a function of device dimension for the studied bulk FinFETs with different TiN grain size. The lines are devices with various minimal grain sizes: 22x22, 13x13, 8x8, 4x4, and 2x2 nm^2, respectively, where the green symbol is an experimental data from [25]. The LWKF simulation is a good agreement with measured data. Moreover, for a device with an arbitrary grain size, the relationship between σV_{th} and channel size is linearly dependent. Thus, from simulation, the σV_{th} is inversely proportional to the square root of device dimension (= effective width times gate length = W_{eff} x L_g), where the W_{eff} is the sum of two times fin height and fin width. From the cumulative probability, the V_{th}'s distribution of SOI FinFET (steep slope) is smaller, compared with the bulk one (gradual slope), as shown in Fig. 2(b), where the green and pink colors indicate statistical data of bulk and SOI FinFETs, respectively. The σV_{th} of SOI FinFET is smaller than that of bulk; for example, the σV_{th} of SOI FinFET induced by the grain size of 4 x 4 nm^2 (about 9.7 mV) is 1.5 times smaller than that of bulk one (about 14.6 mV). The potentials for devices with regular and irregular grain's shapes between the bulk and SOI FinFETs, as shown in Figs. 3(a)-(b), are compared. The inset table of Fig. 3(c) indiciates the V_{th}'s of regular and irregular shapes between the bulk and SOI FinFETs. The V_{th}'s are nearly the same between regular and irregular shapes (within 5% errors).

Fig. 4(a) shows the V_{th}'s distribution versus the number of TiN <200> orientations for the explored bulk and SOI FinFETs with AR = 2. The magnitude of V_{th} of SOI FinFET is smaller than that of bulk one. As the number of <200> orientations increases, the V_{th} is increased. Because the energy band profile is raised in the channel region; consequently, it induces a relatively higher threshold voltage. For the SOI FinFET, most of the random WKs fluctuated V_{th} is smaller than the nominal value of 250 mV owing to suppressing the higher barrier resulting from those high WKs. It implies that the variation of potential profile is

not drastic in the channel region of the SOI FinFET. Besides, we observe that even for the same number of <200> orientations, the threshold voltage exhibits rather different values owing to the nanosized TiN grain's random position effect. Thus, the σV_{th} mainly results from not only the TiN grain's random number but its random position because uncontrollable grain orientations of TiN gate during growth period. Notably, the findings of this study properly explaines the localized nanosized TiN grains induced fluctuation, which is beyond the averaged WK method [10-11]. For a fixed *x* position, in the *y-z* plane of bulk and SOI FinFETs, their cross-section views show that the potential distributions are fluctuated by different WKs locally, as shown in Fig. 4(b). Under the random nanosized grains of TiN gate, the SOI FinFET shows more uniform distribution of potential than that of bulk one. The bulk FinFET exists relatively weak controllability in the bottom of silicon channel so that the DC fluctuation is larger than that of SOI one. Thus, the fluctuation of leakage current of bulk FinFET is serious. For a fixed *y* position, the cross-section view from source to drain (i.e., along the *x-z* direction) of current density distributions are plotted for the bulk and SOI FinFETs, respectively. The current density is strongly governed by the localized WK for both types of devices; furthermore, in the bottom of bulk FinFET's channel, the current density is lower than that of SOI one.

Fig. 5(a) shows the V_{th}'s distribution versus the number of TiN <200> orientation of the bulk FinFET, where the grain size is (4x4) nm^2. As the number of TiN <200> orientation increases, V_{th} is higher. In other words, the potential induced by local WK dominates the value of V_{th}. For example, the case 1 and case 2 with 58 and 40 <200> orientations result in different V_{th} owing to the random grain number effect, where the potential profiles are raised or lowered locally by the high or low WKs, as shown in Fig. 2(b). Even the number of <200> orientation is the same, the position of random grain also induce rather different V_{th}, as shown in the case 3 and case 4, respectively, where the total number of <200> orientation is 46. Similarly, the σV_{th} of SOI FinFET is examined, as shown in Fig. 5(c). Compared with Fig. 5(b), the channel controllability in the bottom of channel is better, though the σV_{th} is strongly fluctuated by number and position effects due to SOI substrate structure, as shown in Fig. 5(d).

We note that the effect of grain size in the 16-nm bulk FinFET has been studied among the minimal grain sizes: 2x2, 4x4, and 8x8 nm^2, respectively. We further compare the fluctuation induced by different minimal grain size of SOI one with AR = 2. Comparison of the magnitude of σV_{th} induced by different grain sizes for both bulk and SOI FinFETs is shown in Fig. 6(a). For both structures, the smaller the grain is, the more fluctuation can be suppressed. About the bulk FinFET, the σV_{th} has 60% reduction from the grain size of 8x8 to 2x2 nm^2. Thus, the σV_{th} of SOI FinFET could be reduced by 23%, compared with the bulk one. The σV_{th} is not only a function of device geometry, but also a function of grain size, as shown in Fig. 6(a), the bulk FinFET possesses large σV_{th} (about 21.5 mV). Through reducing the grain size, the σV_{th} can be suppressed significantly. Figure 6(b) plots I_{off} versus I_{on} with minimal grain sizes: 2x2, 4x4, and 8x8 nm^2 for bulk and SOI FinFETs, respectively. From the plot of I_{on} versus I_{off}, it is clear that the SOI FinFET has relatively smaller I_{off} and larger I_{on} than that of bulk one, where the star and circle symbols indicate bulk and SOI FinFETs. The immunity of fluctuation in the SOI FinFET is superior to the structure of bulk one. And, the table summarizes the σI_{on} and σI_{off} induced by minimal grain sizes: 2x2, 4x4, and 8x8 nm^2 for bulk and SOI FinFETs, respectively.

4 CONCLUSIONS

In this study, we have applied an experimentally calibrated 3D simulation approach, so-called the LWKF simulation method to study the random WK-induced variability in the 16-nm FinFETs with amorphous-based TiN/HfO_2 gate stacks. The random number, position, and size of TiN grains induced rather different characteristic fluctuation which could be reduced by large device geometry and small gain size. And, the error between the regular shap and irregular shap of metal grains is small, which implies we could simulate WKF with regular shape grains using the LWKF simulation.

ACKNOWLEDGEMENT

This work was supported in part by National Science Council (NSC), Taiwan under Contract No. NSC-100-2221-E-009-018 and by tsmc, Hsinchu, Taiwan under a 2011-2012 grant.

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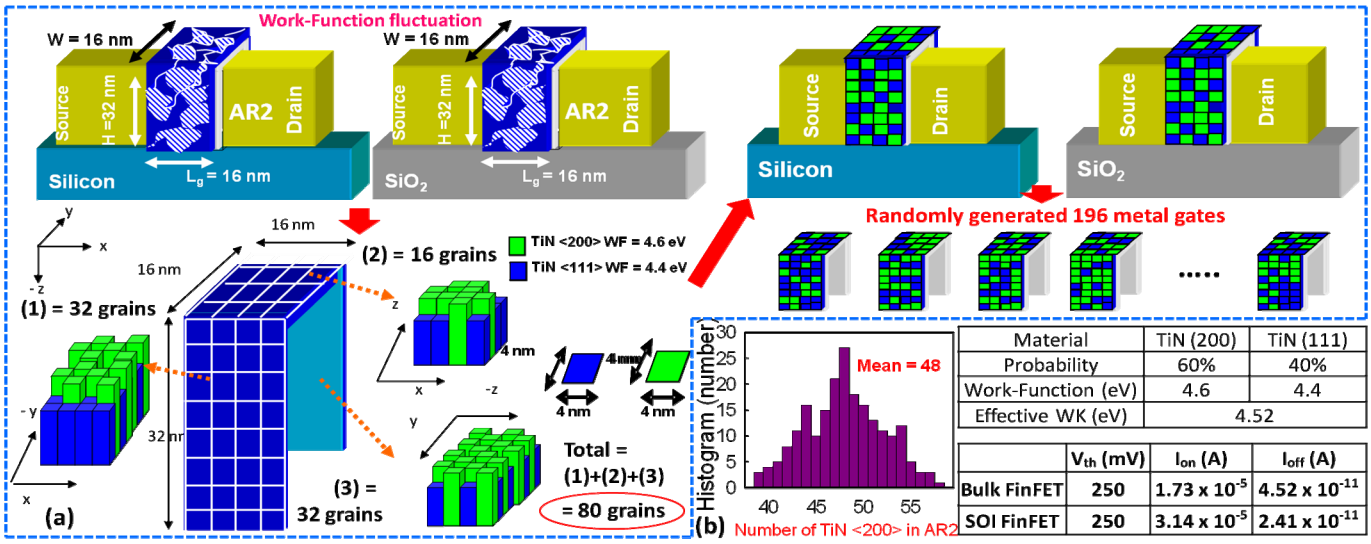


Material	TiN (200)	TiN (111)
Probability	60%	40%
Work-Function (eV)	4.6	4.4
Effective WK (eV)	4.52	

	V_{th} (mV)	I_{on} (A)	I_{off} (A)
Bulk FinFET	250	1.73×10^{-5}	4.52×10^{-11}
SOI FinFET	250	3.14×10^{-5}	2.41×10^{-11}

Figure 1. (a) Schematic plots of the studied bulk and SOI FinFETs with random TiN grains on the top and lateral gates, respectively. There are 80 randomly generated grains in each side of TiN gate for both bulk and SOI FinFETs, where the size of metal grains is assumed to 4x4 nm^2 and green and blue colors represent <200> and <111> orientations. The bulk and SOI FinFETs are with randomly generated 196 metal gates, respectively, for fluctuation estimation. (b) The distribution of totally random generated <200> and <111> orientations, where the material property of TiN and calibrated DC characteristics for the explored bulk and SOI FinFETs are listed in the tables, respectively.

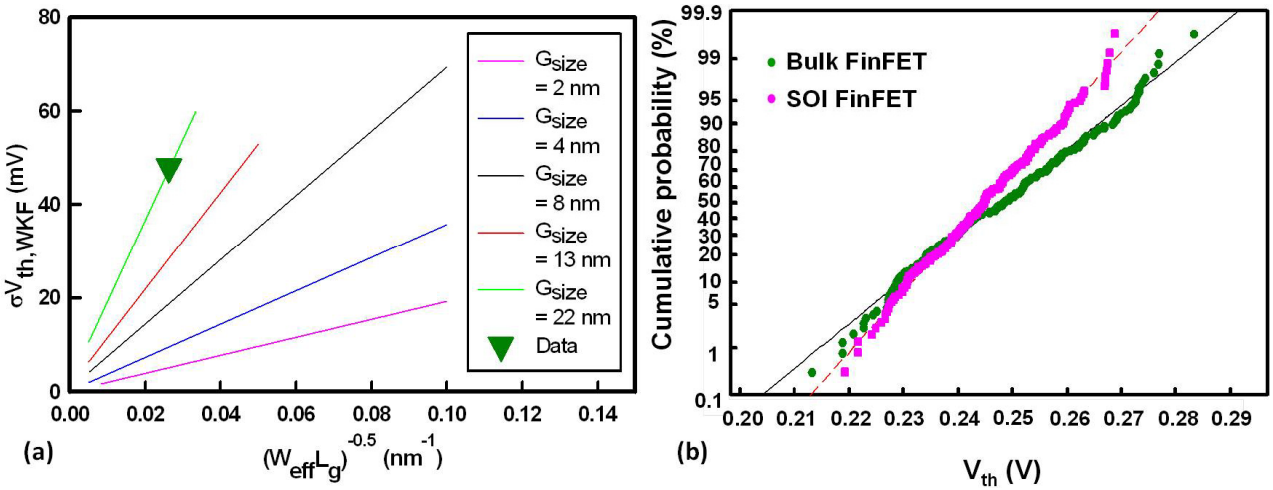
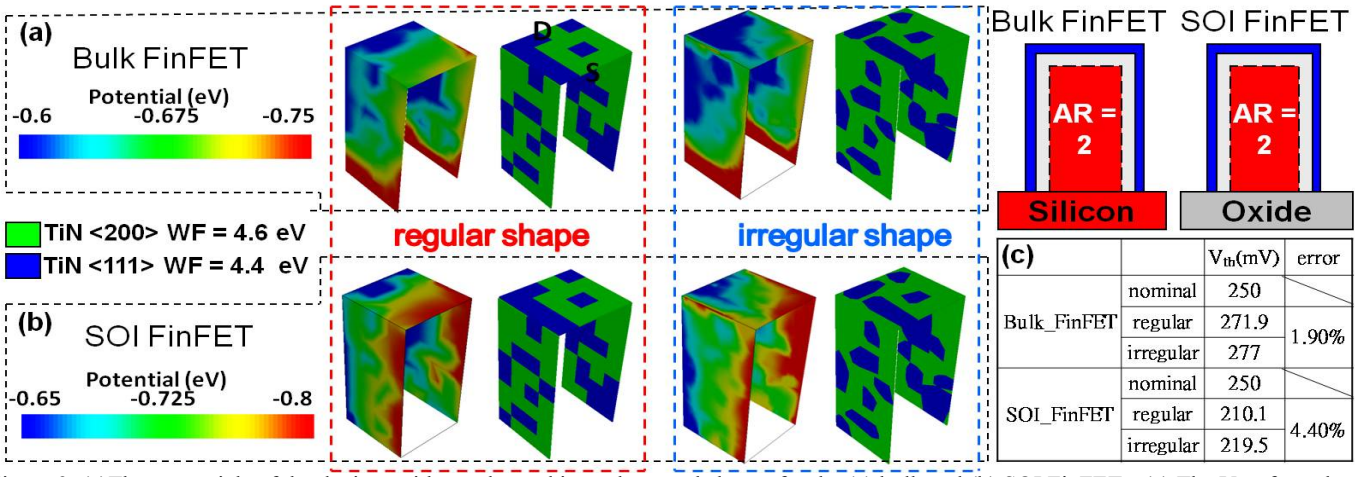


Figure 2. (a) The σV_{th} is as a function of device geometry for the bulk FinFET with respect to the different grain sizes of TiN gate, where the green symbol is an experimental data from [12]. (b) Plot of cumulative probability of the 16-nm bulk and SOI FinFETs, respectively.



(c)		V_{th}(mV)	error
Bulk_FinFET	nominal	250	
	regular	271.9	1.90%
	irregular	277	
SOI_FinFET	nominal	250	
	regular	210.1	4.40%
	irregular	219.5	

Figure 3. (a)The potentials of the devices with regular and irregular metal shapes for the (a) bulk and (b) SOI FinFETs. (c) The V_{th} of regular and irregular shapes between bulk and SOI FinFETs. Both the V_{th}'s are silimar and the errors are within 5% .

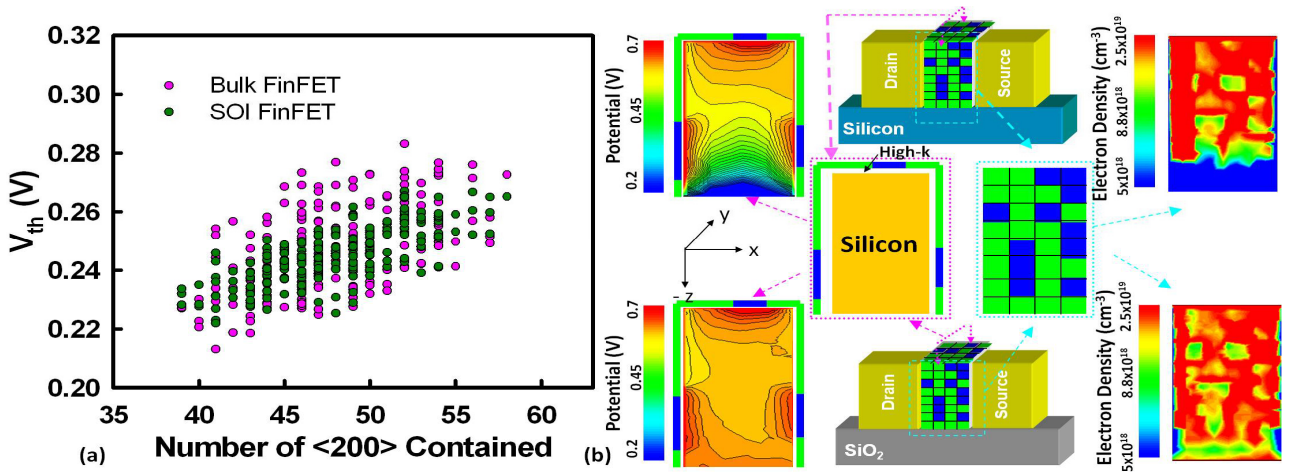


Figure 4. (a) Plot of V_{th} versus the number of <200> orientations contained (b) Comparisons of potential and electron density distributions in the *y-z* plane of bulk and SOI FinFETs.

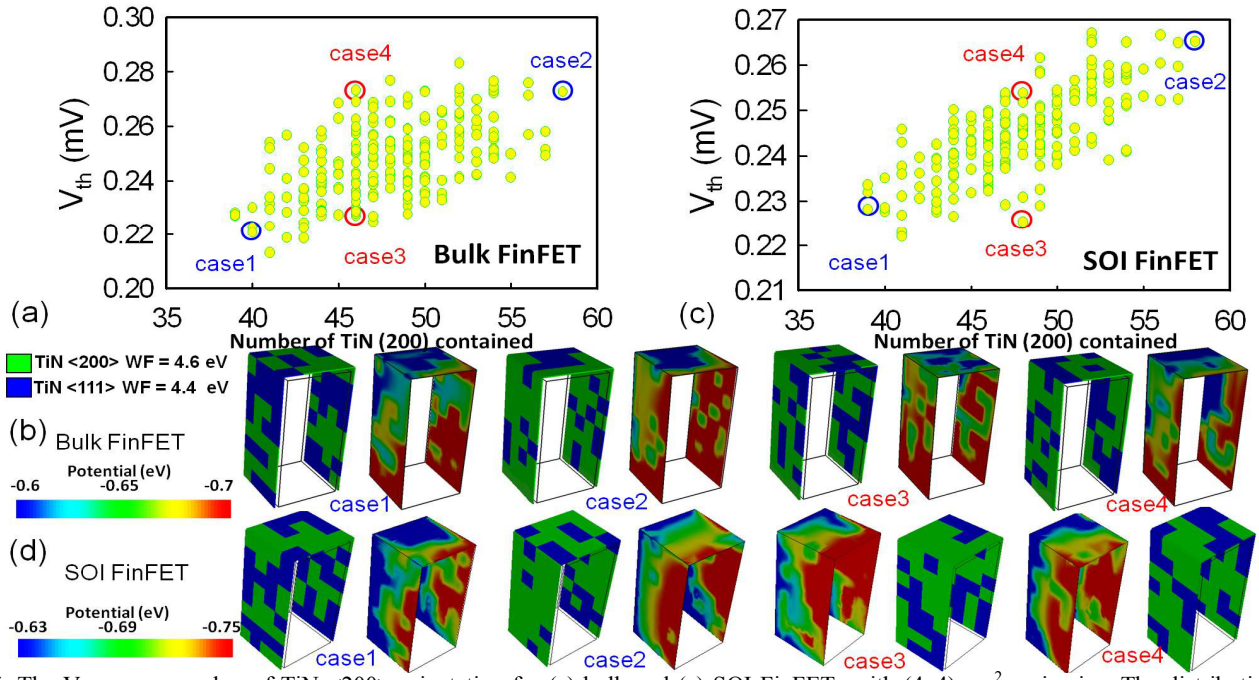
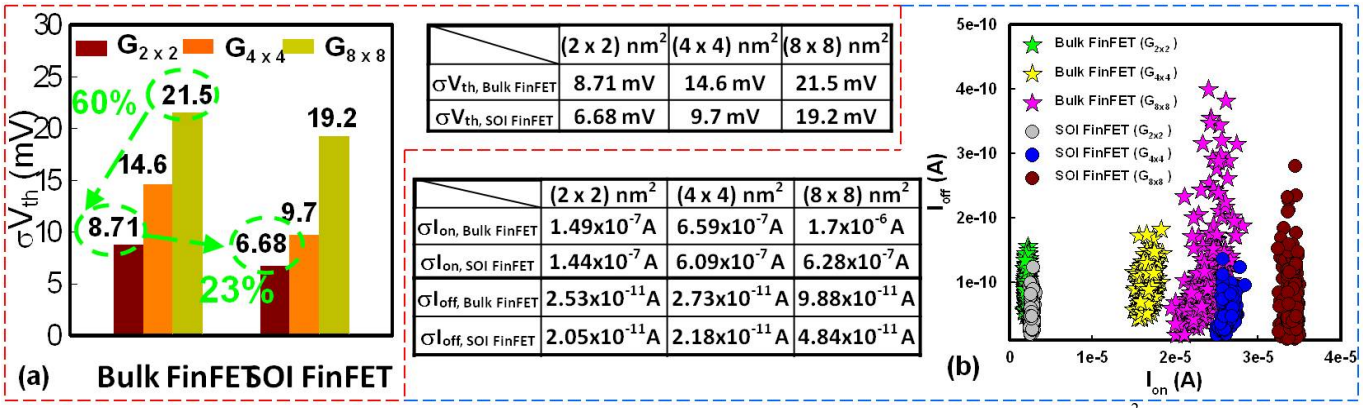


Fig. 5. The V_{th} versus number of TiN <200> orientation for (a) bulk and (c) SOI FinFETs with (4x4) nm^2 grain size. The distribution of potential profile for the case 1 and case 2 with different number of <200> orientation (grain number effect); similarly, the distribution of potential profile for the case 3 and case 4 with the same number but different position of <200> orientation (grain position effect).



	(2 x 2) nm^2	(4 x 4) nm^2	(8 x 8) nm^2
$\sigma V_{th,\ Bulk\ FinFET}$	8.71 mV	14.6 mV	21.5 mV
$\sigma V_{th,\ SOI\ FinFET}$	6.68 mV	9.7 mV	19.2 mV

	(2 x 2) nm^2	(4 x 4) nm^2	(8 x 8) nm^2
$\sigma I_{on,\ Bulk\ FinFET}$	$1.49x10^{-7}$A	$6.59x10^{-7}$A	$1.7x10^{-6}$A
$\sigma I_{on,\ SOI\ FinFET}$	$1.44x10^{-7}$A	$6.09x10^{-7}$A	$6.28x10^{-7}$A
$\sigma I_{off,\ Bulk\ FinFET}$	$2.53x10^{-11}$A	$2.73x10^{-11}$A	$9.88x10^{-11}$A
$\sigma I_{off,\ SOI\ FinFET}$	$2.05x10^{-11}$A	$2.18x10^{-11}$A	$4.84x10^{-11}$A

Figure 6. The plot of (a) σVth and (b) I_{on}-I_{off} curve of the bulk and SOI FinFETs with (2x2), (4x4) and (8x8) nm^2 grain sizes, where the comparison of σVth, σI_{on} and σI_{off} between bulk and SOI FinFETs are summarized in the table.