HiSIM-SOTB: A Compact Model for SOI-MOSFET with Ultra-Thin Si-Layer and BOX

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ABSTRACT

The SOI-MOSFET has three surfaces, for which electrostatic potential values are very much dependent on applied bias conditions. HiSIM-SOTB has been developed by solving the Poisson equation iteratively to calculate the surface potentails accurately for any bias conditions. It has been verified that the model can indeed reflect structural size variations over a very large range. The model includes all possible charges induced at the three oxide surfaces in the SOI structure. The approach with simultaneous inclusion of the three surface charges can easily make the circuit simulation unstable. To overcome such stability problems we have developed a sophisticated method for reliably solving the Poisson equation. We address the development of solutions to the outlined challenges in our report.

Keywords: compact model, surface-potential model, Poisson equation, thin body and thin BOX SOI-SMOFET

1 INTRODUCTION

We can safely say that one of the most promising next generation device structures are SOI-MOSFETs as they are suitable for high performance circuits as well as low power applications due to their improved subthreshold slope and reduced junction capacitances [1]. Here new possible applications of the SOI-MOSFET have been investigated intensively to overcome problems appearing in advanced MOSFETs with thinner SOI layer T_{SOI} as well as thinner buried oxide T_{BOX}. For example, the possibility to suppress MOSFET variations by utilizing the substrate contact and thin BOX thickness, called SOTB-MOSFET (silicon on thin BOX), has been demonstrated [2,3,4]. Thus compact models treating all expected SOI-MOSFET phenomena caused by different SOI-structure types are strongly required for investigating circuit-design advantages.

Our aim is to provide a circuit simulation model capturing all effects of the complete SOI-device structure. It is shown here that this is realized on the basis of a completely surface-potential-based modeling including all possible charges induced. This enables a compact SOI-MOSFET model also for simulation of any structural variations as well as bias conditions.

2 MODEL EQUATIONS

The Poisson equation together with the Gauss law describes the relationship between induced charges and the potential distribution written as [5,6]

$$V_{gs} - V_{fb} - \Delta V_{th} = \phi_{s.SOI} - \frac{Q_i + Q_{dep} + Q_{b.SOI} + Q_{s.bulk}}{C_{FOX}} \quad (1)$$

where V_{gs} is the gate voltage, V_{fb} is the flatband voltage, $\phi_{s.SOI}$ is the front surface potential of the SOI silicon layer, $\phi_{b.SOI}$ is the back surface potential, $\phi_{s.bulk}$ is the surface potential of the substrate. The charges, the inversion charge of SOI silicon surface Q_i, the depletion charge of the SOI silicon layer Q_{dep}, the charge induced at the SOI silicon back surface, and Q_{bulk} are functions of the potential differences between $\phi_{s.SOI}$ and $\phi_{b.SOI'}$, $\phi_{b.SOI'}$ and $\phi_{b.SOI}$, and $\phi_{s.bulk}$ to the substrate node, respectively, where $\phi_{b.SOI'}$ is the potential min/max within the SOI layer. C_{FOX} is the capacitance of front oxide, and ΔV_{th} is the threshold voltage shift describing the short-channel effect [7].

Since the SOBT-MOSFET includes three additional freedoms (the T_{BOX} thickness, the impurity concentration in the substrate, and the bulk bias V_{bs}), there should be a huge variety of device geometries according to different applications. One extreme variation is the double gate MOSFET with very thin T_{BOX} together with very high substrate impurity concentration. Another extreme case is the partially depleted SOI-MOSFET with relatively thick T_{SOI}, which is still actively used for high performance applications. As a new development of SOI-MOSFET with thin T_{SOI} as well as thin T_{BOX} designers are intending to exploite the V_{bs} bias variation to optimize the circuit performance. Therefore, the imporatnt task is to develop a model which can be applicable for optimizing the V_{bs} depepdence. Under such application condition a very strong coupling among three surface potentials is expected. To achieve accurate prediction for such tasks the Poisson equation must be solved without any approximations. Possible solutions of four typlical potential distribtuion are summarized in Fig. 1. It is seen that signs of charges in the Poisson equation are varied according to the applied bias conditions. To consider all possible combinations of the signs explicitly is very important for SOTB generation.

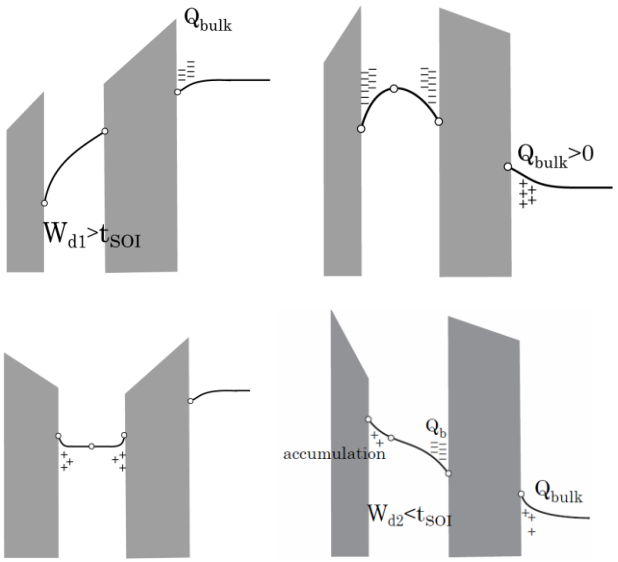

Fig. 2. Four typical potential distributions along the vertical direction for different bias conditions.

To solve three surface potentials two additional equations must be derived. One is derived from the boundary condition, and the other is derived from the approximation of the triangle potential distribution

$$\phi_{b.SOI} = \phi_{s.bulk} - \frac{Q_{s.bulk}}{C_{BOX}} \quad (2)$$

$$\phi_{s.SOI} = \phi_{b.SOI} - \frac{Q_{s.bulk} + \frac{1}{2}Q_{dep}}{C_{SOI}} \quad (3)$$

where C_{BOX} is the capacitance of BOX and C_{SOI} is defined as follows

$$C_{SOI} \equiv \frac{\varepsilon_{Si}}{T_{SOI}} \quad (4)$$

These three surface potential equations must be solved simultaneously to achieve accurate general solutions for any bias conditions. Fig. 2a shows charges induced in different semiconductor layers and the potential distribution for an applied bias of V_{gs}. The calculated three important potential values are shown in Fig. 2b as an example for a T_{SOI}=50nm case [8].

In HiSIM-SOTB three equations (Eqs. 1-3) are solved iteratively from the gate electrode to the substrate electrode in a consistent way. For the SOTB-MOSFET case all equations are strongly coupled each other, and can be solved only iteratively. However, the iteration procedure could be unstable due to the strong coupling. Therefore good initial guesses are the key for the convergence. Fortunately, the SOTB-MOSFET can be specified as the fully-depleted conditon, which simplifies the analytical descriptions.

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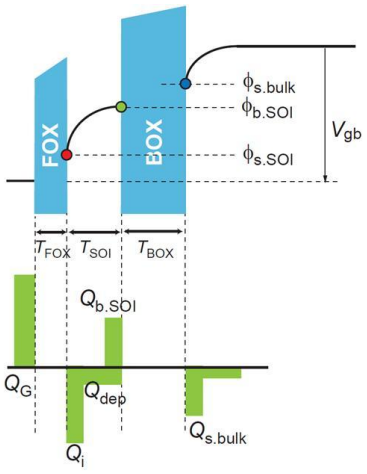

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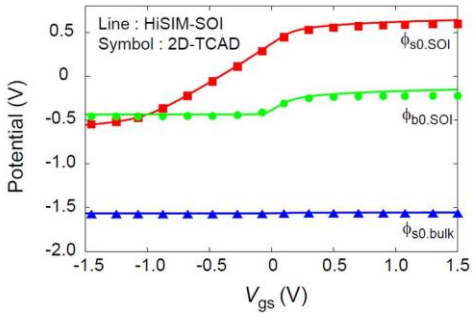

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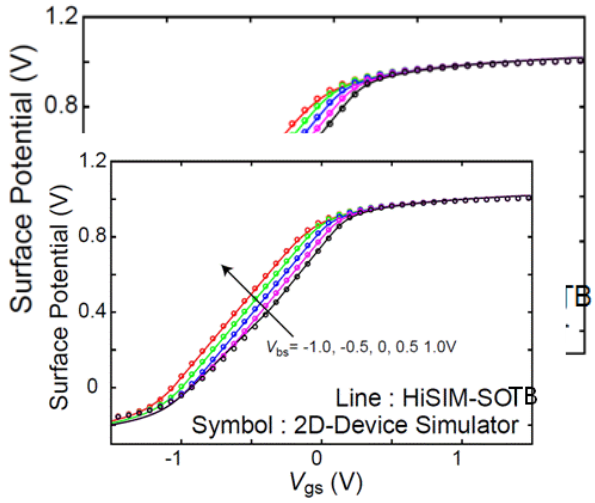

Fig. 3. Comparison of calculated potential values as a function of V_{gs} for various bulk voltage V_{bs} values.

3 CALCULATION RESULTS

The model includes all device parameters explicitly and solves the Poisson equation iteratively without

approximations, which is the same way as numerical device simulators undertake. In addition to the short simulation time in comparison to the numerical simulators, stable convergence has been also verified.

Fig. 4 shows calculated I_{ds}-V_{ds} characteristics with an extracted model card (T_{FOX}=2.5nm, T_{SOI}=60nm) and further calculations are investigated by varying T_{FOX} and T_{SOI}. The impurity concentration in the SOI lalyer is kept 10^{18}cm^{-3} and the channel width and length are fixed to 0.25µm and 0.15µm, respectively. The reduction of T_{SOI} switches the condition of the SOI layer from the partial depletion to the full depletion, resulting in weakening of the kink effect. The increase of the T_{FOX} weakens the gate control, resulting in the enhanced characteristics obvious for thepartial depletion condition.

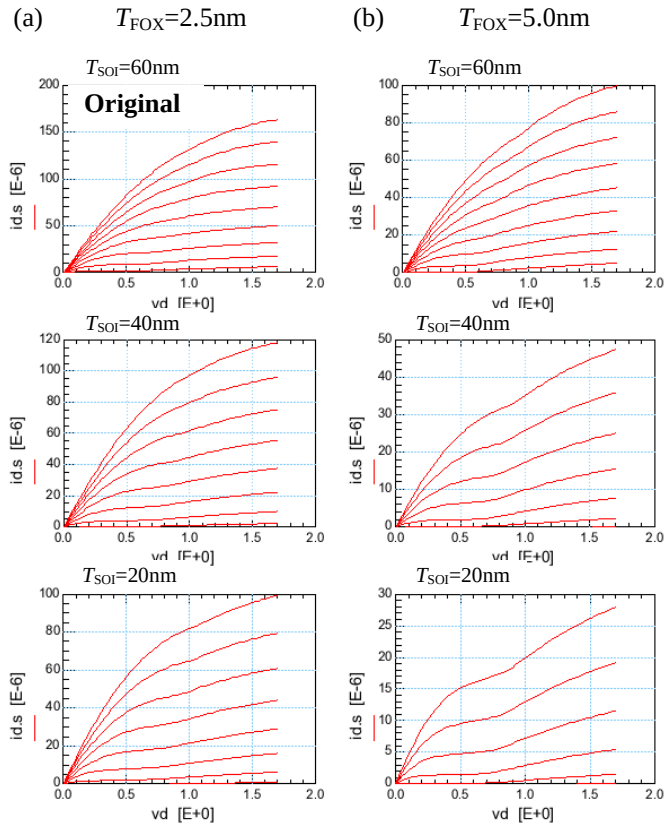

Fig. 4. Investigation for predictability test of HiSIM-SOTB. Calculation results with a model card extracted for a technology is shown in the upper left figure. The device parameters are varied with the fixed impurity concentration of the SOI layer N_{SOI} to 10^{18}cm^{-3} and it is shown that calculation results show extected characteristics.

Since the V_{bs} controllability of the SOTB-MOSFET is used for design optimization, accurate modeling of the V_{bs} dependence is important. Fig. 5 shows the threshold voltage V_{th} as a function of the impurity concentration of the SOI layer N_{SOI}. The model card is the same as used for the calculations shown in Fig. 4. By increasing N_{SOI}, the depletion width is reduced, resulting in the the disapplearing of the coupling of the surface with the substrate. This is seen in the independence of V_{th} on V_{bs}. Fig. 6 compares the same characteristics as shown in Fig. 5 but a SOTB-MOSFET with a thinner T_{SOI}. It is obvious that the V_{bs} dependence of V_{th} becomes stronger thus more V_{th} variation is achieved. It is also seen that the reduction of N_{SOI} dependence is also effective for suppressing the V_{th} variation.

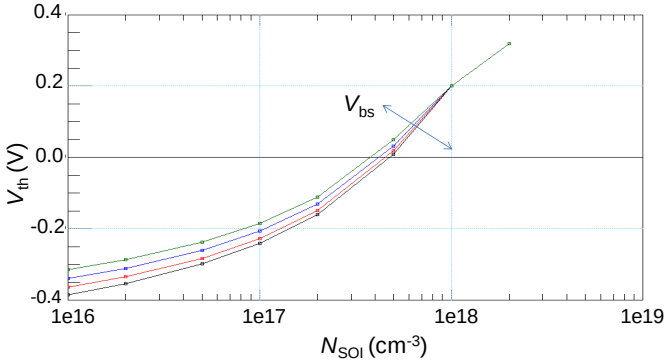

Fig. 5. Calculated inversion charge with HiSIM-SOI (lines) and 2D-device simulation (symbols) as a function of V_{ds} for various V_{gs} values.

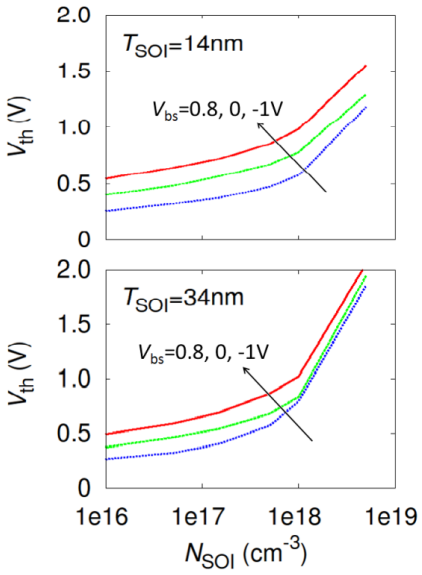

Fig. 6. Threshold voltage V_{th} as a function of the impurity concentration in the SOI layer N_{SOI} for various V_{bs} values. Two different SOI layer thicknesses T_{SOI} are compared.

Another important characteristic compact models have to model accurately is the capacitance. Fig. 7 shows calculated nine independence intrinsic capacitances with HiSIM-SOTB as a function of V_{gs}. For the calculation T_{SOI} is fixed to 40nm. It is seen that the partially depleted condition starts to occur below V_{gs} where the jump is observed. On the contrary the calculation result with TSOI=30nm shown in Fig. 8 demonstrates that the fully depleted condition is

kept nearly a whole bias region. It enters the partially depleted condition just at the flat-band. Even though the partially-depleted condition seems unimportant for SOTB-MOSFETs, a smooth transition to all possible conditions is a key to obtain stable circuit simulation. For the purpose to consider all possible charges induced in SOTB-MOSFETs is inevitable.

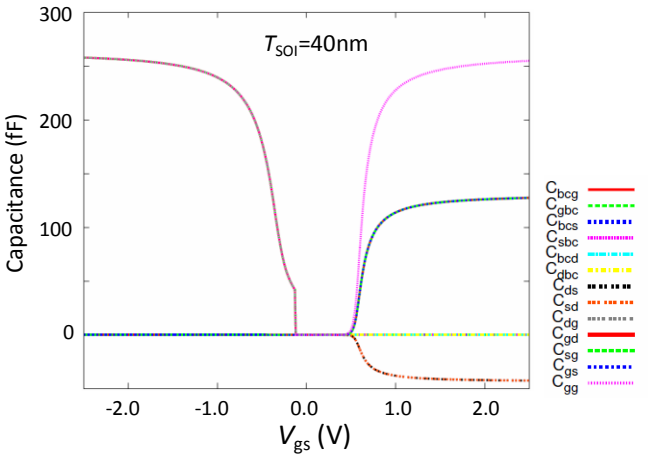

Fig. 7. Calculated nine independent capacitances as a function of V_{gs} for T_{SOI}=40nm. The jump shows the switch between partially/fully depleted conditions.

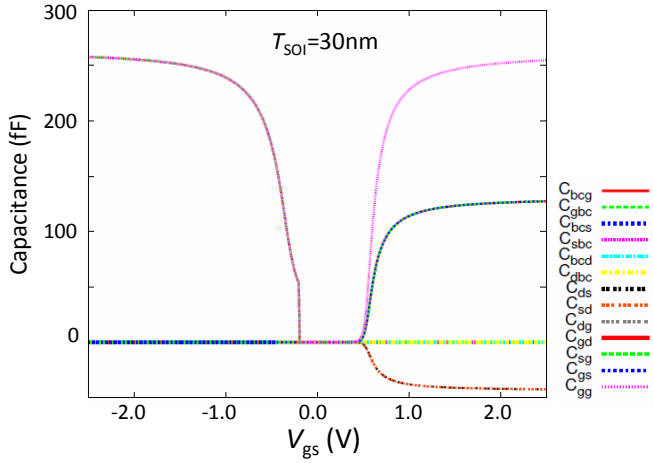

Fig. 8. The same calculation results as shown in Fig. 13 for T_{SOI}=30nm. The switch is reduced to nearly at the flat-band voltage of -0.32V.

4 CONCLUSION

We have developed the compact model HiSIM-SOTB for SOTB-MOSFETs for circuit simulation based on the Piosson equation. All possible induced charges are included in the equation. Thus the model enables to calculate any structural variations as well as bias conditions. The model can be even applicable for device optimization for designing high performance circuits.

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