Fabrication of an interposer with FIB-etched nanovias for molecular electronics

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ABSTRACT

As molecular electronics gets more explored, the need for a device enabling electrical characterization of the synthesized molecules arises. A micro-nano interposer is thus proposed to allow the electrical connection between a molecular circuit and mesoscopic electrodes with atomic scale precision. This paper especially focuses on the nanovias module, which aims at bridging the gap between the nanoscale circuit and the microscale electrodes. Nanovias were fabricated with a Focused Ion Beam (FIB) equipment, both for the etching and filling steps. The influence of set-up parameters was investigated in order to understand deposition process and improve the vias quality (geometry and filling). Nanovias with aspect ratios between 2 and 8 were fabricated and are presented to illustrate the etching and deposition optimizations.

Keywords: Nanovias, FIB, interposer, molecular electronics

1 INTRODUCTION

The field of molecular electronics is being increasingly explored, from the synthesis to the characterization of molecular electronic functions such as diodes [1,2], memories [1,3] and logic gates [1,4]. The electrical characterization of such nano-objects is mainly conducted under vacuum with scanning probe microscopies and near-field approaches (STM, AFM). These advanced techniques do not allow an easy access to the electrical properties of the synthesized molecules since it requires a complex configuration, such as UHV environment and a mutliple probes equipment. Break junctions are also commonly used to measure the conduction properties of such molecules [5]. Achieving a stable and reproducible contact device is however still very challenging [6,7]. Besides, Moore's law and the downward scaling of transistors, which has guided most of the developments in microelectronics over the last 40 years, has enabled the development of new component designs, innovative techniques and processes.

Here is proposed an integration platform based on microelectronic processes and allowing the electrical characterization of molecular functions. This paper particularly focuses on the fabrication of nanovias using a commercially available FIB equipment and the tungsten filling of such vias with an aspect ratio between 2 and 8 (AR2 to AR8).

2 CHIP DESIGN AND FABRICATION

The proposed interposer is composed of three key-parts: an atomically-reconstructed surface (A), which receives the atomic circuit, a connective part (B), which contains the nanoscale and micro-scale interconnections, and a cap (C) , which aims at protecting the atomic circuit and the reconstructed surface (Fig.1).

The reconstructed surface (A) and the connective part (B) are part of the same SOI (silicon on insulator) substrate, whereas the cap (C) is a Silicon substrate bonded on the SOI substrate. Part B ensures the electrical connection from the nanoscale circuit to the microscale pads and includes implanted areas (in the top Si layer), nanovias (in the burried oxide layer – BOX), and metallic lines between nanovias and micropads (electrodes). Cavities are etched on the backside of part B to enable nanovias fabrication, dopant implantation, and metallic lines deposition.

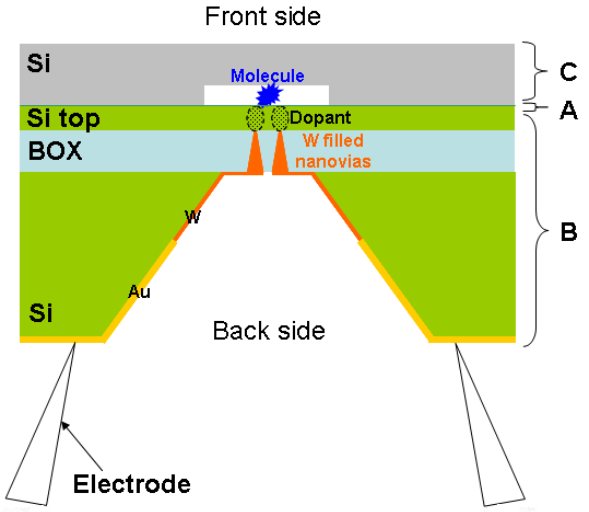


Figure 1: Scheme of the designed chip for integration of molecules on Si substrate.

This paper focuses on the fabrication of nanovias, which is one of the key-module of part B. Nanovias ensure the electrical connection through the BOX, between implanted species on the front side and metallic lines plus micropads on the back side. Nanovias are firstly etched in the SiO_2 layer prior to being filled with tungsten with FIB equipment. This technique has been chosen for its versatility and its ability to etch, deposit metal and characterize the sample.

3 EXPERIMENTAL DETAILS

Two types of oxydized silicon substrates with respectively 400nm (T400) and 1000nm (T1000) thick oxyde layer were used to qualify the process. The configuration T400 with 400nm of silicon oxide mimics the BOX layer of the final chip stack (Fig.2).

To study nanovias etching and filling, a FIB Strata DB400S from FEI was used. A liquid metal source is used to generate a Ga^+ ion beam with currents between 1.5pA and 21nA. The dwell time can be tuned from 50ns to 1ms. The ion energy was kept at 30keV.

The dual beam FIB/SEM system enables to realize cross sections of the nanovias after etching or after W filling. Surface protection by electron beam induced deposition (EBID) of $W(CO)_6$ or TEOS decomposition was carried out prior to any FIB cross section and SEM imaging.

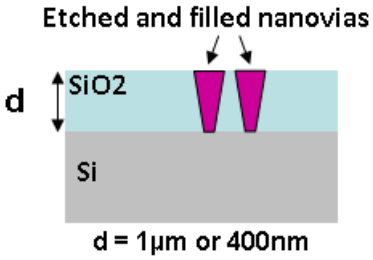


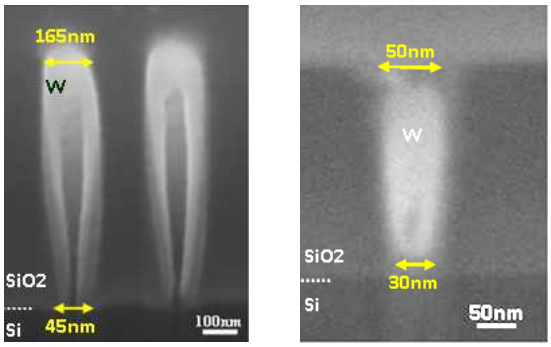
Figure 2: Substrate used for experimentations

4 RESULTS AND DISCUSSION

4.1 Nanovias etching

As a first step, the accurate control of the etching stop at the SiO_2/Si interface has been studied. Using a pre-defined and calibrated time of etching is not a reliable method as the beam emission and size vary from one day to another.

The endpoint detection method consists in monitoring the sample's absorbed current during the experiment [8] and provides an accurate detection of the SiO_2/Si interface.



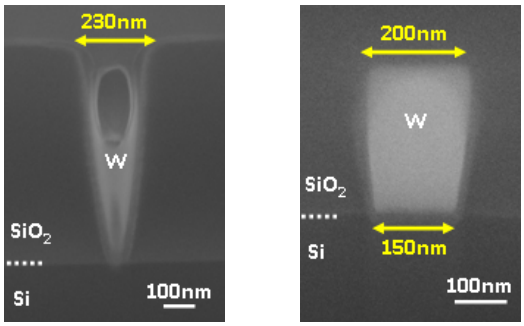
(a) (b)

Figure 3: Partially filled (a) AR6 via (165x165nm²) in T1000 (b) AR8 via (50x50nm²) in T400

The diameter of the ion beam used to etch the oxyde layer is an important parameter as it determines the etching duration of the vias. Higher beam diameter (i.e. higher beam current) will lead to a fast etching of the oxyde. However, a too rapid etching results in a lack of control of the etching stop. We found that at least 10 seconds of etching are needed for an accurate etching stop at the SiO_2/Si interface.

The ion beam current is then chosen depending on the oxyde thickness and via diameter. For the sample T1000, a current beam between 10 and 14pA can be used, while for vias etched in sample T400 the used current beam is 4pA. Typically, for T1000, 20s are necessary to etch AR4 vias in T1000 while 10s are required to etch AR4 vias in T400.

The obtained results are presented on figure 3a for T1000 and 3b for T400. Vias with an aspect ratio as high as 8 were etched, but the stop at the SiO_2/Si interface was not optimized due to the short etching duration (6s). We can observe on the figure 3 that the via is cone-shaped. The via geometry depends on the expected aspect ratio. With AR smaller than 5, vias present vertical sides and a flat bottom while higher AR vias are more cone-shaped. The influence of the aspect ratio on the geometry is shown in figure 4. The dimension of the AR4 via (T1000) on the surface is the same as the AR2 via in T400, but the shape is conic due to the higher depth. The sputtered material is indeed redeposited on the sides of the via, preventing a flat bottom.



(a) (b)

Figure 4: (a) AR4 via (230x230nm²) in T1000 (b) AR2 via (200x200nm²) in T400

The nanovia shapes and geometries obtained for T1000 samples are in good agreement with the nanovia aspect ratio previously demonstrated by Lwin [9]. Etching vias in T400 allows to reach smaller diameters and more favorable geometries (flat bottom), due to the smaller aspect ratio.

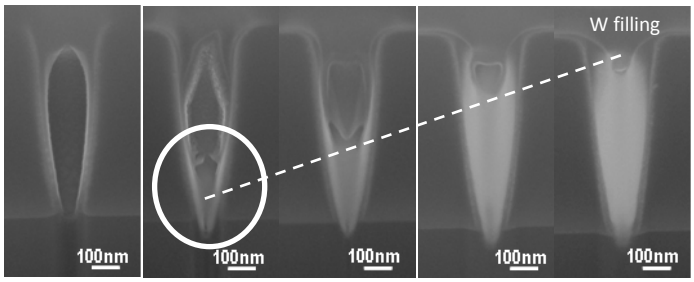
As a conclusion, for nanovias with aspect ratio lower than 5, via etching is well controlled and the via bottom is flat. For higher aspect ratio, etching becomes challenging due to the short etching duration, and material redeposition.

4.2 Nanovias filling

In order to ensure the current conduction, we need to deposit a low resistivity metallic material, here the tungsten.

A FIB/SEM dual beam system has the capability to deposit tungsten by either electron beam or ion beam induced deposition (EBID or IBID) using $W(CO)_6$ as a precursor. In our application, tungsten will be used as a conductive connection meaning its resistivity is an important prameter. Previous studies have measured resistivities as low as $2{,}5.10^{-6}\Omega m$ for W-IBID [10] and $3.10^{-5}\Omega m$ for W-EBID [11]. We have then focused our work on IBID deposition. However, due to the C and Ga contents within the deposited material, these reported values are higher than the resistivity of bulk tungsten: $5{,}510^{-8}\Omega m$ [12].

Challenges presented by this process are the quality of the filling and the over-etching issue due to the competition between deposition and etching when using the ion beam.
Concerning the first objective, the most important is to obtain a continuous deposition of the tungsten from the bottom of the via to the top. Beam parameters can be tuned in order to understand the filling mechanism and avoid a partial filling. Beam parameters optimization and suitable scan strategies allow a high rate deposition and a minimized over-etching.



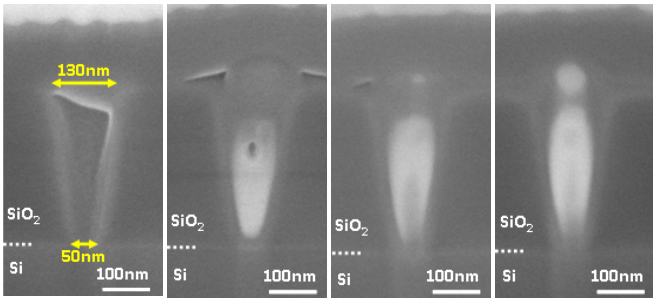
(a) (b) (c) (d) (e)

Figure 5: SEM pictures of AR4 nanovias (T1000) etched and filled with tungsten. Pictures have been taken at several steps: (a) no filling, (b) 3s, (c) 7s, (d) 16s, (e) 20s.

Several parameters can particularly influence the quality of nanovias filling: the beam size, the dwell time, the overlap, the size of the deposition scan window. Choosing the smallest beam size results in an accurate scan window positionning and a controlled material deposition. Using a larger beam induces deposition on the side walls and a bridge formation with a void under it.
The area of the deposition scan window has to be in the same range as the one of the via bottom.
These parameters influence the filling phenomenon in different ways. To understand and optimize it, the nanovias filling process was investigated. First, on figure 5, SEM pictures of via section made in AR4 vias ($240x240nm^2$ in T1000) at several steps of the filling progress are presented.
We can observe that, the side of the vias are first covered, and then the bottom of the via is progressively filled. When the via width is larger than the deposition scan window size, the deposition does not occur only on the via sides and the growth of a pin is observed.

We can also notice that in the via without tungsten, the via etching stopped at the SiO_2/Si interface, while in all the other ones, there is an over-etching about 30nm whereas the etching conditions are the same. We can assume it is done during the filling, because of the competition between deposition and etching: as the via is cone-shaped, precursor molecules have difficulties in accessing to the bottom of the via and etching is prevailing.

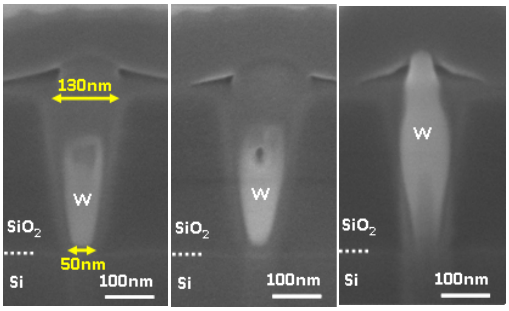
To optimize nanovias filling, the influence of dwell time and overlap was studied.



(a) (b) (c) (d)

Figure 6: SEM pictures of tungsten filled AR4 vias (T400) with dwell times: (a) 100ns (b) 300ns (c) 600ns (d) 1000ns.

On figure 6 are presented AR4 vias etched in T400 and filled with the same overlap (0%) and duration (17s). Dwell time variation is going from 100ns to 1000ns. No filling was observed for 100ns as we can see on figure 6a while dwell times of 600ns (figure5c) and 1000ns (figure 6d) result in a partial filling. A complete filling is obtained for 300ns (figure 6b). As dwell time is the duration the beam stays in one pixel, we can assume that for 100ns, the beam does not stay long enough to generate tungsten deposition. When dwell time is too long (like 600ns), we can assume that the deposition on the via walls is too thick, thus preventing the filling of the via bottom and leading to the creation of a void. As a consequence, for the study of the overlap, a dwell time of 300ns was used.



(a) (b) (c)

Figure 7: SEM pictures of tungsten filled AR4 vias (T400) with overlaps: (a)-50% (b) 0% (c) 90%.

On figure 7 are presented AR4 vias etched in T400 and filled with the previously selected dwell time (300ns) and the same duration (17s), while overlap varies between -50% and 90%.

For a 90% overlap, a partial filling is obtained while for 0% and -50%, a complete filling is observed.
A compromise can be found between 0% and 90% since, the higher the overlap, the smaller the pitch and then the higher the efficiency of the deposition. An overlap of 50% with a dwell time of 200ns were used as a optimizes parameters. The result is presented on figure 8 for T400: we can see an AR4 via completely filled.

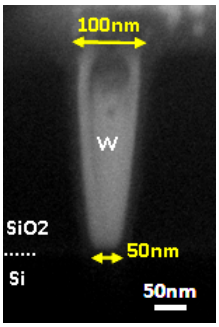


Figure 8: Completely filled AR4 vias in T400

As a conclusion of the filling study, for aspect ratio lower than 3, filling is achieved using standard conditions whereas parameters tuning is compulsory to fill vias with aspect ratio between 3 and 5. The best reported parameters to reach complete filling are a dwell time of 200ns and a positive overlap of 50%.

5 CONCLUSION

We report etching and filling of nanovias with aspect ratio between 2 and 8. We studied the filling process and the influence of the beam parameters to improve via filling and prevent the formation of a void at the bottom of the via.

We demonstrated the fabrication of nanovias with aspect ratio as high as 8 and the complete filling of nanovias with aspect ratio as high as 5.

Considering the integration platform, a complete filling of AR4 vias in a 400nm thick SiO_2 layer was obtained with an accurate etching stop at the SiO_2/Si interface.

The characterization of the electrical properties and the chemical composition of the nanovias is under investigation. Future work will also include the integration of the implantation and the nanovia modules in the connective substrate.

6 ACKNOWLEDGMENTS

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