Modeling of DMOS Device for High-Voltage Applications Based on 2D Current Flow

F. Ueno, A. Tanaka, M. Miyake, T. Iizuka, *T. Yamamoto, H. Kikuchihara, H. J. Mattausch, M. Miura-Mattausch
Graduate school of Advanced Sciences of Matter, Hiroshima University, Higashi-Hiroshima, Japan
*Denso Corporation, Aichi, Japan
Telephone: +81 82 424 7659, e-mail:fumiya-ueno@hiroshima-u.ac.jp

ABSTRACT

We have extended the compact model HiSIM_HV valid for the DMOS structure by considering the vertical 2D current flow. The resistance in the drift region is modeled in the way how the depletion width spread according to the current injected into the darin contact. The model includes an additional fitting parameter. Accuracy of the developed model has been verified with 2D-device simulation results. Predictability of the model is demonstrated.

Keywords: DMOS, compact model, depletion region, 2D-effect, current flow

1 INTRODUCTION

High-voltage devices are utilized for a variety of applications, where voltages rang from a few volts to a few hundred volts. To develop high performance circuits for variety of applications, an accurate compact-model development is inevitable. LDMOS is usually applied for rather low bias conditions [1], whereas DMOS has been developed for higher voltage applications with low on-resistance [2]. HiSIM_HV has been developed originally for the LDMOS structure and has been extended for the symmetrical HV-MOSFET. This paper describes extension of the compact model HiSIM_HV for DMOS applications. The key development is to consider the vertical current flow caused by the feature of the DMOS structure with the drain contact on the bottom of the device. It will be demonstrated that the developed model can reproduce observed features of DMOS characteristics accurately.

Fig. 1 compares I_d-V_{ds} characteristics between DMOS and LDMOS, where the overlap length and the drift length are kept the same. Only the difference is the structure, namely LDMOS is lateral and DMOS is vertical.

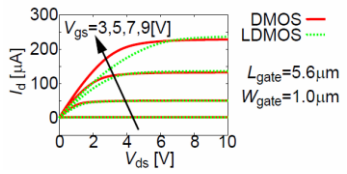

Fig. 1: 2D-device simulation results of a DMOS *I-V* characteristics (solid lines) in comparison to those of LDMOS (dotted lines).

2 FEATURE OF HV-MOSFETS

HiSIM_HV solves the Poisson equation along the depth direction iteratively [3]. In addition to the iteration for the surface-potential calculation, the potential distribution along the device from the source contact to the drain contact is also solved iteratively. Here the high resistive drift region is modeled separately from the conventional MOSFET part as shown in Fig. 2. This high resistive drift region causes anomalous node potential characteristics as shown in Fig. 3 [4,5].

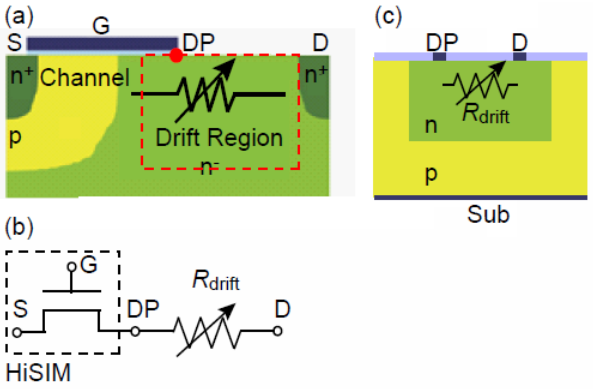

Fig. 2: (a) Schematic of the LDMOS structure. (b) Modeling of the high resistive dirfit region as a resistor.

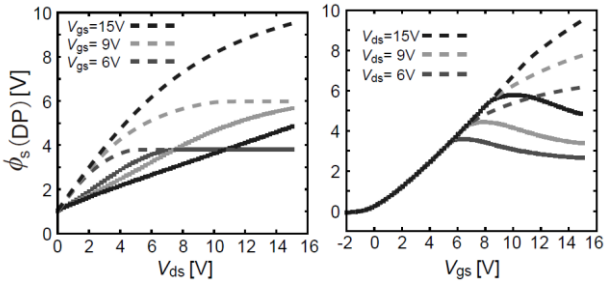

Fig.3. Comparison of calculated potential values at the edge underneath the overlap region (see Fig. 2a) by HiSIM_HV with the resistance effect (full lines) and without (dashed lines) for a gate length of 0.3μm and a gate width of 10μm.

The DMOS structure is shown in Fig. 4. DMOS sustains high voltage within the drift region, which is formed

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vertical to the device surface. The drain contact is fabricated at the bottom of the lightly doped substrate. For our investigation only half of the device is considered, because the device is perfectly symmetrical. If the gate voltage V_{gs} is switched on, carriers are injected into the drift region from the channel and drifted into the drain contact. This principle current flow is the same both for DMOS and LDMOS. Fig. 5 compares simulated current flows in drift region for the both cases. It can be observed that the width of the current flow for DMOS within the drift region spreads nearly in the whole the drift region. This widening of the current flow could be the reason for the reduced resistance effect observed in Fig. 1.

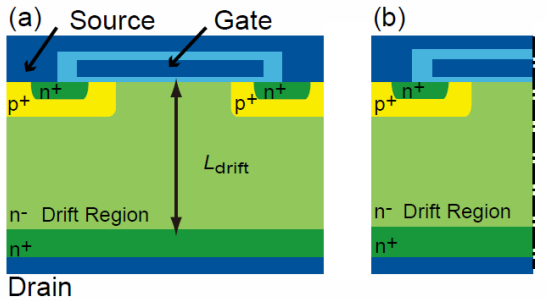

Fig. 4: (a) Schematic of DMOS structure. (b) structure used for investigation of 2D-device simulation.

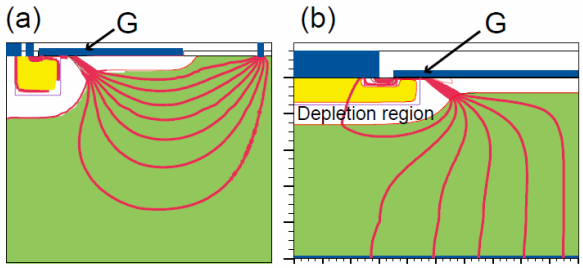

Fig. 5: 2D-device simulation results of current flow for (a) LDMOS and for (b) DMOS. The white colored region underneath the the overlap region and at the channel/drift region junction denotes the depletion condition.

3 MODEL DEVELOPMENT

Carriers are injected from the channel into the drift region, where the depletion condition could fulfill the injected region as can be seen in Fig. 5(b). Under such condition the current flow is restricted within a narrow path. Afterwards the current is spread nearly to the whole width of the drift region. Thus the current flow can be characterized in two regions. One is the current flow within the depletion region, and the other is in the drift region. This feature of the current flow in DMOS can be modeled by two different resistances as shown in Fig. 6.

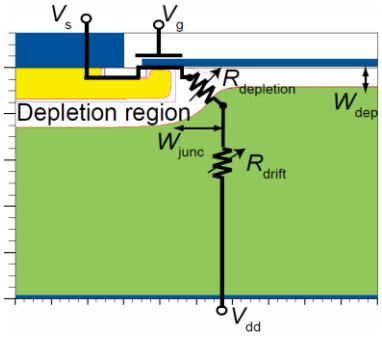

Fig. 6: Modeling of the DMOS current flow with two different resistances, $R_{depletion}$ and R_{drift}.

At first $R_{deletion}$ is modeled, where two depletion widths, W_{dep} and W_{junc}, are distinguished. As shown in Fig. 2 HiSIM_HV recognizes the potential value at the channel/drift junction ϕ_s(DP) by solving the current equation iteratively. This ϕ_s(DP) is used to calculate W_{dep} as

$$W_{dep} = \sqrt{\frac{2\varepsilon_{si}\left(V_{ds} - \phi_s(\mathrm{DP})\right)}{q \cdot N_{drift}}} \,. \tag{1}$$

The lateral depletion width at the channel/drift junction W_{junc} is calculated similarly as

$$W_{junc} = \sqrt{\frac{2\varepsilon_{si}\left(\phi_{bi} + V_{dps}\right)}{q} \cdot \frac{N_{sub}}{N_{drift}\left(N_{sub} + N_{drift}\right)}} \tag{2}$$

where N_{drift} is the impurity concentration in the drift region, N_{sub} is the impurity concentration in the channel. Calculated depletion width W_{dep} with Eq. (1) and W_{junc} with Eq. (2) are shown in Fig. 7 together with 2D-device simulation results. The current flow length L'_{dep} in the depletion region is the diagonal length of the rectangle composed by these two depletion widths and is written as

$$L'_{dep} = \sqrt{W_{dep}^{\,2} + W_{junc}^{\,2}} \,. \tag{3}$$

However, it actually gives the shortest length as schematically shown in Fig. 8. Due to the simplification introduced to describe L'_{dep} analytically, a fitting parameter A is given as

$$L_{dep} = A \cdot L'_{dep} \,. \tag{4}$$

The current flow width X_{ox} is calculated similarly by the depletion widths. W_0 is defined as the diagonal length from the lower edge at the channel/drift junction to the gate overlap region as shown in Fig. 9. Thus X_{ov} is calculated by subtracting X_{dep} and X_{junc} from W_0, which are calculated by the similarity as

$$x_{ov} = W_0 - x_{dep} - x_{junc}$$
$$= W_0 - \sqrt{2} \cdot W_{dep} - \sqrt{2} \cdot W_{junc} \quad (5)$$

where the triangle for the calculation is approximated to be isosceles. Finally, the resistance in the depletion region $R_{depletion}$ is calculated by using current flow length L_{dep} and width X_{ov} as

$$R_{depletion} = \rho \frac{L_{dep}}{x_{ov} \cdot W_{ov}} \quad (6)$$

where ρ is resistivity calculated by HiSIM_HV [2].

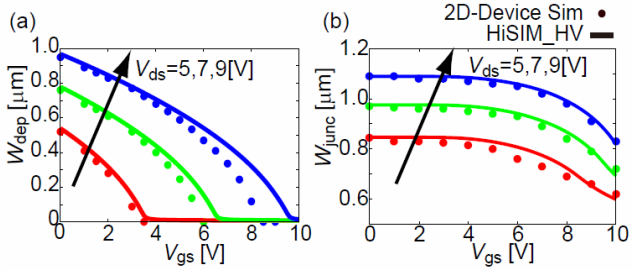

Fig. 7: Depletion Width of (a) W_{dep}, along vertical direction under the gate overlap, (b) W_{junc}, lateral direction along the surface at the channel/drift junction.

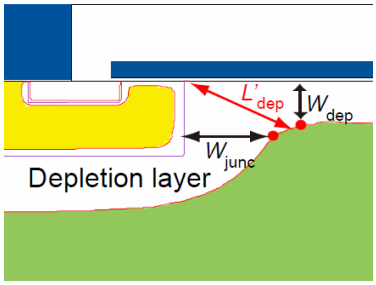

Fig. 8: 2D-device simulation result of the studied DMOS cross-section of the depletion region. L'_{dep} denotes the current-flow path.

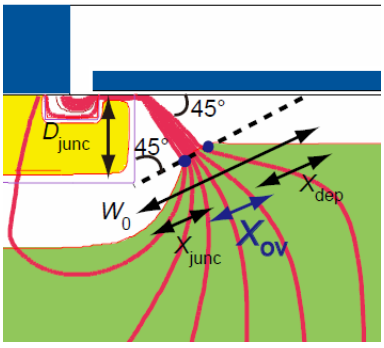

Fig. 9: Determination of the current-flow width x_{ov} within the depletion resion.

Now the resistance R_{drift} is modeled. Carriers continue to flow to the drain contact through the drift layer, where the current crowding effect is depicted in Fig. 10 schematically by a trapezoid. The current flow length L_{drift2} is modeled by subtracting the vertical depletion width at the surface W_{dep} from the total drift length L_{drift} (see Fig. 10) as

$$L_{drift2} = L_{drift} - W_{dep}. \quad (7)$$

The averaged current flow width W_{drift} is written for simplicity with W_{ov} and L_{drain} as

$$W_{drift} = \frac{W_{ov} + L_{drain}}{2} \quad (8)$$

where W_{ov} is written as

$$W_{ov} = L_{over} - W_{junc}. \quad (9)$$

The resistance in the drift region Rdrift is thus written as

$$R_{drift} = \rho \frac{L_{drift2}}{W_{drift} \cdot W}. \quad (10)$$

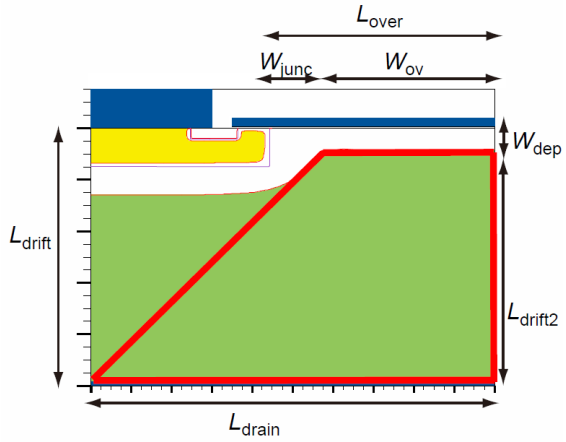

Fig. 10: Schematics of the current crowding effect in the drift region by a trapezoid.

The total resistance within the drift region is modeled as the sum of the two resistance components as

$$R_{drift\_all} = R_{depletion} + R_{drift}. \quad (9)$$

4 CALCULATION RESULTS

Calculation results of I_d-V_{ds} as well as I_d-V_{gs} characteristics with the developed resistance model are shown in Fig. 11 together with 2-D device simulation results.

Here the device parameters applied are: $L_{channel}$(channel length) = 0.8μm, L_{over} = 5.6μm, L_{drift} = 10μm, N_{sub} = 1.0e17cm^{-3}, and N_{drift} = 1.0e16cm^{-3}. Good agreements have been achieved.

Here predictability of the developed model is investigated. Fig. 12 compares 2D-device simulation results for two different L_{drift} lengths. As can be seen in the figure, increased L_{drift} results in enhanced resistance effect. Fig. 13 shows comparisons of calculated results for the L_{drift} = 20μm case with the 2D-device simulation results. For the calculation model parameter values are kept the same as those extracted for the L_{drift} = 10μm except the L_{drift} length. Good agreements prove the predictability of the developed model.

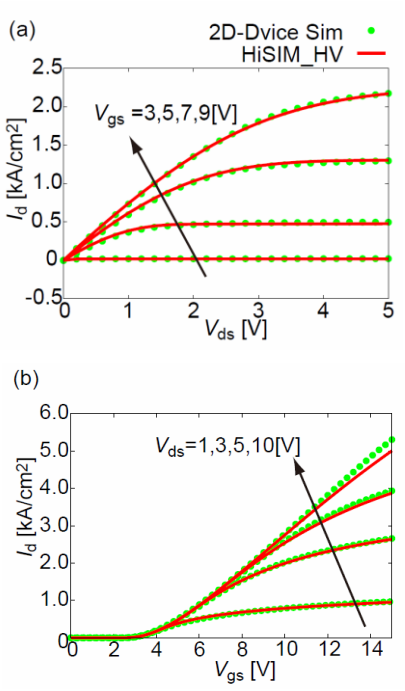

Fig. 11: Calculated characteristics of (a) I_d-V_{ds} and (b) I_d-V_{gs} with the developed model (solid lines) in comparison to 2D-device simulation results (dotted lines), where the drft length L_{drift} is kept 10μm.

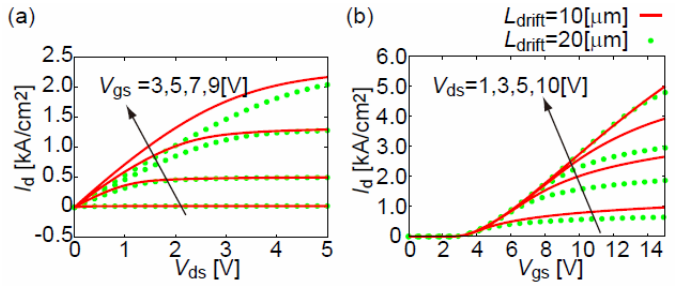

Fig. 12: Comparison of simulated characteristics for two different L_{drift} lengths (solid lines for L_{drift} =10μm and dotted lines for L_{drift}=20μm) with a 2D-device simulator (a) I_d-V_{ds} (b) I_d-V_{gs}.

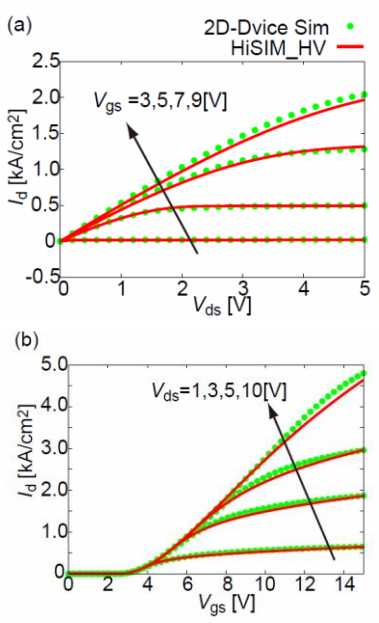

Fig. 13: The same comparison as shown un Fig. 11 for L_{drift}=20μm. For the HiSIM_HV calculation the same model parameter values are used as those used in the Fig. 11 but L_{drift} is changed to 20μm.

5 CONCLUTION

We have developed the new model for DMOS by considering depletion layer. The dependence of the resistance in the drift region on the drift length and bias condition is analyzed.

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