

Modeling of Chain-History Effect based on HiSIM-SOI

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ABSTRACT

SOI-MOSFETs suffer from the inevitable history effect. Our investigation focuses on the effect under dynamic operation with HiSIM-SOI, a compact SOI-MISFET model developed based on the Poisson equation. The special focus is given on modeling of the chain-history effect, where the dynamic history effect can be analyzed. From the investigation it is found that the history effect cannot be ignored even for SOI-MOSFETs with very thin SOI layer, which is commonly believed.

Keywords: SOI-MOSFET, history effect, compact model, chain history effect

1 INTRODUCTION

SOI-MOSFETs are considered to be suitable for high performance as well as low power applications due to their improved subthreshold slope and reduced junction capacitances [1]. A new development era is focusing on the thinner SOI layer as well as the thinner buried oxide (BOX). For example, a possibility to suppress MOSFET variations by utilizing a substrate contact with a thin BOX thickness T_{BOX} has been demonstrated [2]. SOI-MOSFETs with extremely thin SOI layer thickness T_{SOI} are now considered as a serious candidate for the main-stream sub-30nm MOSFET technology due to such advantageous features.

The floating-body structure, common for SOI-MOSFETs, prevents carriers from the spontaneous flow-out of the substrate into electrodes during device switching. The remained carriers are accumulated in the Si-layer below the gate and originate the history effect [3]. It is generally believed that the history effect will be no longer obvious for SOI-MOSFETs with very thin T_{SOI} thickness. However, long-term dynamic operation of SOI-MOSFETs in circuits could induce the history effect even for very thin-film transistors due to the continuous accumulation of carriers and we investigate this possibility here. For this purpose the floating-body effect must be modeled based on its underlying physics.

2 MEASURING HISTORY EFFECT

Different from the bulk-MOSFET, generated carriers

within the SOI layer through the impact ionization cannot flow out due to the floating-body structure. These carriers are accumulated at the bottom of the SOI layer and change the potential distribution along the vertical direction. Fig. 1 shows a schematic of the carrier storage under the impact ionization condition, which occurs during the switch-on status. In this case generated electrons flow out easily from the drain contact (see "A"). The charge Q_h stored during the switch-on condition must flow out to the source electrode during the switch-off condition (see "B"). To model the dynamic magnitude of the charge storage Q_h , we have to know the time constants required for the charging (Case A) and the discharging (Case B) for the modeling. Fig. 2 shows simulated transient drain current I_d with a 2D-device simulator for different drain voltages V_d where the gate voltage is fixed to 1V.

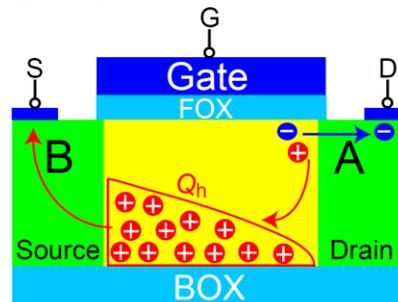


Fig. 1. Schematic of the floating-body effect. Due to the impact ionization, holes are accumulated at the bottom of the SOI layer whereas electrons flow out to the drain electrode (Case A) during the switch-on condition. The accumulated holes flow out to the source during the switch-off condition (Case B).

Fig. 3 shows measured transient drain current I_d for different drain voltage V_d where the gate voltage is fixed to 1V. Fig. 4 summarizes the time constant T_d required to store the maximum amount of the carrier density Q_h within the SOI layer as a function of the substrate current I_{sub} . An inverse relationship between T_d and I_{sub} is observed over several orders of magnitude. This constitutes a universal relationship, independent of device geometry as well as bias condition, and leads to the conclusion that the time required to store the charge Q_h is only dependent on the impact-ionization rate, which is measured as I_{sub} .

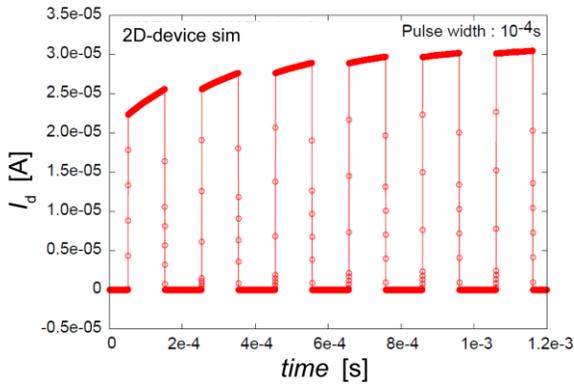


Fig. 2. Simulation result of the drain current I_d response to repetition of pulse input with width of 10^{-4} s with a 2D-device simulator. Most accumulated carriers remain within the SOI layer.

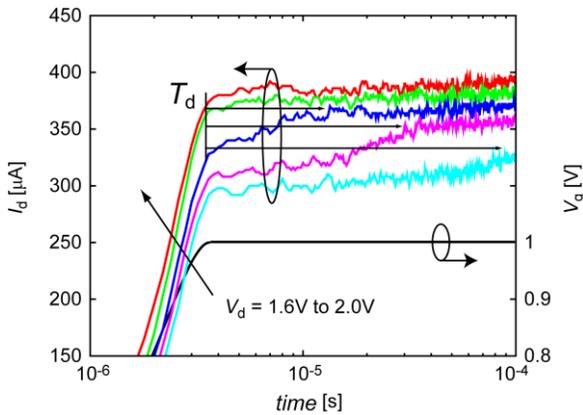


Fig. 3. Measured drain current I_d as a function of time. The charging time constant T_d is the time required to reach the maximum I_d .

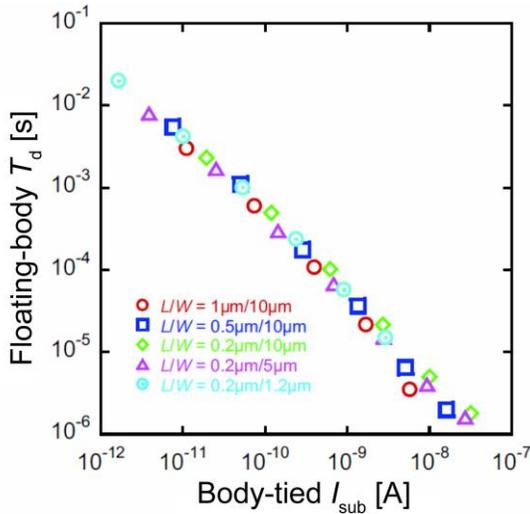


Fig. 4. Measured relationship between the time constant T_d required for reaching the maximum amount of carrier storage observed with floating-body devices and the substrate current I_{sub} of body-tie devices.

From the results observed in Fig. 4 a simple relationship is derived as

$$T_d = \frac{q_1}{I_{sub}} \quad (q_1 = 5 \times 10^{-14} [\text{A} \cdot \text{s}]) \quad (1)$$

where q_1 is a constant that does neither depend on the device geometry nor the bias condition. In HiSIM-SOI T_d is treated as the response delay of charging implemented as

$$T_d = R_{sb} \cdot C_{FOX} \quad (2)$$

$$R_{sb} = \frac{\text{HIST1}}{I_{sub}} \quad (3)$$

where the front-oxide capacitance C_{FOX} times the model parameter HIST1 is equal to q_1 in Eq. 2, obtained from the measurement shown in Fig. 4. From measured results $\text{HIST1} = 3.72 \times 10^{-8} [\text{V} \cdot \text{cm}^2]$ is extracted.

Fig. 5a shows the T_d measurement for discharging. The measurement is performed by varying the pulse-off duration as shown in Fig. 5b. If the off duration is short so that not all of accumulated charges can flow out, the charging T_d is expected to be shorter than that required to charge the whole amount. Fig. 5a concludes that the discharging time is 10ms. It was observed that this discharging time is independent of device size as well as the bias condition.

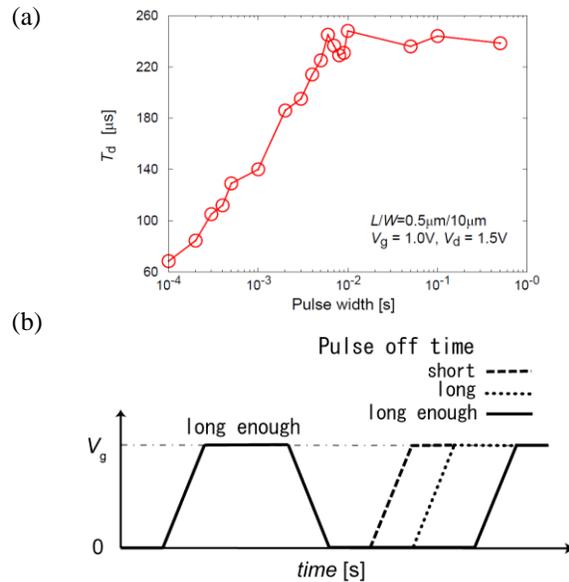


Fig. 5. (a) Time constant T_d as a function of the pulse width (switch-on duration time). The pulse-release (switch-off) time is kept the same as the pulse width. The switch-on time required for entering the saturation condition, 10^{-2} s, is the discharging delay and is independent of the device geometry and the bias condition. (b) The pulse waveform applied to the measurements.

Under dynamic operation of circuits, charge/discharging processes are repeated continuously in each device. Modeling the discharging characteristics is done by extending Eq. 3 as

$$R_{sb} = \frac{\text{HIST1}}{I_{sub} + \text{HIST2}} \quad (4)$$

where the model parameter HIST2 is equal to C_{FOX} times 10^{-2} s, the time constant required for discharging Q_h . Under the switch-off condition no I_{sub} flows and the time constant becomes simply that required for the discharge.

3 MODELING HISTORY EFFECT

We have developed the circuit simulation model HiSIM-SOI based on the complete surface-potential-based description [4]. The model is extended by considering the storage charge Q_h , which is included in the Poisson equation explicitly. The developed delay T_d description for accumulating Q_h in the T_{SOI} layer given in Eq. 4 is implemented into the model in the same way as the NQS effect. Thus the history effect is treated in a consistent way based on its physics.

Fig. 6 shows calculated switching performance with the developed model in comparison to 2D-device simulation results. For the comparison four different V_d values are shown, while V_g is fixed to 1V. For the calculation model parameter values for describing the history effect (HIST1 and HIST2) are kept the same. Good agreements are verified. The reason for the increased I_d is the potential increased due to the stored charge. Thus it is seen that the large stored charge induces large current flow.

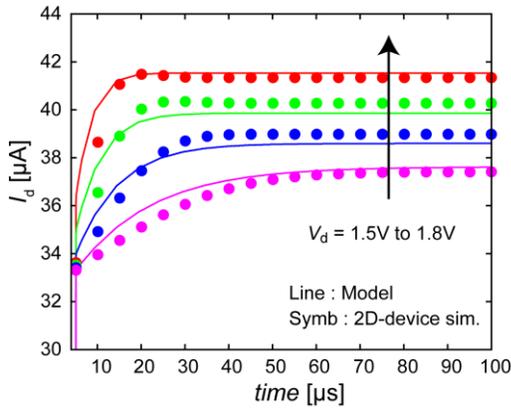


Fig. 6. Calculated drain current I_d as a function of time for four V_d values at fixed V_g to 1V.

4 CHAIN-HISTORY EFFECT

Under the dynamic operation, the time constant T_d both for charging and discharging of the stored charge in the T_{SOI} layer plays an important role. The balance between the charging and discharging also determines circuit

performances. Because it can be easily expected that a long charging delay causes the long term history effect, and a long discharging delay makes the history effect serious.

The chain-history effect is used to characterize the pulse-duration dependence of the charging/discharging carrier response. The response is measured as the delay of an inverter chain as shown in Fig. 7a. For our investigation we studied a 8 stages inverter chain. Simulation conditions are explained in Fig. 7b. The inverter delay is measured as the output signal delay to the input signal. There are two different measures, TdHL and TdLH as depicted in Fig. 7b. There are other possible two conditions, namely low start and high start. Thus four different simulation conditions (low start I: TdLH, IV: TdHL; high start II: TdLH, III: TdHL) to be investigated. Fig. 8 shows calculation results for the four conditions with the measured charging/discharging delays. For the high start, the stored charge reaches its maximum resulting in high current flow, which reduces the delay. For the low start, on the contrary, the delay increases. These two delays converge asymptotically towards the same value after many pulse inputs. The final converged delay is derived from the DC condition. Measured T_d for charging is around order of 10^{-6} s, where as that for discharging is around 10^{-2} s. This concludes that no discharging occurs under normal operation conditions but the monotonous increase of stored charge is expected. For comparison, results without the history effect is also show in Fig. 9. Since no additional charge stroge is expected without the impact ionization, the split between the high and low is diminished.

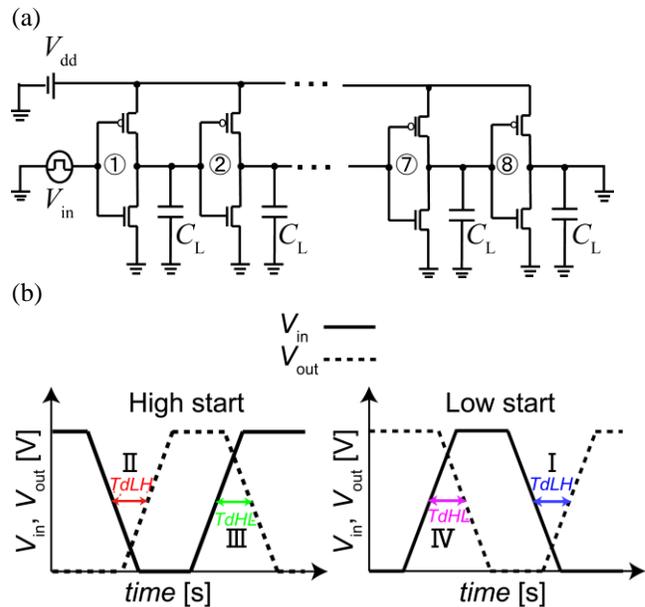


Fig. 7. (a) Test circuit for analyzing the chain-history effect, which consists of inverter stages. (b) Two different delay definitions (TdLH and TdHL) with two different bias conditions (high start and low start) requires four delay analyses.

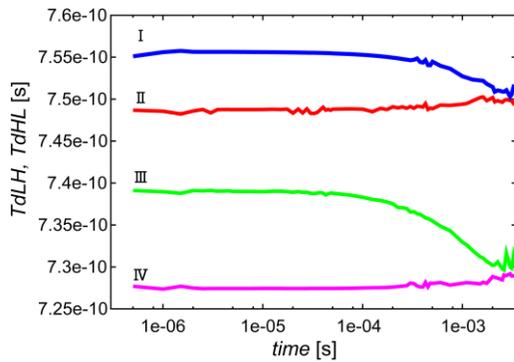


Fig. 8. Simulated chain-history effect of a fully depleted SOI-MOSFET. The line numbers (I-IV) refer to those explained in Fig. 7b

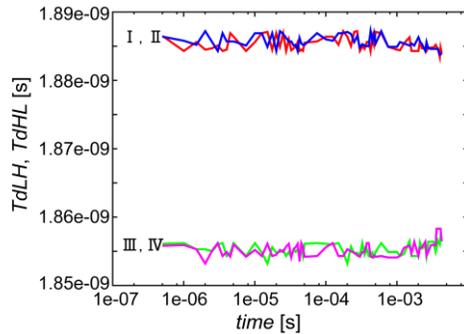


Fig. 9. The same simulation as shown in Fig. 8 but excluding the history effect.

Fig. 10 shows calculation results of the transient stored charge Q_h at the first stage of nMOSFET in the inverter chain. Since the gate voltage is high and thus the output node is set to zero, the impact ionization can be ignored resulting in the minimum Q_h . However, the low-start case results in the output node of VDD causing the impact ionization. After 10^{-4} s Q_h starts to converge. At this time the condition III and IV start to converge.

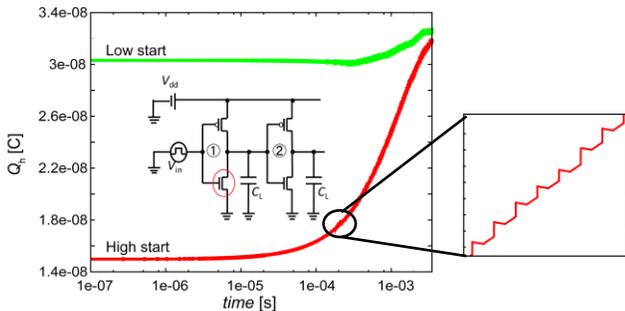


Fig. 10. Simulation results of accumulated charges Q_h as a function of pulse duration as shown in the inset.

5 DISCUSSIONS

One possibility to reduce the chain history effect is to reduce the impact ionization, which can be realized by

reducing T_{SOI} layer thickness. For the case the deep fully depleted condition spread over the whole SOI layer prevents from the accumulation condition. Fig. 11 shows 2D-device simulation results of the accumulated holes as a function of T_{SOI} . It is seen that the history effect could be diminished by reducing T_{SOI} or suppressed strongly. Fig. 12 shows calculation result of the potential change of the floating node as a function of the pulse duration time. The T_{SOI} layer thickness is reduced to 20nm instead of the studied case of 40nm. Even though T_{SOI} is reduced, the gradual increase of the floating node potential cannot be prevented. The reason is that the generated holes by the impact ionization cannot flow out from the SOI layer immediately but stays within the layer, which are continuously accumulated, because the discharging time is long in comparison to the circuit operation. This originates the long term history effect.

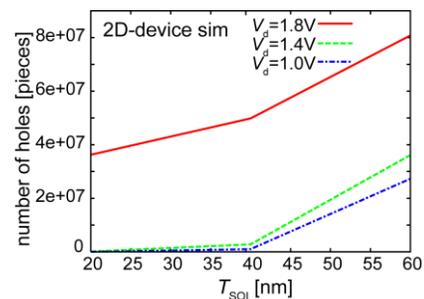


Fig. 11. 2D-device simulation results of accumulated number of holes within the SOI layer as a function T_{SOI} . The drain voltage V_d is varied.

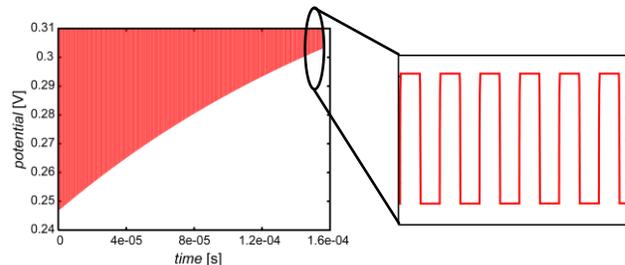


Fig. 12. Transient simulation result with HiSIM-SOI. Repetition of pulse on V_g (from zero to 1.5V) at $V_d=1.5V$ is applied as shown in the inset and the floating node potential is monitored.

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