High Accuracy Dual Side Overlay with Wet Anisotropic Etching for HAR MEMS

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ABSTRACT

Through wafer etching of silicon, using anisotropic wet chemical etchants, like KOH, is a key process in the fabrication of many types of MEMS devices. In this work, a dual side 2 mask process is used in combination with an advanced front to back side alignment system to characterize the precision of KOH through wafer etch processes by means of electrical measurements. It was found that the shift in the front to back wafer overlay (FTBO) is 2-3 µm, determined by the crystallographic tilt of the wafers. However, the 3 sigma value of the FTBO is less than 350 nm. Through wafer deep reactive ion etching (DRIE) is much more accurate but less precise; the measured FTBO shift is less than 200 nm and the 3σ FTBO is …? nm. Wet etching is more precise compared with DRIE, so when the crystal orientation of a batch of wafers is precisely known, high accuracy through wafer etch, using anisotropic wet chemical etching, is made possible in a high volume production environment.

Keywords: KOH etch, DRIE, dual side lithography, dual side overlay.

1 INTRODUCTION

For many bulk micro machined MEMS devices and technologies like 3D integration, dual side wafer lithography is a key enabling technology. Increasing aspect ratios and further lateral shrinking of device dimensions are reducing the dual side overlay budget. To meet with the advanced dual side overlay requirements, wafersteppers with dual side alignment hardware [1,2] are applied in MEMS and 3D device manufacturing .

Conventional single side overlay characterization involves the exposure of two layers in separate exposure processes but in the same photoresist film, followed by a relative position measurement of two corresponding targets in the respective layers. Usually optical techniques are used hence optical access to the corresponding targets is required. Obviously this is not possible for dual side processing on opaque wafers. And, even for transparent wafers, limited depth of focus and any non-perpendicularly off the optical axis of the overlay inspection tool can cause measurement errors. Furthermore, wafer unflatness results in non-parallel planes on corresponding front and back wafer sites and the question arises how the overlay is defined in this case (see Figure **1**).

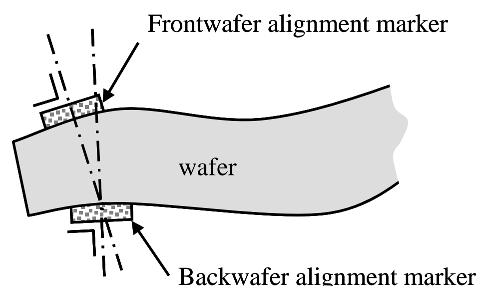

Figure 1. Potential a symmetric overlay errors due to local non planar wafers.

Overlay is one of the key metrics in device manufacturing, also for dual side processing. In devices that requires through wafer processing, not only the overlay performance of the exposure tool is important, also the performance of the through wafer etch tool or process has a significant influence on the overlay accuracy [3]. Any deep etch profile, not perpendicular to the wafer surface (angular deviation) will cause a pattern shift, proportional to the etch depth. Particularly in through wafer etching, this pattern shift results in large overlay errors between the patterns on the front side of the wafer (frontwafer) and on the backside of the wafer (backwafer). Today, high precision dual side alignment systems are available, and earlier work [4] indicates that the overlay performance of the lithographic tool is much better that the post-etch front to backwafer overlay (FTBO).

However, precise dual side alignment allows for an accurate study of the through wafer etch performance of different etch processes, like wet anisotropic etching and DRIE. The main technologies for through wafer etching are Deep Reactive Ion Etching (DRIE) and anisotropic wet etching using KOH or TMAOH solutions. In DRIE the direction of the etch profile depends on parameters like plasma conditions, gas flows and hardware layout of the DRIE tool. Because of the many coupled parameters involved, the relation between process parameters and post-etch FTBO in a DRIE process is rather complex. Anisotropic wet chemical etching, like KOH solutions, has been used as through wafer etch technology in MEMS for decades. The etching relies on the differential etch rate between the different crystal plane orientations. Hence the accuracy of the crystal orientation of the wafer will affect the resulting post etch overlay. Consequently, the accuracy

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of the through wafer etch process is dominated by two parameters: crystal plane orientation and wafer thickness.

In this work, a through wafer KOH etch is characterized in terms of post etch overlay performance and compared with the overlay obtained in a DRIE process.

2 EXPERIMENTAL

The post-etch FTBO was measured on a test device employing electrical overlay test structures. With these electrical test structures, (see Figure 2) the overlay between layer 1 and layer 2 can be measured with a precision of 15 nm (3σ) [5]. The process flow is summarized in Figure 3.

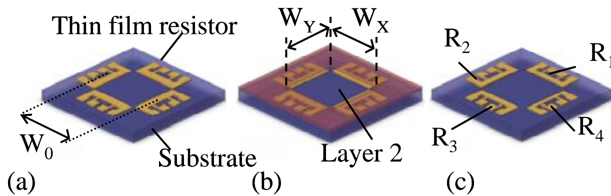

Figure 2. Principle of electrical overlay measurements. In (a) a resistor pattern is etched in a TiN (layer 1), in (b) layer 2 is exposed (b) and etched (c). The overlay of layer 2 to layer 1 is determined from electrical line width measurements on R_1, .., R_4.

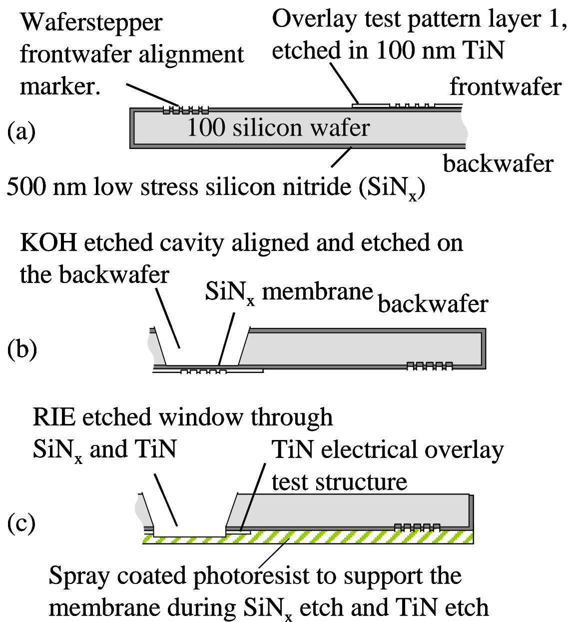

Figure 3. Process overview of the dual side overlay electrical test structures.

Wafers with electrical overlay test structures are fabricated on double side polished silicon Czochralski grown wafers, diameter 100 mm, the wafer thickness was 670 μm. As an etch mask for KOH etching, 500 nm LPCVD low-stress silicon nitride (SiN_x) was used. On the frontwafer, layer 1 of the electrical overlay test pattern was patterned (figure 3a). The conductive film required for the electrical overlay test structures was made of 100 nm PVD TiN. Because TiN is virtually not etched in KOH, no additional protective films are required during the through wafer etch. The backwafer was patterned with squares to match with the frontwafer pattern after KOH etch. The through wafer etch was performed in KOH 33% in H_2O at 85^oC (figure 3b). Each wafer was etched in a fresh prepared KOH solution. This etch stops on the SiN_x film and to transfer the KOH etch window into the resistor pattern on the front side an additional RIE etch was required. To protect the TiN films on the front side of the wafer, this side was spray-coated with photoresist and the RIE process applied on the backwafer stops into this resist layer. The overlay test devices are completed by a plasma resist removal step. A micrograph and a schematic cross section of the completed deviceis given in Figure 4.

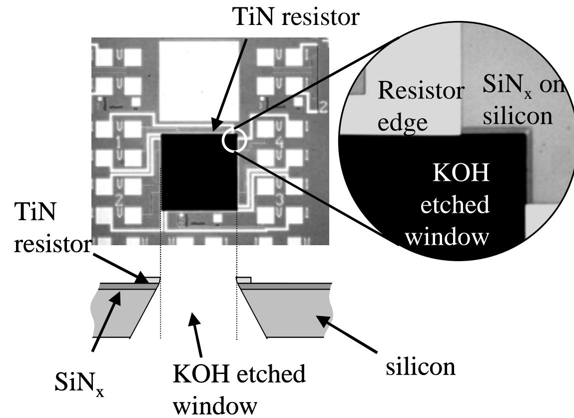

Figure 4. Micrograph and schematic cross section of the completed overlay test device.

The front side and backside exposures were performed with an ASML PAS5500 waferstepper equipped with a front-to backside alignment (FTBA) system. To minimize the contribution of lens and reticle errors to the FTBA overlay, the field size was limited 5.1x5.1 mm, this field comprises a 3x3 array of overlay test structures. The measured precision of the intra die errors like die rotation, die magnification, lens errors etc. was in this case is 31 nm and 39 nm (3σ) in X and Y respectively.

The alignment system of the ASML PAS5500 is schematically given in figure 4. For the frontwafer alignment any location on the wafer was accessible; the precision for frontwafer alignment is 9 nm (3σ). For the backwafer alignment 4 optical branches are embedded in the wafer stage to provide optical access to the alignment markers on the backside of the wafer. The precision of the backwafer alignment is 32 nm (3σ). Less compared to frontwafer alignment, but still much lower compared to the expected post-etch FTBO.

To discriminate the FTBA shift from the front to back offset caused by the crystallographic tilt (crystal shift), the backwafer pattern was exposed in two groups; group I with 0° rotation and group II with 180° rotation of the flat edge (see figure 6). By this, FTBA shift, which is associated with

the waferstepper coordinate system and crystal shift (associated with the wafer) can be numerically solved.

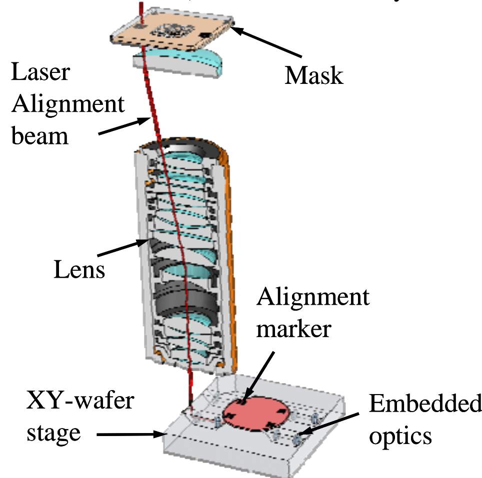

Figure 5. Schematic overview of the alignment system in an ASML PAS 5500 waferstepper. During frontwafer alignment, the markers are positioned under the alignment beam, in backwafer alignment, embedded optics project the beam under the wafer.

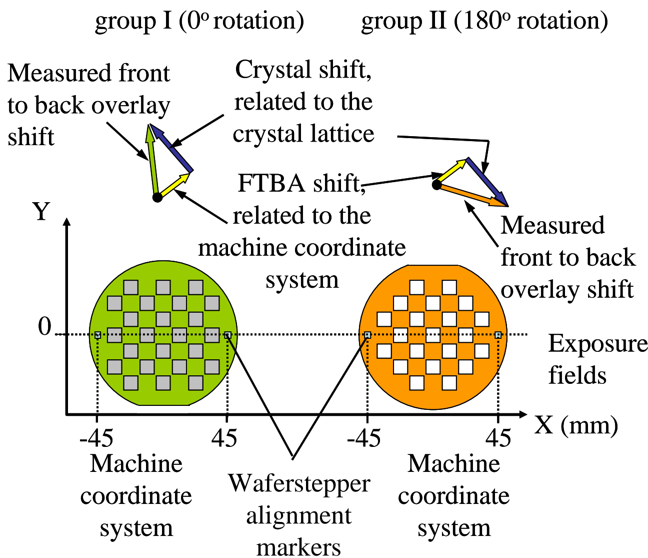

Figure 6. Schematic presentation of the double exposure method to separate FTBA shift from crystal shift.

3 RESULTS AND DISCUSSION

In dual side lithography, the alignment on the frontwafer and on the backwafer result in a theoretical grid on each wafer side. This grid is used to define the die positions for the exposures. The overlay between the frontwafer grid and backwafer grid can be described with 4 parameters; a translation in X and Y (ΔX, ΔY_A or FTBA-shift), a rotation (θ) and a scale factor (M).

Assuming that the intra die errors are negligible, any dual side overlay measurement should yield these parameters after fitting. However, in the case of KOH through wafer etch an unknown translation due to the crystal orientation, further referred to as crystal shift, must be added. θ and M are not affected by the KOH etch and can be fitted to the post-etch overlay data, to separate the FTBA shift from the crystal shift, the double exposure method was applied. The electrical overlay test structures were measured on 5 wafers, the results are summarized in Table 1.

Table 1: Measured post etch front to backwafer overlay.

Wafer nr	Rotation (°)	Measured front to back overlay (μm)				Number of data points
		X	Y	$3\sigma_X$	$3\sigma_Y$	
1	0	-0.237	2.298	0.655	0.685	462
	180	0.202	-2.457	0.814	0.616	480
2	0	-1.47	1.758	0.34	0.376	695
	180	1.464	-1.926	0.303	0.372	735
3	0	-0.205	-1.1	0.557	0.484	711
	180	0.19	0.933	0.602	0.469	716
4	0	-1.435	-2.382	0.232	0.387	752
	180	1.421	2.227	0.261	0.379	823
5	0	-0.516	0.942	0.296	0.436	738
	180	0.496	-1.128	0.33	0.399	791

The 3sigma values on the post-etch FTBO (Table 1) can be as low as 232 nm. Compared with deep reactive ion etching (DRIE) (see Figure 7) the precision of KOH etching is much better, however, the accuracy is lower.

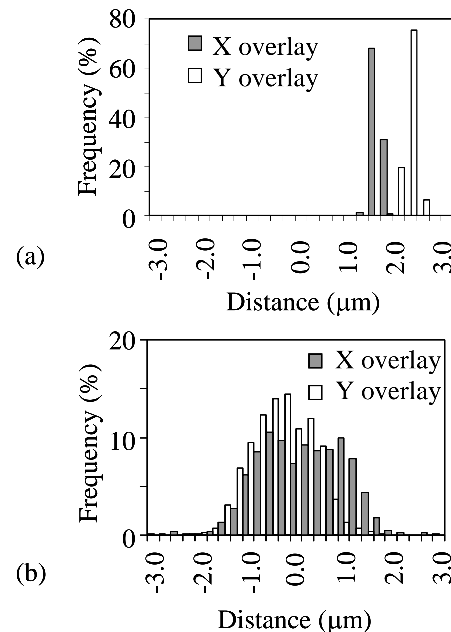

Figure 7. Front to back wafer overlay for KOH through wafer etch (a) and DRIE through wafer etch (b).

The fit parameters; ΔX, ΔY and crystal shift are given in Table 2. The average values for M is 0.075 ppm (0.433 ppm 3σ) and for θ -0.137 μrad (0.722 μrad 3σ). For

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the calculation of the crystal shift, the average FTBA shift is used.

Table 2 Calculated FTBA shift and crystal shift

Wafer nr	Rotation (^{O})	FTBA shift (μm) X	FTBA shift (μm) Y	Crystal shift (μm) X	Crystal shift (μm) Y
1	0	-0.018	-0.080	-0.228	2.381
	180			0.211	-2.374
2	0	-0.003	-0.084	-1.461	1.841
	180			1.473	-1.843
3	0	-0.007	-0.084	-0.196	-1.016
	180			0.199	1.016
4	0	-0.007	-0.078	-1.426	-2.299
	180			1.430	2.311
5	0	-0.010	-0.093	-0.507	1.026
	180			0.505	-1.044
	Average	-0.009	-0.084		
	3σ	0.049	0.052		

As can be seen in Table 2, the FTBA shift was , as expected very low hence the crystal shift was by far dominating the front to back overlay error. Furthermore, the 3σ values on the FTBA shift was very low, 49 and 52 nm respectively.

This indicates not only that, as expected, the alignment system was very reproducible, but also the KOH etch was surprisingly reproducible from wafer to wafer. Consequently, if the crystal shift can be precisely specified by the wafer manufacturer, or measured by X-ray, etch tests etc., through wafer KOH etching can be both very precise and very accurate. Furthermore, the crystal shift is a linear shift in X and Y direction and on a waferstepper, these values can be dialed in as exposure parameters. In a production environment such corrections would be feasible if the wafers are batch wise grouped from the same crystal ingot (same crystal orientation).

When DRIE is applied in through wafer etching the post-etch FTBO does not depends on crystal orientation but on process settings and tool configurations. A typical post-etch FTBO result of a through wafer etch with DRIE is given in Figure 8. The angular deviations are uniform over a diameter of about 70 mm on a 100 mm wafer. In this area, the post-etch FTBO can be modeled as a single expansion of the XY positions. In a waferstepper this can be corrected by tuning the image magnification and XY scale factor. The results of this fit is given in Table 3 and Figure 9

Table 3 FTBO with and without magnification correction

XY scale factor (ppm)	Image magnification (ppm)	Average FTBO (μm) X	Average FTBO (μm) Y	3σ FTBO (μm) X	3σ FTBO (μm) Y
0	0	0.174	-0.308	2.598	1.879
-43	-36	0.172	-0.312	1.038	1.340

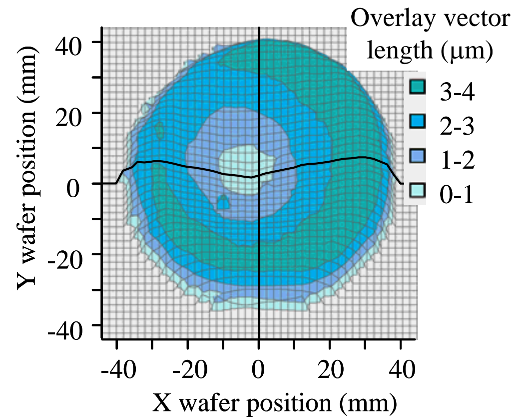

Figure 8. Effect of angular deviation in DRIE on FTBO.

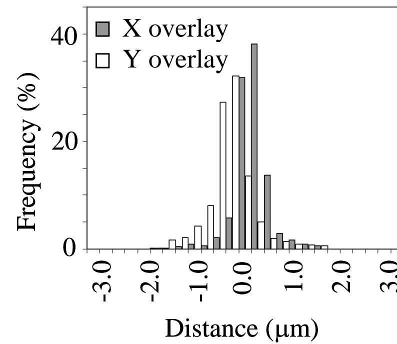

Figure 9. Front-to-Back overlay in through wafer DRIE.

4 CONCLUSIONS

The performance of a FTBA system has been experimentally verified with high accuracy, by fabrication of a dual side overlay sensitive device. Wet anisotropic etching with KOH was used to etch through a 525 μm thick wafer. This through wafer etch was surprisingly precise and can be very accurate when the crystal orientation of the silicon is known. Front to back side alignments on a waferstepper can correct for a known crystal offset making KOH through wafer etching not only precise but also very accurate.

The post DRIE FTBO can be improved by tuning the XY scale factor and image magnification, although the measured overlay is less precise compared with the KOH etch process (see Figure 7 and Figure 9).

The combination of high accuracy FTBA exposures with KOH through wafer etch on wafers with known crystal shifts will facilitate cost effective fabrication of MEMS that requires high overlay precision and accuracy.

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