High Performance ZnO-based Thin Film Transistor with High-κ Gate Dielectrics Fabricated at Low Temperature

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ABSTRACT

We report on the fabrication and characteristics of low-driven-voltage and high mobility the thin film transistors (TFTs) using undoped ZnO as an active channel layer grown by using radio frequency (rf) magnetron sputtering technique. The TFT device structure used in this study is a bottom gate type, which consists of high-κ HfO_2 film as the gate dielectric. The sputtering and post-annealing conditions of the gate insulators are optimized for leakage current and TFT performances. The device shows a low threshold voltage of 1 V, an high current on/off ratio of 1.0 $\times 10^7$, a high field effect mobility of 32.1 cm^2 / V • s, a subthreshold swing of 0.46 V/decade, and the off current of less than 10^{-12}A at a maximum device processing temperature of 280℃. The ZnO-TFT is a very promising low-cost optoelectronic device for the next generation of invisible and flexible electronics due to transparency, high mobility, and low-temperature processing.

Keywords: high performance, ZnO TFT, high-κ gate dielectrics, low temperature

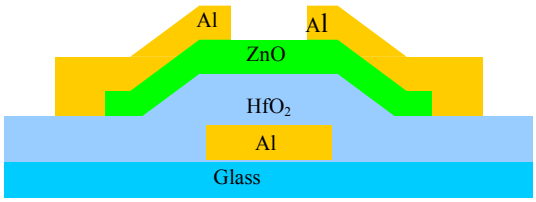
1 INTRODUCTION

In the past few years, transparent oxide semiconductor materials have gained significant attention for applications in varied fields such as photodetectors, light-emitting diodes, solar cells, thin film transistors, flat panel display (FPD), flexible display, organic light emitting diode (OLED) devices etc[1-14]. In particular, transparent Zinc Oxide (ZnO) thin film transistors (TFTs) have been considered as a potential alternative candidate to amorphous silicon (a-Si) TFTs because of their high mobilities (>10 cm^2/V•s) and low process temperature (<300 °C) [2,3]. It is well known that conventional amorphous silicon (a-Si) TFTs are not so stable under constant positive-bias stress, and their threshold voltage shift easily [9]. The low-temperature polycrystalline silicon (LTPS) TFTs show good stable electrical characteristics, but the uniformity is not good on large area substrate. Compared to conventional a-Si TFTs, ZnO-based TFTs take advantage for active-matrix organic light-emitting diode (AMOLED) displays because of their superior properties that include wide band gap, transparency, and high field effect mobility. Recently, more interest is focused on the new channel layer materials to solve the problems associated with conventional Si based TFTs such as their low field effect mobility and opacity. Moreover, great importance is given to replace the conventional Si TFTs with transparent semiconductors in order to fabricate invisible display devices.

The ZnO thin film is optically transparent in the visible regions. ZnO-based TFTs have very nice characteristics, such as low off currents, high on to off current ratios and high saturation mobilities. The performance of the ZnO is twenty times better than a-Si:H or organic semiconductors, it can be fabricated on plastic substrates at room temperature and is transparent across the whole visible spectrum. The use of ZnO TFTs could resolve some problems of flexible devices based on a-Si:H and organic semiconductors, especially the low mobilities. In this work, we report on characteristics of ZnO TFTs with high-κ HfO_2 gate dielectric fabricated by using radio frequency (rf) magnetron sputtering on glass substrates at low temperature.

2 EXPERIMENTAL PROCEDURES

The fabrication process was as follows. The TFT was fabricated on a Corning glass 7740 substrate cleaned with acetone, methanol, and deionized water, in that order. A 50-nm-thick Al gate electrode was deposited by sputtering and patterned by conventional lithography process. Then, a 40-nm-thick HfO_2 gate dielectric was deposited by sputtering. The active layer of a 60-nm-thick ZnO film was deposited by radio frequency (rf) magnetron sputtering at room temperature to form the channel layer. Al was then sputtered to form the source and drain electrodes. The channel and source/drain contacts were patterned using shadow masks. This TFT has a channel width of 10μm and channel length of 10 μm. The samples of ZnO TFTs were annealed in O_2 under annealing temperatures 280℃ for 60 minutes. The electrical characteristics of samples were measured at room temperature using Agilent 4156C semiconductor parameter analyzer. A diagram of the ZnO-based TFT structure and a photograph of the ZnO-based TFT on the glass described here are shown in figures 1(a) and (b), respectively. The photograph shows that the underlying color image can be seen clearly through the ZnO-based TFT on the glass substrate, demonstrating the high transparency of the ZnO thin film, so that, the high transparency ZnO thin film was gained.



(a)

(b)

Figure 1. (a) A schematic cross section and (b) Photograph of ZnO-based TFT

3 RESULTS AND DISCUSSION

The X-ray diffraction (XRD) spectrum of ZnO thin films deposited at room temperature by radio frequency (rf) magnetron sputtering is showed in the figure 2. XRD spectrum presents intense peak of (002) orientation of the wurtzite structure. The dominant peak of XRD pattern of ZnO thin film on glass substrates is located at $2\theta = 34.2^{o}$. The diffraction peak of metallic Zn was not detected by XRD for the samples. The XRD pattern indicates highly oriented crystallographic growth of ZnO films with c-axis perpendicular on glass substrate. The surface free energy is the smallest on the (002) surface of ZnO and hence the thin films tend to grow along it.

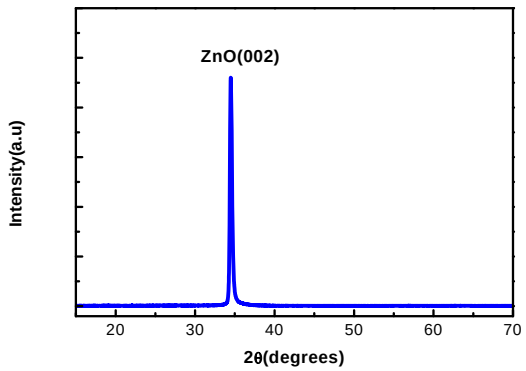


Fig. 2. XRD pattern of ZnO thin films deposited by sputtering

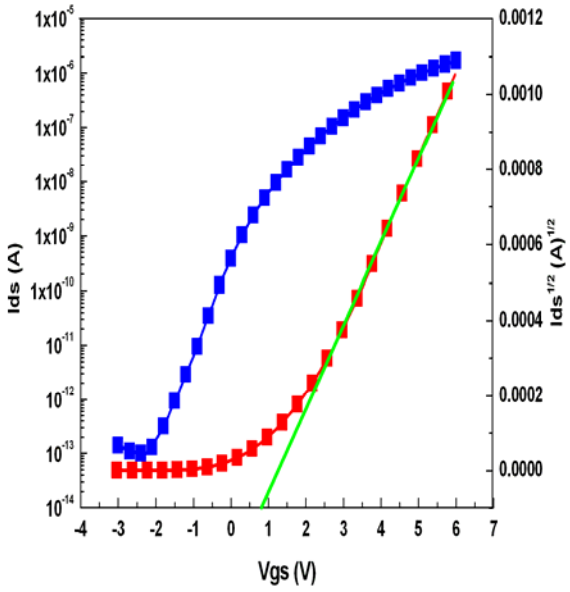


Fig. 3. drain current–gate voltage (I_{ds}–V_{gs}) curves for ZnO-based thin-film transistor

Typical drain current (I_{ds}) - gate voltage (V_{gs}) transfer characteristics of ZnO-based TFTs are portrayed in figure 3. It is observed that the ZnO-TFT operate as an n-channel enhancement mode device, because that a positive gate voltage is required to induce a conducting channel, and that the channel conductivity increases with increasing positive gate bias. Enhancement mode is preferable to depletion mode behavior because application of a gate voltage is required to turn the transistor off and circuit design is easier and power dissipation is minimized when enhancement-mode transistors are employed [10]. A high I_{ds} (2uA) is obtained for V_{gs} =5 V and V_{ds}=1 V. Besides that a nice pinch-off and current saturation is clearly observed indicating that this ZnO-TFT is in accordance with the standard theory of field effect transistors. The saturation mobility and the threshold voltage (V_{th}) were calculated by fitting a straight line to the plot of the square root of Ids versus V_{gs}, according to the expression (saturation region) [11]:

$$I_{ds} = \left(\frac{C_i \mu_{sat} W}{2L}\right)\left(V_{gs} - V_{th}\right) \qquad V_{ds} > V_{gs} - V_{th} \quad (1)$$

where C_i is the capacitance per unit area of the gate insulator. W and L are the width and length of the channel, respectively. The obtained μsat is 32.1 cm^2 /V•s and the Vth is 1 V, showing that the ZnO-TFT operates in the enhancement mode. Enhancement mode is preferable to

depletion mode since it is not necessary to apply a gate voltage to switch off the transistor, because the circuit designer is simpler and the power dissipation is lower. The high value of μsat deals with the high quality (improved crystallinity and low oxygen vacancies and/or Zn interstitials working as donors) presented by the ZnO layer as well as the good channel-insulator interface obtained. The magnitude obtained for the Vth is directly proportional to the gate insulator thickness. So, these values could be easily reduced by reducing the gate insulator thickness. The off-current is low, on the order of 10^{-13} A, and the on/off ratio is 10^7. The gate voltage swing, S, defined as the voltage required to increase the drain current by a factor of 10, is given by

$$S = \frac{dV_{gs}}{dLogI_{ds}} \quad (2)$$

and was 0.46V/decade for the ZnO-TFT under analysis. The S is given by the maximum slope in the transfer curve [figure 3].

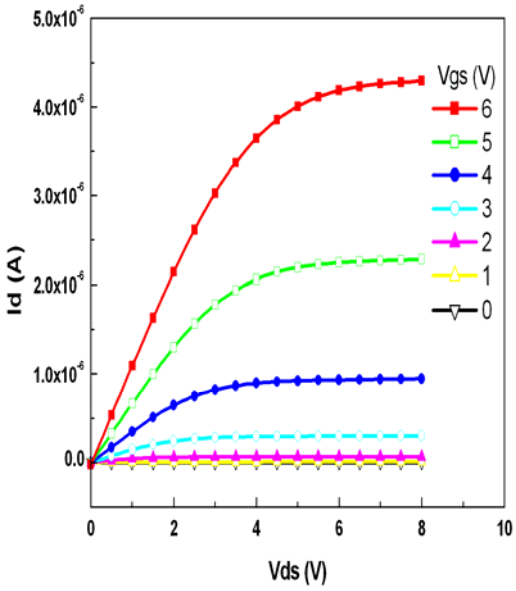
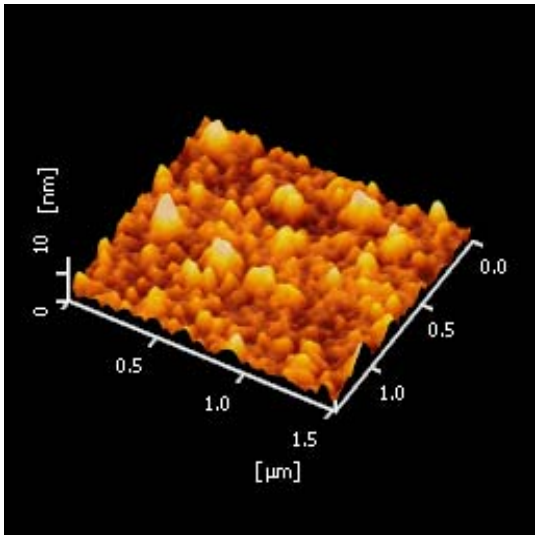


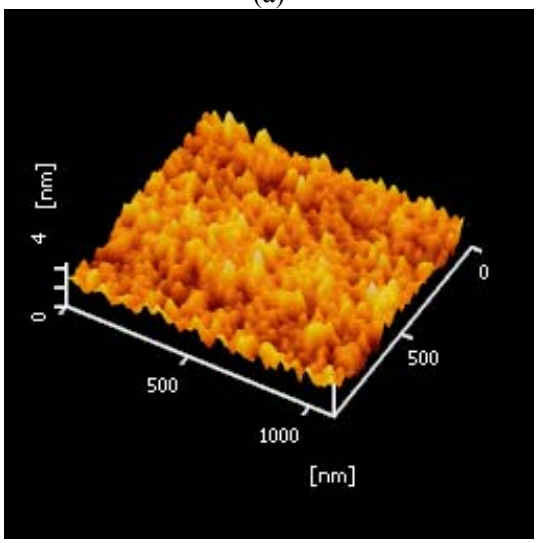
Fig. 4. drain current–drain voltage (I_{ds}–V_{ds}) curves for ZnO-based thin-film transistor

Figure 4 displays the I_{ds} current curves as a function of the drain voltage V_{ds} for different V_{gs}. The saturation was about 4.5uA under a gate bias of 6 V. Besides the high value obtained for the saturation current, the device exhibits "hard" saturation, evidenced by the flatness of slope of each Ids curve, for large V_{ds}. This indicates that the entire thickness of the ZnO channel layer is depleted. This type of behavior is very desirable for most circuit applications, since transistors exhibiting this property have large output impedance.

The two essential TFT materials components are the ZnO semiconductor and HfO_2 the gate dielectric. The influence of the dielectric roughness on the performance of ZnO devices has been reported in some papers [12]. The three-dimensional (3D) view of the surface morphology of HfO_2 gate dielectric is shown in figure 5(a). It is observed that the grains grow uniformly with homogenous distribution. The root-mean-square (rms) surface roughness of HfO_2 thin films is 0.997nm. The smooth gate dielectric surface plays a very important role for ZnO-based TFT because it could induce much less interface defects and improve the performance and stability of devices. The three-dimensional (3D) view of the surface morphology of ZnO thin film is shown in figure 5(b). The root-mean-square (rms) surface roughness of ZnO thin film is only 0.941nm. The very smooth thin film surface is in favor of fabrication of high quality ZnO-based TFT.



(a)



(b)

Fig.5. (a) Three-dimensional (3D) AFM of HfO_2 gate dielectric thin film. (b) Three-dimensional (3D) AFM of ZnO thin film.

4 CONCLUSIONS

In summary, we have fabricated ZnO-based thin-film transistors (TFTs) on glass substrates by radio frequency (rf) magnetron sputtering. The structural characterization of ZnO thin films were studied by X-ray diffraction (XRD). The X-ray diffraction measurements show that the films had high crystalline quality. The electrical properties of the ZnO-based thin-film transistors were investigated by drain current–drain voltage and drain current–gate voltage measurements. The results show the low-driven-voltage and high mobility ZnO TFT is gained. The TFT shows a low threshold voltage of 1 V, a high on/off ratio of 1.0×10^7, a high field effect mobility of 32.1 cm^2 /V•s, a subthreshold swing of 0.46 V/decade, and a low off current of 10^{-13} A. The maximum device annealing temperature is 280℃. Therefore, the ZnO TFTs have revealed the potentials for future invisible and flexible electronics.

5 ACKNOWLEDGMENT

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