Modeling and Analysis of MOS Capacitor Controlled by Independent Double Gates

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ABSTRACT

This paper, for the first time, explores the characteristics of MOS capacitor controlled by independent double gates by numerical simulation and analytical modeling for its possible use in RF circuit design as a varactor. By numerical simulation it is shown how the quasi-static and non-quasi-static characteristics of the first gate capacitance could be tuned by the second gate biases. Effect of body doping and energy quantization are also discussed in this regard. A semi-empirical quasi-static model is also developed by using the existing incomplete Poisson solution of independent double gate transistors. Proposed model, which is valid from accumulation to inversion, is shown to have excellent agreement with numerical simulation for practical bias conditions.

Keywords: Compact Modeling, MOS Capacitors, Doubel Gate MOSFETs, Varactors

1 Introduction

Voltage controlled oscillators (VCOs) based on metal oxide semiconductor (MOS) varactors have became an integral part of RF communication circuits [1]-[4]. As the Double gate (DG) MOSFETs have appeared as replacement for bulk-MOSFETs in sub-32 nm technology nodes, it is important to analyze the performance of DG-MOS based varactors. While the characteristics of a tied double gate MOS capacitor is not expected to be much different from that of the bulk-MOS capacitor, an independently controlled double gate based MOS capacitor can bring out new functionalities, which could be interesting for RF circuit applications. However, to our best knowledge, characteristics of an independently controlled DG-MOS capacitor have not yet explored through numerical simulation or analytical modeling.

In the first part of this paper, with the help of professional 2D numerical device simulator [5] we study how second gate voltage modulates the quasi-static and non-quasi-static capacitance of the first gate. The effect of doping and quantum-confinement is also discussed in this regard. The second part of the paper focuses on the compact modeling issues of such capacitor. Effort has been put to develop a semi-empirical analytical model for the quasi-static capacitance, which is valid from accumulation to inversion. Proposed model is shown to have excellent agreement with numerical device simulator for practical range of applied biases.

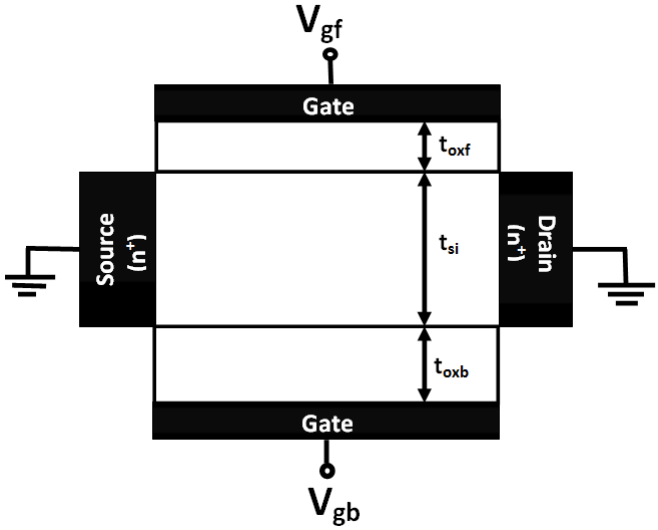

Figure 1: Schematic diagram of IDG based MOS Capacitor. t_{oxf}, t_{oxb}, and t_{si} are the front-gate oxide , back-gate oxide and Si body thickness respectively

2 NUMERICAL ANALYSIS

The schematic of an n-type undoped body Independent Double Gate (IDG) based MOS capacitor is shown in Figure 1. Here source and drain are grounded. The main objective of this work is to study how the first gate capacitance defined by $C_{gf} = \frac{\partial Q_{gf}}{\partial V_{gf}}|_{V_{gb}}$ gets modulated with the presence of second gate voltage (it is imperative that the device will behave as bulk-MOS capacitor when the second gate is grounded). Here Q_{gf} is the charge density at the front-gate and $V_{gf(b)}$ is the effective front(back)-gate voltage. For this study we use ATLAS TCAD tools [5] and for generalization asymmetric gate oxide configurations.

In Fig. 2 we have demonstrated the quasi-static characteristics of the front gate capacitance for different values of back gate voltages. Buy applying suitable back gate voltage, one can change the electron and hole concentration of the Silicon body and thus can alter the first gate capacitance. Fig. 3 shows the percentage change of the front gate capacitance (from the value when the back gate is grounded) for

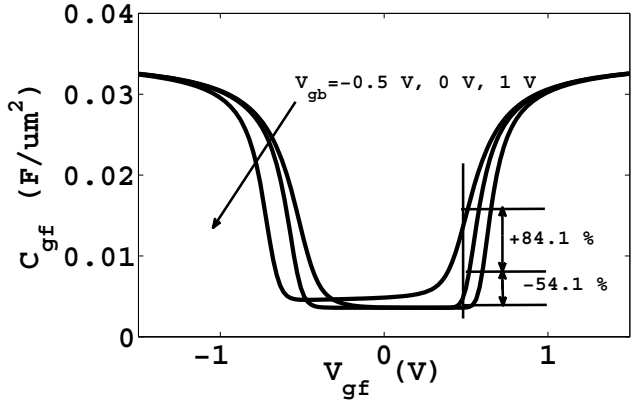

Figure 2: Quasistatic MOS capacitance for the device parameters $t_{si} = 20\,nm$, $t_{oxf} = 1\,nm$, $t_{oxb} = 2\,nm$.

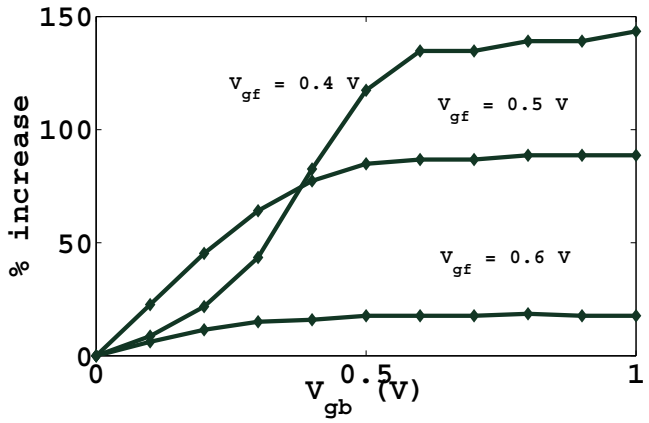

Figure 3: Precentage change in *quasistatic* MOS capacitance with change in the second gate voltage V_{gsb} at given first gate volatges V_{gsf} for the device parameters $t_{si} = 20\,nm$, $t_{oxf} = 1\,nm$, $t_{oxb} = 2\,nm$.

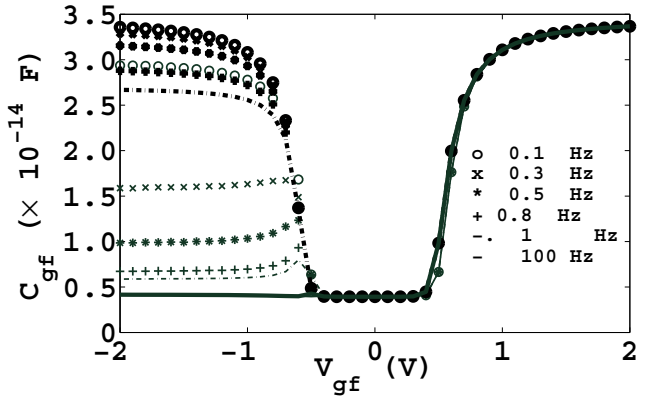

Figure 4: Behaviour of MOS capacitor with gate voltages of different ac frequencies for the device parameters $t_{si} = 20\,nm$, $t_{oxf} = 1\,nm$, $t_{oxb} = 2\,nm$. *Thin* symbols indicate $V_{gsb} = 0\,V$ and *thick* symbols indicate $V_{gsb} = 0.2\,V$.

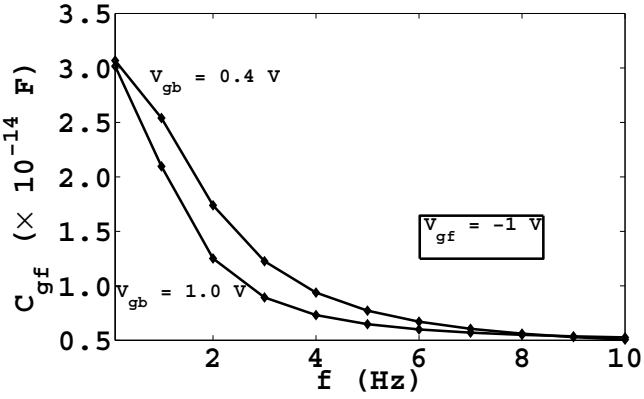

Figure 5: Dynamic tunning of MOS capacitor by the variation of the second gate voltage V_{gsb} for the device parameters $t_{si} = 20\,nm$, $t_{oxf} = 1\,nm$, $t_{oxb} = 2\,nm$.

different back gate biases. Such kind of tunability can not be achieved in bulk transistor and thus IDG-MOS capacitor can bring out new functionalities in RF circuit design. Fig. 4 shows the non-quasi static characteristics of the MOS capacitor at different ac frequencies. As the electrons are majority carriers, when body is in depletion and inversion region the front gate capacitance is almost independent of frequencies of the ac signal applied to the gate. However in accumulation (of hole) regime the capacitance exhibited is frequency dependent. Similar to quasi-static characteristics, the second gate of the IDG based MOS capacitor offers dynamic tunability to the device. The value of the front gate capacitance in accumulation regime increases for a particular frequency with the increase of the back gate voltage (due to the increase of majority carrier, electrons in Silicon body). This property could be used to compensate the degradation of front gate capacitance due to frequently rise by tuning the back gate voltage (for example note the superimposition of the capacitances at 0.1 Hz for the second gate bias of 0 V with the capacitances at 0.8 Hz for second gate bias of 0.2 V). The change of first gate capacitance with frequency for different second gate voltage is shown in Fig. 5. We have also studied the effect of energy quantization effect of and doping on IDG-MOS capacitance.

3 ANALYTICAL MODELING

It is important to develop time-dependent surface potential based compact models for successful implementation of IDG-MOS varactor in RF circuit design [6]-[7]. However the compact modeling of IDG MOS capacitor is a difficult task as the analytical solution of complete (considering both electron and hole concentration) Poisson equation (PE) is unavailable . Zhou *et. al.* [8] recently proposed a rigorous solution of the full PE for the undoped symmetric double-gate MOS capacitor in terms of *Legendre's incomplete elliptic integral of first kind* and thus is not practical for circuit simulation purpose as such function is not available in

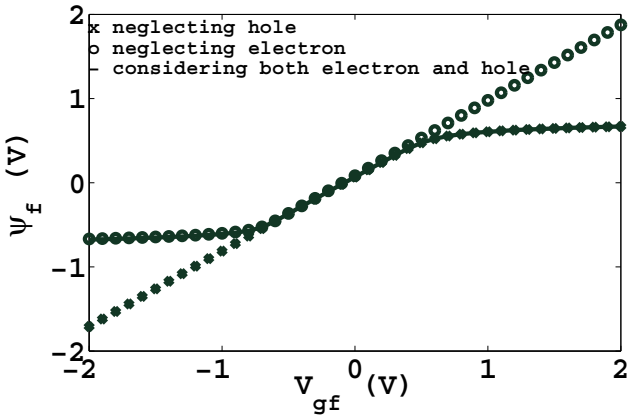

Figure 6: Front-gate surface potential at the back-gate bias $V_{gb} = 0.8V$ for the device parameters $t_{si} = 20\,nm$, $t_{oxf} = 1\,nm$, $t_{oxb} = 2\,nm$.

standard 'C' or 'Verilog-A' library. It should be noted that analytical solution of the PE for IDG MOS capacitor considering only electron/hole itself is very complicated [9]. By using similar approach to [8], one might come up with some analytical solution for full Poisson equation for IDG MOS capacitor, but its implementation in a circuit simulator will definitely be questionable. In this paper, using our previous incomplete Poisson solution (which considers either electron or hole concentration), [9] , we propose a semi-empirical surface potential based quasi-static model for IDG MOS capacitor, which is valid from accumulation to depletion. The modeling methodology is described below. The complete PE for the undoped body long-channel IDG MOS capacitor is given by

$$\frac{\partial^2 \psi}{\partial y^2} = \frac{qn_i}{\varepsilon_{si}}\{e^{\beta\psi(y)} - e^{-\beta\psi(y)}\} \tag{1}$$

with the general boundary conditions for IDG

$$-\frac{d\psi(y)}{dy}\Big|_{y=\frac{-t_{si}}{2}} = \frac{C_{oxf}}{\varepsilon_{si}}(V_{gf} - \psi_f) \tag{2}$$

$$-\frac{d\psi(y)}{dy}\Big|_{y=\frac{t_{si}}{2}} = \frac{C_{oxb}}{\varepsilon_{si}}(\psi_b - V_{gb}) \tag{3}$$

Where q is the elementary charge, n_i the intrinsic carrier density, $C_{oxf(b)}$ the oxide capacitance per unit area of front(back)-gate defined as $\varepsilon_{ox}/t_{oxf(b)}$, ε_{si}, ε_{ox} are the permittivities of Silicon and SiO_2 respectively. β the inverse thermal voltage, $\psi_{f(b)}$ Si/SiO_2 interface potential at $y = \mp t_{si}/2$ with $y = 0$ being the center of the Si film, and finally $V_{gf(b)}$ is the effective front(back)-gate voltage *i.e.*, $V_{gf(b)} = V_{gf(b)applied} - \Delta\phi_{f(b)}$, where $\Delta\phi_{f(b)}$ is the work function difference at the respective gates.

The analytical solution of this PE does not exist. Let us consider ψ_{fe} and ψ_{fh} are the front gate surface potentials when we completely neglect the hole and electron concentration respectively. ψ_{fe} and ψ_{fh} could be expressed by single implicit equation [9] and an efficient solution technique for solving these equations are recently proposed in [10]. In Fig. 6, ψ_{fe} and ψ_{fh} are plotted as a function of V_{gf} along with ψ_f (the front gate surface potential considering both electron and hole). One can see that in strong inversion $\psi_f \simeq \psi_{fe}$ and in strong accumulation $\psi_f \simeq \psi_{fh}$. However in the weak inversion regime $\psi_{fe} \simeq \psi_{fwi}$, where ψ_{fwi} is the surface potential at the front-gate when body is in weak inversion and neglecting all mobile charges it could expressed as

$$\psi_{fwi} = V_{gf}\frac{1}{1+\frac{C_{oxb}C_{si}}{C_{oxf}C_{si}+C_{oxf}C_{oxb}}} + V_{gb}\frac{1}{1+\frac{C_{oxf}C_{si}+C_{oxf}C_{oxb}}{C_{oxb}C_{si}}} \tag{4}$$

Joining ψ_{fe}, ψ_{fh}, ψ_{fwi} using suitable interpolating function we propose the model for ψ_f as follows:

If $V_{gb} > 0$ and $V_{gf} > 0$

$$\psi_f = \psi_{fe} \tag{5}$$

Else if $V_{gb} > 0$ and $V_{gf} < 0$

$$\psi_f = \frac{\psi_{fh} + \psi_{fe}e^s}{1+e^s} \tag{6}$$

where $s = -\zeta + \log(\psi_{fh} - \psi_{fwi} + \varepsilon)$, $\zeta = mV_{gb} + c$, $m = \frac{\zeta_1 - \zeta_2}{V_{gb2} - V_{gb1}}$, $c = \frac{\zeta_1 V_{gb2} - \zeta_1 V_{gb1}}{V_{gb1} - V_{gb2}}$. Here $\zeta_1 = 6$, $\zeta_2 = 4.5$, $V_{gb1} = -0.5$, and $V_{gb2} = 1.2$ are fitting parameters and whereas ε is the machine precision and for a long double data-type, it is equal to $2^{-52} \approx 2.3 * 10^{-16}$.

If $V_{gb} < 0$ and $V_{gf} < 0$

$$\psi_f = \psi_{fh} \tag{7}$$

Else if $V_{gb} < 0$ and $V_{gf} > 0$

$$\psi_f = \frac{\psi_{fe} + \psi_{fh}e^s}{1+e^s} \tag{8}$$

where $s = \zeta + \log(\psi_{fwi} - \psi_{fe} + \varepsilon)$ and $\zeta = m(-V_{gb}) + c$. m and c are given as above. Using the surface potential thus obatined, Q_{gf} is first calculated ($Q_{gf} = C_{oxf}(V_{gf} - \psi_f)$), which is then used to obtain C_{gf} numerically. The proposed model is validated against the professional device simulator ATLAS and excellent agreement is observed as shown in Figs. 7 and 8 for diferent device geometries. However due to the semi-empirical nature, the proposed model is found to loose its accuracy for $|V_{gb}| > 1V$. Since the DG MOS transistors are expected to be operated under 1 Volt bias conditions, such limitations could be acceptable. The quantum effect could be included by the 'surface potential perturbation' technique as explained in [11].

It should be noted that one need to develop non-quasi-static (or time dependent) capacitor model for proper utilization of IDG MOS capacitor in RF circuits. The nature of complete Poisson solution for bulk MOS capacitor is such that one can separate the positive (from the hole) and negative (from the electron) charges from the total charge expression, which allows to apply RTA (relaxation time approximation)

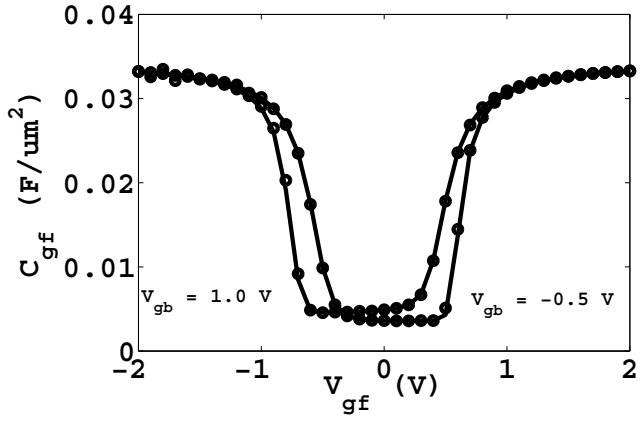

Figure 7: *Quasistatic* MOS capacitance for the device parameters $t_{si} = 20\,nm$, $t_{oxf} = 1\,nm$, $t_{oxb} = 2\,nm$. Straight lines represent *model* and circles represent TCAD simulations.

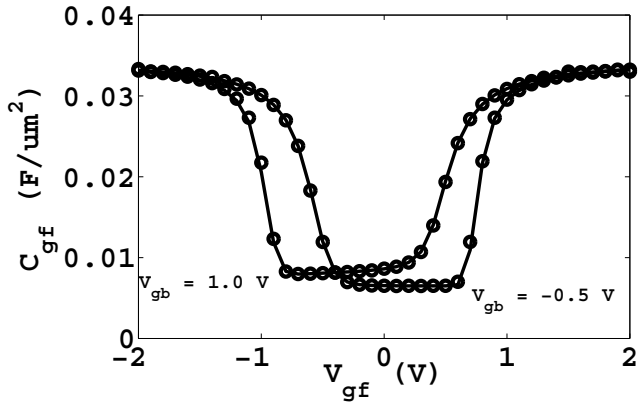

Figure 8: *Quasistatic* MOS capacitance for the device parameters $t_{si} = 10\,nm$, $t_{oxf} = 1\,nm$, $t_{oxb} = 1\,nm$. Straight lines represent *model* and circles represent TCAD simulations.

in order to develop time dependent model [6]. Therefore due to unavailability of suitable complete Poisson solution, it appears to be a very difficult task to develop non-quasi-static model for IDG MOS capacitor. However the proposed quasi-static model will enable the design to explore novel RF circuit design possibilities using the unique charcatersitics of IDG MOS capacitor.

4 CONCLUSIONS

Based on numerical simulation and analytical modeling, the characteristics of MOS capacitor controlled by independent double gates are explored for its possible use in RF circuit design as a varactor. As the numerical simulation results show, the quasi-static and non-quasi-static characteristics of the first gate capacitance can be tuned by the second gate biases. Also the effect of body doping and energy quantization is discussed . Using the existing incomplete Poisson solution of independent double gate transistors, a semi-empirical quasi-static model is developed. The proposed model, which is valid from accumulation to inversion, is shown to have excellent agreement with numerical simulation for practical bias conditions.

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