Impact of Channel Length and Gate Width of a n-MOSFET Device on the Threshold Voltage and Its Fluctuations in Presence of Random Channel Dopants and Random Interface Trap: A 3D Ensemble Monte Carlo Study

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ABSTRACT

Previously we have reported the correlation in the threshold voltage fluctuations caused by (1) the presence of random number and random distribution of dopant ions in the channel region of a 45 nm n-MOSFET and, (2) single interface trap positioned at random from source to drain of the *n*-MOSFET. In past work we have also supplemented the numerical simulations by results obtained with the usage of existing analytical models [1-4]. From the knowledge of random telegraph noise (RTN) based device physics data pertaining to scaled devices, it can be speculated that, as the gate width and the channel length are increased, the fluctuations in threshold voltage variations tend to decrease to manageable levels aiding in reliable device performance for both analog and digital ICs with long-term operational characteristics. The Ensemble Monte Carlo (EMC) device simulation results presented in this paper for a 70 nm gate length and 90 nm gate width *n*-MOSFET device confirm the above findings.

Keywords: random dopant fluctuations, random interface trap, threshold voltage variations, 3D Monte Carlo device simulations, channel length and gate width scaling.

1 INTRODUCTION

Random telegraph noise or random telegraph signal fluctuations (RTN/RTS) manifest themselves as fluctuations in transistor threshold voltage (V_T) and saturation drive current due to single-electron trapping/detrapping events near the $Si:SiO_2$ interface. The RTN amplitude has been shown to not only to increase with the reduction of device dimensions, but also depends on the bias conditions at gate and drain terminals, trap's position at the interface along the channel from source to drain, and substrate doping due to the non-uniform inversion layer thickness caused by the atomistic nature of the dopants. The large fluctuations in threshold voltage and transistor saturation drive current as manifested by RTN amplitudes have shown to cause RTN instabilities affecting the miniaturization of cell dimensions following the development of sub-90 nm Flash technologies. For instance, RTS amplitude variation as high as 60% has been reported experimentally [5] taking into account the device scaling, especially for the case of ultra-narrow gate width MOSFET, as is expected from the ITRS projections. Apart from the reliability concerns of flash memory mentioned above, both dynamic and static random access memories will suffer greatly from extremely stringent threshold voltage (V_{th}) control window requirements resulting in read/write access time failures. The examination of the impact of RTN on presently manufactured highly scaled devices is very important as a single or few discrete charges trapped in the defect states lying near the substrate-oxide interface are sufficient to cause significant performance degradation in sub-100 nm channel length MOSFETs.

The impact of device scaling in both gate length and gate width of an *n*-MOSFET is significant with regard to the magnitude of the threshold voltage fluctuations and the drain current fluctuations induced RTS amplitudes. Since the total number of discrete and random channel dopant distribution scales with effective gate area, for a more aggressively scaled channel length and ultra narrow gate width, a fewer number of dopant atoms exists in the active channel region of the MOSFET. The random trapping and detrapping of inversion carriers by an interface trap will give more drastic fluctuation spikes in the RTS amplitude owing to voltage conditions at the gate and drain contacts with the bias effect being more pronounced in near threshold or sub-threshold operation of the *n*-MOSFETs. For larger gate area devices in the vicinity of sub-100 nm technology node, the number of actual dopants, although still discrete and random in position, is increased so that trapping/detrapping effect by interface traps will be less pronounced at weak to moderate inversion bias conditions at gate and drain terminals of the *n*-MOSFET. The purpose of this paper is to demonstrate this feature by comparing a 45×50 nm^2 *n*-MOSFET device with a 70×90 nm^2 *n*-MOSFET device simulation study using 3-D Ensemble Monte Carlo (EMC)/Molecular Dynamics device simulations [6].

2 THEORETICAL MODEL AND DEVICE STRUCTURES BEING CONSIDERED

The 3-D EMC device simulator used in this study is described in details in Ref. [6], and can be utilized for analysis of arbitrary geometry sub-100 nm devices. The inclusion of the proper Coulomb interaction significantly affects both the energy and momentum relaxation processes of the carriers in the channel region of the device and also

has significant impact on the device output characteristics. We have used the corrected Coulomb approach [6] to account for the short-range electron-electron (e-e) and electron-ion (e-i) interactions.

In the analysis, we have modified device parameters, such as oxide thickness and mean substrate doping values as per ITRS projections for 45 nm and 70 nm technology node. The gate width for 45 nm device is 50 nm and the corresponding one for the 70 nm device is 90 nm. We have considered a set of 20 different channel dopant profiles (for both device dimensions) that correspond to 20 different numbers of impurities in the active channel region of the device with different distributions of the impurity atoms.

3 SIMULATION RESULTS

Figure 1 shows the threshold voltage values for different random dopant type and configurations for 70×90 nm^2 n-MOSFET device as a function of different drain biases. The average of V_{th} for this device as extracted from the EMC simulation for the cases of V_{ds} = 0.2V, 0.3V, 0.4V and 0.5V are 0.1551V, 0.2203V, 0.2080V and 0.3011V, respectively. The standard deviation of V_{th} (σV_{th}) for this device for the cases of V_{ds} = 0.2V, 0.3V, 0.4V and 0.5V are 0.0228V, 0.0279V, 0.0250V and 0.0176V, respectively. From the threshold voltage data it is evident that with the increase of drain bias, the average threshold voltage values are shifted upwards. However, the threshold voltage spread is higher for lower drain biases. This is attributed to the fact that as the drain bias is increased, electrons travel with a larger average velocity in the channel, thus spending less time in the vicinity of the impurities, which in turn leads to smaller overall importance of Coulomb scattering.

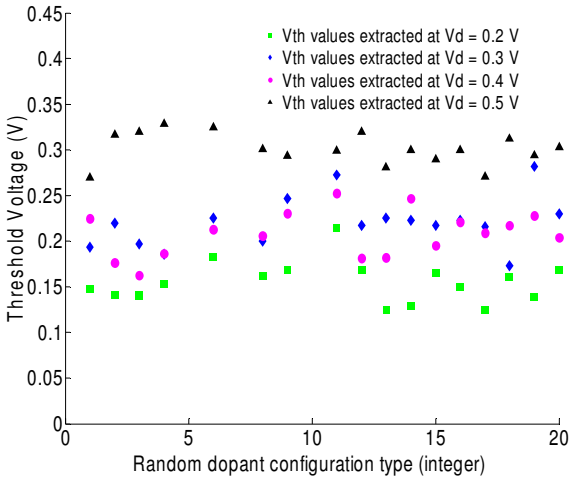

Figure 1: Threshold voltage distribution as a function of different random channel dopant configuration for a 70×90 nm^2 device.

Figure 2 shows the threshold voltage fluctuations at three different interface trap positions showing the impact of drain voltage bias conditions for a 70×90 nm^2 device. The traps are positioned at 9 nm (closer to source edge), 37 nm (near the middle of the channel) and 62 nm (near the drain edge). To maximize the effect of the traps, the traps are all located in the middle of the gate width (45 nm). The standard deviation of the threshold voltage induced by a trap (ΔV_{th}) for these three trap positions at drain biases of 0.2V, 0.3V, 0.4V and 0.5V are 0.001V, 0.0044V, 0.0018V and 0.0047V, respectively. The average V_{th} fluctuations measured in percentage for these drain bias conditions taking the three trap positions into considerations are 14.66%, 9.58%, 8.82% and 6.63%, respectively. These results show the important impact of RTS as revealed by threshold voltage fluctuations for different drain bias conditions at threshold. The results presented in Figure 2 clearly show higher fluctuations in threshold voltage deviations in the presence of trap for lower drain bias conditions. As the drain bias is increased, the fluctuation percentages steadily decline. At lower drain bias (in the range of 200 mV or lower), the drift field along the channel is too weak to cause the carriers injected from the source to drift with high velocity. As the carrier drift velocity is lower short-range Coulomb force interactions play significant role. When the drain bias increases, the electric field increases and the Coulomb interaction is considerably suppressed resulting in smaller threshold voltage variation.

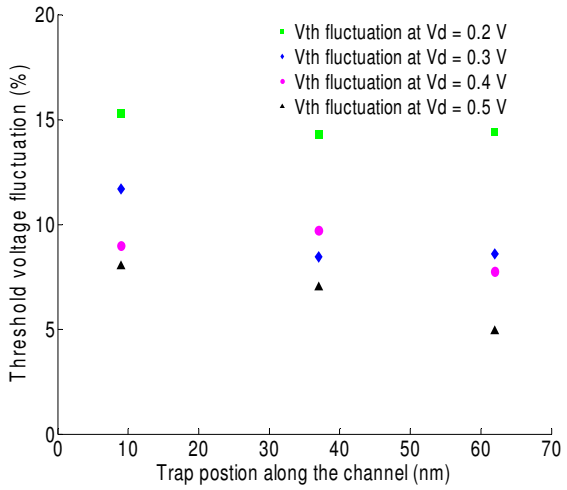

Figure 2: Threshold voltage fluctuations at three different interface trap positions showing the impact of drain voltage bias conditions for a 70×90 nm^2 device.

Figure 3 shows comparison of threshold voltage values for different random dopant type configurations and for a drain bias of 0.5 V. The impact of device scaling is illustrated on the examples of 70×90 nm^2 and 45×50 nm^2 *n*-MOSFET devices. The average threshold voltage values for all different statistical random dopant configurations for the two device dimensions are 0.30V and 0.13V, respectively. This follows the normal threshold voltage roll-off condition with decreased channel length. The standard deviation of

the threshold voltage values, as estimated from EMC simulation results, are 0.018V and 0.039V, respectively. This shows a distinctive feature of random channel dopant fluctuations (RDF) effect with increasing device scaling where the scatter in threshold voltage fluctuations caused by RDF is more pronounced for shorter gate length and narrower gate width device, i.e., for 45×50 nm^2 *n*-MOSFET device.

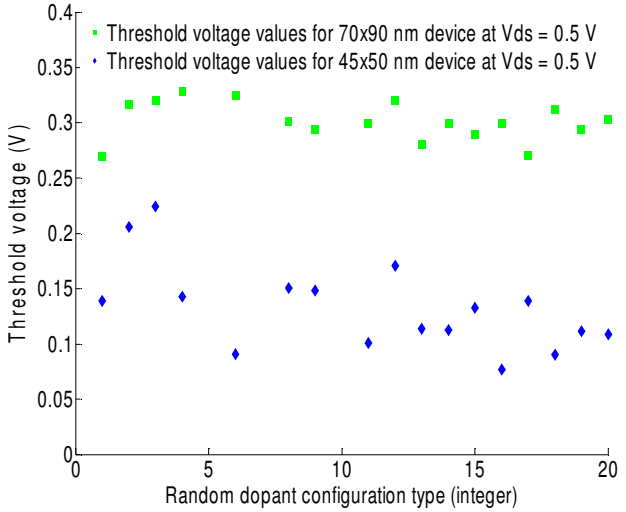

Figure 3: Threshold voltage distribution as a function of different random channel dopant configuration for the cases of 70×90 nm^2 and 45×50 nm^2 device.

Figure 4 shows the comparison of threshold voltage fluctuations percentages for the three trap positions, for the drain bias condition of 0.5V and for the cases of 70×90 nm^2 and 45×50 nm^2 device geometries. The trap positions for 70×90 nm^2 MOSFET device are 9 nm, 37 nm and 62 nm. The trap positions for 45×50 nm^2 MOSFET device are 7 nm, 23 nm and 37 nm. The results presented in this figure clearly reveal the impact of device area scaling on trap induced threshold voltage fluctuations. The source side threshold voltage fluctuations for the 45×50 nm^2 device is more than twice the percentage fluctuations in threshold voltage observed for 70×90 nm^2 device. The threshold voltage fluctuations for the three trap positions for 45 nm MOSFET falls more rapidly towards the drain when compared to the 70 nm MOSFET device due to higher drift velocity of carriers, driven by higher lateral electric field for 45 nm MOSFET, enabling them to surmount the trap's barrier.

Figure 5 shows the threshold voltage standard deviation as a function of inverse of the square root of the gate area as recorded for the two device dimensions and with and without trap's effect (for both the device dimensions, trap is positioned at the middle of the channel length). Also shown in the Figure is the analytical model [7] predicted σV_{th} trend used to compare with EMC simulation results. A more realistic trend line is also included in this Figure to illustrate the more stronger variation of σV_{th} with gate area scaling. The analytical model equation of [7] (RDF variation only) is tailored to within 0.00697V-0.00719V of actual EMC simulation extracted values of σV_{th} for RDF variation.

$$\sigma V_{th} = 3.19\times10^{-8}\left(\frac{t_{ox}^{\ 0.994} N_A^{\ 0.405}}{\sqrt{WL}}\right) \quad (1)$$

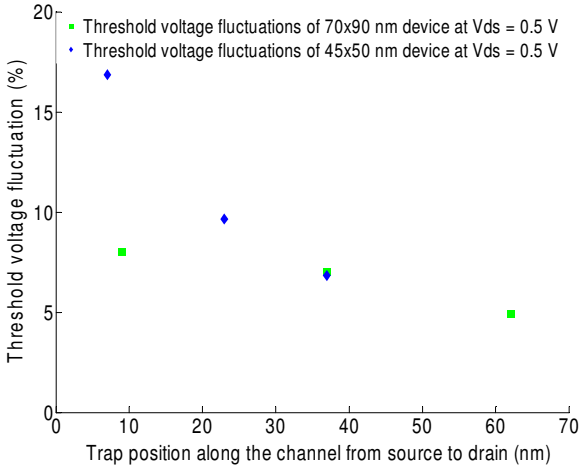

Figure 4: Threshold voltage fluctuations at three different interface trap positions showing the impact of device scaling for a 70×90 nm^2 and 45×50 nm^2 device.

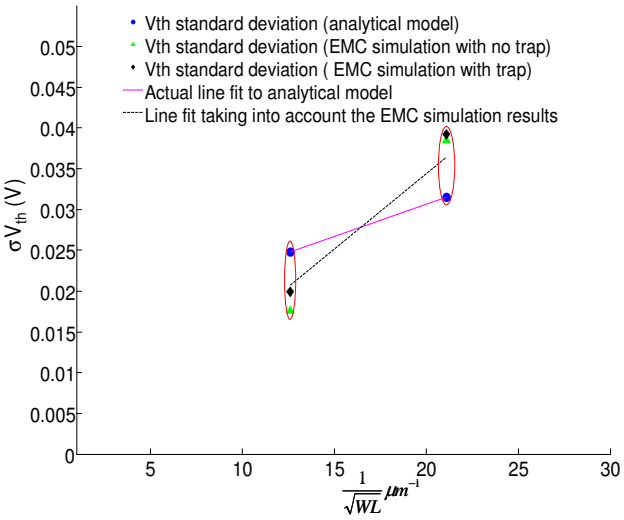

Figure 5: Threshold voltage standard deviation as a function of inverse of square root of gate area showing the EMC simulation generated values for RDF only and with RDF+trap. The analytical model (1) predicted trend and a more realistic trend are also shown.

4 CONCLUSIONS

Random channel dopant fluctuations and random channel interface trap induced threshold voltage

fluctuations reveal important observations with regard to device scaling into sub-100 nm gate length dimensions. A comparative analysis enabled us to reach the viewpoint that while aggressively scaled devices suffer substantially for threshold voltage degradation in the presence of a trap, for a larger gate area device, RTN/RTS impact is more tolerable when the applied drain bias is sufficient to move the carriers with enough drift velocity across the channel at threshold condition. These effects are summarized in the Figures 1-4. Finally the important σV_{th} trend as a function of $\frac{1}{\sqrt{WL}}$ has been examined taking account of EMC device simulation results which included RDF and random trap's effect at the interface along the channel.

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