Suppression of Variability in Metal Source/Drain SOI MOSFET with Partial Buried Oxide and δ-doping

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ABSTRACT

Recently, metal source/drain (S/D) dopant-segregated Schottky barrier (DSSB) SOI MOSFET has attracted the attention of researchers due to its planar structure, CMOS compatibility and reduced S/D series resistance at thin silicon film. However, at nanoscale the inhomogeneity in Schottky barrier height and segregation length increases the device parameter variations. To alleviate this problem, in this work it has been shown that, employing partial buried oxide only under the metal S/D and δ-doping under the channel suppresses the variability in DSSB SOI MOSFET. In addition, for the first time, the impact of variability on digital/analog circuit performance metrics such as leakage power dissipation, intrinsic gate delay, cut-off frequency and open-circuit voltage gain has been investigated.

Keywords: Schottky barrier, variability, partial buried oxide, SOI MOSFET, digital/analog circuit performance

1 INTRODUCTION

Due to CMOS compatibility, low-source/drain (S/D) series resistance, improved scalability and better short-channel effect immunity dopant-segregated Schottky barrier (DSSB) silicon-on-insuator (SOI) MOSFET has been widely studied as a potential work horse for meeting the challenges at the end of semiconductor technology roadmap [1]-[6]. However, it has been shown that, employing dopant-segregation during silicidation leads to an increase in the device parameter variations and the inhomogeneity in Schottky barrier (SB) height (Φ_{bn}) affects the saturation threshold voltage (V_{TSAT}) of the device [7]-[9]. To address this problem, in this work it has been shown that, employing partial buried oxide and p-type δ-doping under the epitaxial channel of DSSB SOI MOSFET suppresses the device parameter variations induced by the process fluctuations in dopant segregation length (L_{DSL}), Φ_{bn} and silicon film thickness (T_{Si}) of the device.

Furthermore, the impact of variability on digital/analog circuit performance metrics such as leakage power dissipation ($I_{OFF}.V_{DD}$), intrinsic gate delay ($C_G.V_{DD}/I_{ON}$), cut-off frequency (f_t) and open-circuit voltage gain (A_{Vopen}) of DSSB SOI and the proposed δ-doped partially-insulated DSSB (DSSB Pi-OX-δ) MOSFETs has been investigated. Here, I_{OFF}, I_{ON}, C_G and V_{DD} represents the off-state leakage current, on-state drive current, gate capacitance and the supply voltage respectively.

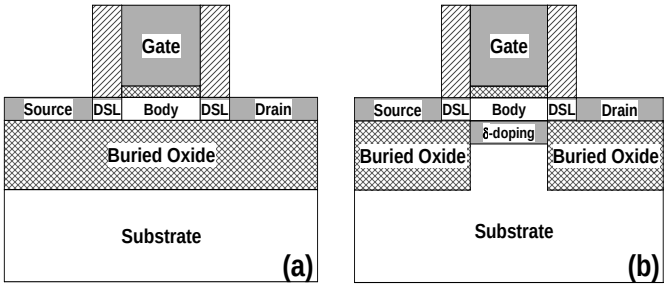

Figure 1: (a) DSSB SOI and (b) DSSB Pi-OX-δ MOSFETs used in MEDICI simulations.

The organization of rest of the paper is as follows, Section 2 presents the device structures and the simulation methodology used in this work whereas Section 3 presents the detailed discussion on process induced device parameter variations and the impact of variability on digital/analog circuit metrics of DSSB SOI and DSSB Pi-OX-δ MOSFETs. Finally the conclusion is given in Section 4.

2 DEVICE STRUCTURES AND SIMULATION SETUP

The device structures and the parameters used in the MEDICI simulator [10] are shown in Fig. 1 and Table 1 respectively. The range of physical gate length (L_G) and the gate oxide thickness have been considered as per the requirements specified in ITRS-2009 [6]. The segregation length i.e. L_{DSL} has been considered as the distance between the metal-semiconductor (M-S) junction edge and the p-n junction edge where the doping in the segregation layer drops to 1×10^{15} cm^{-3}.

Since carriers in the channel are mainly transported due to drift-diffusion and at the M-S junction are due to tunneling, both drift-diffusion and SB tunneling models have been incorporated along with the mobility models. Further, to extract the analog figures of merit for both DSSB SOI and proposed DSSB Pi-OX-δ MOSFETs, the small-signal ac analysis by considering source as a ground terminal has been carried out [3]-[5]. In order to study the impact of process fluctuations in L_{DSL}, Φ_{bn} and T_{Si} different sets of devices with varying L_{DSL}, Φ_{bn} and T_{Si} have been simulated. The standard deviations (σ) obtained in each set of 25 devices for L_{DSL}, Φ_{bn} and T_{Si} are 1.8 nm, 0.06 eV and 1.3 nm respectively [5]. The detailed fabrication steps of the proposed DSSB Pi-OX-δ MOSFET can be seen in [3].

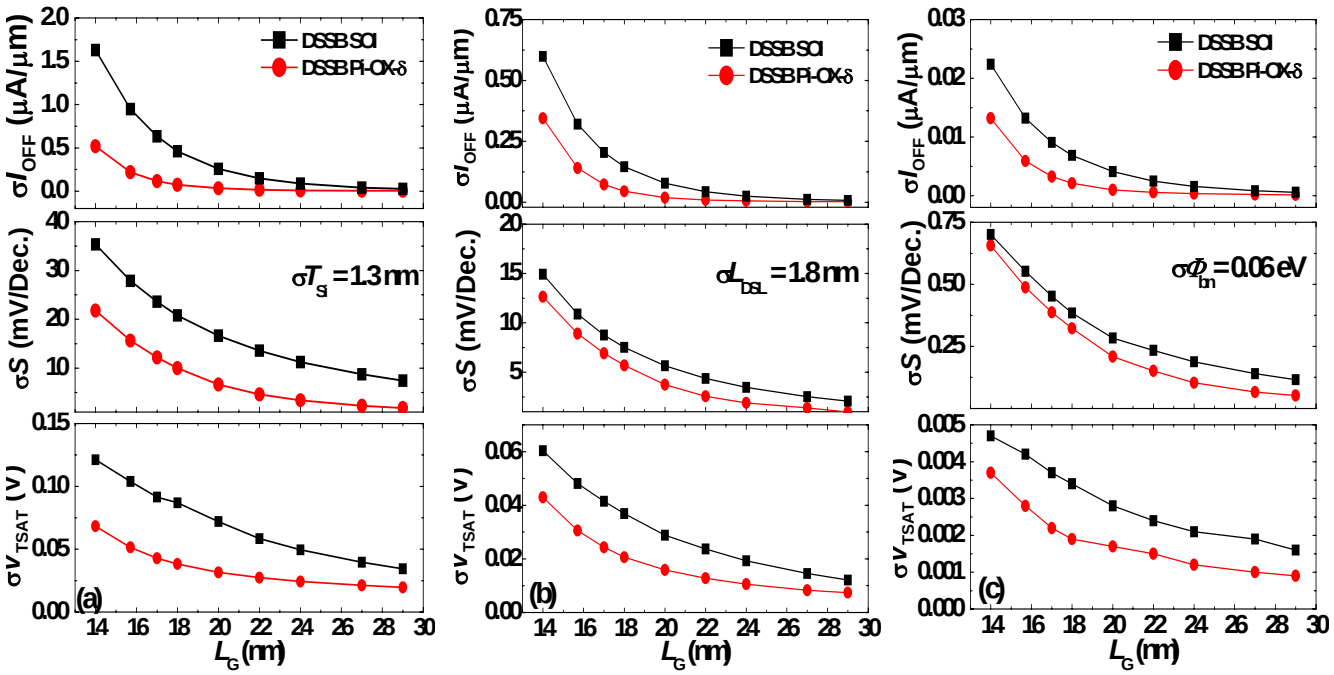

Figure 2: Variation of σV_{TSAT}, σS and σI_{OFF} with physical gate length showing the impact of process induced fluctuations in (a) T_{Si}, (b) L_{DSL} and (c) Φ_{bn} of DSSB SOI and DSSB Pi-OX-δ MOSFETs.

Parameter	DSSB SOI	DSSB Pi-OX-δ
Physical gate length (nm)	variable	variable
Gate oxide thickness (nm)	1	1
Nominal Silicon film thickness (nm)	8	8
Buried oxide thickness (nm)	50	50
Substrate thickness (nm)	100	100
Spacer thickness (nm)	10	10
Doping in segregation layer (cm^{-3})	1×10^{20}	1×10^{20}
Channel doping (cm^{-3})	1×10^{15}	1×10^{15}
Substrate doping (cm^{-3})	1×10^{15}	1×10^{15}
Nominal dopant-segregation layer length (nm)	11	11
Nominal electron SB height (eV)	0.3	0.3
Nominal hole SB height (eV)	0.82	0.82
p-type δ-layer doping density under the channel (cm^{-3})	#	3×10^{18}
Thickness of p-type δ-layer under the channel (nm)	#	10
Supply voltage (V)	1	1
Saturation threshold voltage (V)	0.2	0.2

Table 1: Device parameters used in the MEDICI simulations.

3 RESULTS AND DISCUSSION

3.1 Process Induced Device Parameter Variations

The comparison of standard deviations in V_{TSAT}, subthreshold swing (S) and I_{OFF} as a function of L_G for DSSB SOI and the proposed DSSB Pi-OX-δ MOSFETs is shown in Fig. 2. The V_{TSAT} is defined as the gate voltage at which

$$I_D = 1\times10^{-7}\left(\frac{W}{L_G}\right), \quad (1)$$

where W = 1 μm is the width of the transistor. Further, S has been extracted at V_{DS} = 1 V whereas I_{OFF} has been extracted at $V_{DS} = V_{DD}$ = 1 V and $V_{GS} = V_{GOFF}$ = 0 V.

From Fig. 2 it can be clearly seen that, the variations in V_{TSAT}, S and I_{OFF} due to T_{Si}, L_{DSL} and Φ_{bn} fluctuations in both DSSB SOI and DSSB Pi-OX-δ MOSFETs are relatively small when L_G is more than 20 nm. However, when L_G is scaled down the parameter variations become more significant. Further, due to exponential dependence of device characteristics on T_{Si} [11], the variations in V_{TSAT}, S and I_{OFF} due to T_{Si} fluctuations are larger in comparison to L_{DSL} and Φ_{bn} fluctuations. Moreover, since the presence of buried oxide opening under the channel reduces the stringent requirement of uniformity in thin Si film and the screening effect due to p-type δ-doping reduces the random dopant fluctuations [11]-[12], the parameter variations in scaled DSSB Pi-OX-δ MOSFET are significantly low as compared to scaled DSSB SOI MOSFET.

3.2 Impact of Variability on Digital/Analog Circuit Performance Metrics

In order to study the impact of process induced fluctuations in physical device parametres (T_{Si}, L_{DSL} and Φ_{bn}) on digital/analog circuit performance metrics such as ($I_{OFF}.V_{DD}$), ($C_G.V_{DD}/I_{ON}$), f_t and A_{Vopen} the standard deviations in I_{OFF}, I_{ON}, C_G, A_{Vopen} and the short-circuit current gain (A_{ishort}) has been recorded. Here, I_{ON} has been extracted at $V_{DS} = V_{DD}$ and $V_{GS} = V_{GOFF} + V_{DD}$ whereas C_G has been extracted by summing the parasitic capacitances namely gate-to-source (C_{gs}) and gate-to-drain (C_{gd}) of the MOSFETs. The C_{gs} and C_{gd} are defined as [13]

$$C_{i,j} = \frac{Q_i}{V_j}, \quad (2)$$

where i = g and j = s, d. and have been extracted by applying $\frac{dQ}{dV}$ method of the MEDICI simulator at drain bias of 1 V. The cut-off frequency i.e. f_t has been extracted from the A_{ishort} which is defined as [14]

$$A_{ishort} = \frac{Y_{21}}{Y_{11}}, \quad (3)$$

whereas the open circuit voltage gain i.e. A_{Vopen} is defined as [14]

$$A_{Vopen} = \frac{Y_{21}}{Y_{22}}. \quad (4)$$

From Fig. 3(a)-(d) it can be seen that, although σA_{Vopen} in the proposed DSSB Pi-OX-δ MOSFET is larger in comparison to DSSB SOI MOSFET, the ~77%, ~44% and ~70% reduction in $\sigma(I_{OFF}.V_{DD})$, $\sigma(C_G.V_{DD}/I_{ON})$ and σf_t respectively makes the proposed DSSB Pi-OX-δ MOSFET suitable for fluctuation resistant digital/analog circuits.

In addition, from Fig. 3(a) it can be seen that, in comparison to σT_{Si}, the standard deviation in $I_{OFF}.V_{DD}$ due to $\sigma\Phi_{bn}$ and σL_{DSL} is lower. Further, from Fig. 3(b)-(c) it can be seen that, the standard deviation in ($C_G.V_{DD}$)/I_{ON} and f_t due to σL_{DSL} is lower in both the devices. From these results, it can be clearly seen that, among all the process induced fluctuations (i.e. $\sigma\Phi_{bn}$, σT_{Si} and σL_{DSL}) the intrinsic digital/analog circuit performance of DSSB SOI MOSFET is mainly affected by the fluctuations in T_{Si}. Thus, although the fluctuations in Φ_{bn} and L_{DSL} of DSSB SOI MOSFET can leads to an increase in the device parameter variations, the main source of variability of this device is the T_{Si} fluctuations, which can be significanly suppressed by employing the partial buried oxide and δ-doping under the channel of this device.

4 CONCLUSIONS

In this work, a comprehensive study on process induced variability in DSSB SOI MOSFET has been carried out by using the two dimensional MEDICI simulator. It has been shown that, employing partial buried oxide only under the S/D and p-type δ-doping under the epitaxial channel of

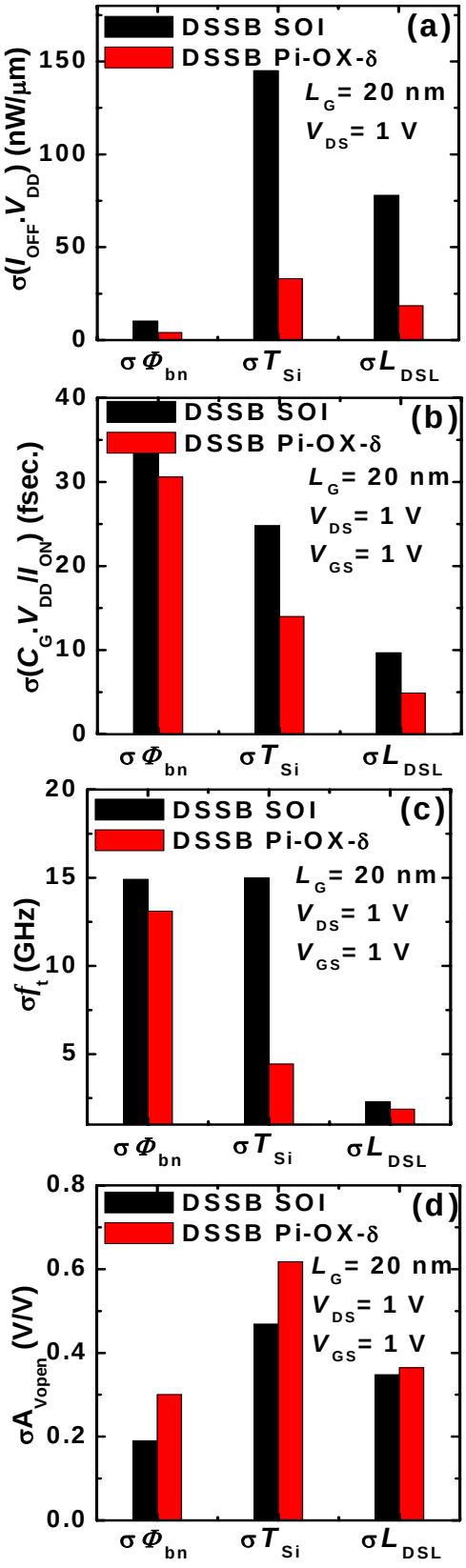

Figure 3: Comparision of standard deviation in (a) $I_{OFF}.V_{DD}$ (b) ($C_G.V_{DD}$)/I_{ON} (c) f_t and (d) A_{Vopen} due to process induced fluctuations in Φ_{bn}, T_{Si} and L_{DSL} of DSSB SOI and DSSB Pi-OX-δ MOSFETs.

DSSB SOI MOSFET suppresses the process induced variability of this device. The impact of variability on digital/analog circuit performance metrics of DSSB SOI and the proposed DSSB Pi-OX-δ MOSFETs has also been investigated. It has been found that, although σA_{Vopen} in the proposed DSSB Pi-OX-δ MOSFET is larger in comparison to DSSB SOI MOSFET, the significant reduction in $\sigma(I_{OFF}.V_{DD})$, $\sigma(C_G.V_{DD}/I_{ON})$ and σf_t makes the proposed device suitable for fluctuation resistant digital/analog circuits.

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