A New Method for Vertical Growth of Silicon Nanowire in the Vapor-Liquid-Solid (VLS) Process

[*]Y. J. Kim, [*]D. Suh, [**]M. L. Lee and [**]H. J. Ryu

[*]Creative and Challenging Research Division and
[**]Next-Generation Display research Division,
Electronics and Telecommunications Research Institute
138 Gajeomg-no, Yuseong-gu, Daejeon, 305-700l, Korea
junkim@etri.re.kr, dwsuh@etri.re.kr, mllee@etri.re.kr, and hjryu@etri.re.kr

ABSTRACT

A series of silicon nanowires were grown uisng the vapor-liquid-solid (VLS) process in an effort to produce nanowires aligned vertically to the subsrate by varying the chemical properites that are in contact with silicon substrate. In contrast to the conventionally used method in which $SiCl_4$ is used to remove silicon oxide and to produce vertical silicon nanowires, in this report chemical modification was carried out to produce vertical silicon nanowire. Gold nanoparticles (60 nm and 80 nm) were used as catalyst. Poly-L-lysine (PLL) was used in between the gold nanoaprticles and silicon substrates. The attchment of the gold nanoparticles on the silcon substrate was confimred by SEM images. The oxide layer on silcon surface was either treated with buffered oxide etchant (BOE) or HF. In another case some chemical modification was done on PLL before applying on the silicon surface. The growth of the nanowrie was processed using the temperature below 550 °C. Although not in perfect vertical, the nanowires treated with BOE and HF showed tendency toward vertical direction. Better control in the vertical direction was accomplished with the nanowires produced using the chemically modifed PLL.

Keywords: nanowire, vapor-liquid-solid, gold nanoparticel, and vertical.

1 INTRODUCTION

Due to the potential impact of the nanotechnology application, much interest has steadily grown in nanowires. Considering that silicon is the major material in the electronics, silicon nanowire is expected to play more impactful role than nanowires based on other materials. Vapor-liquid-solid (VLS) process is the most widely used method for the silicon nanowire synthesis. In the VLS method gold is the major catalyst for the growth of silicon nanowire. In the phase binary diagram of gold and silicon, the eutectic point is formed at 363 °C which is much lower than the melting point of pure gold and silicon. In order to grow silicon nanowire, conventionally thin layer of gold is coated on a silicon surface. Small islands of gold are formed at the silicon surface by increasing temperature. At an elevated temperature SiH_4 is absorbed into gold which is in liquid form. Further supply of SiH_4 facilitates oversaturation of Si on the liquid mixture of gold and silicon. The oversaturated silicon starts to precipitates and at the bottom the silicon starts to grow. However since this method provides nano-gold island with varying sizes, which directly results in silicon nanowires with different nanowire thickness.

Another important factor in the growth of silicon nanowire is the direction of the nanowires. It has been reported that the native oxide on the surface of the silicon hinders the vertical growth of silicon nanowire. In the present VLS method for the growth of silicon nanowire, $SiCl_4$ is used to remove the native oxide and to provide environment for the vertical growth. However the use of $SiCl_4$ in VLS process has two major disadvantages[1, 2] ; (1) need for high process temperature ranging from 800 °C to 1000 °C, and possibility of damage to the substrates and the equipment due to HCl produced from the reaction of $SiCl_4$ with H_2.

We present a new facile method for vertical growth of the silicon nanowire (Si NW) that obviates the need for $SiCl_4$ in vapor-liquid-solid (VLS) process. Also we used gold nanoparticles of uniform size in order to produce nanowires with uniform nanowire thickness. By using some chemically modified polymers we were able to produce vertically aligned silicon nanowires without using $SiCl_4$ at low temperature range, below 550 °C. The vertically-grown silicon nanowires are useful building blocks for electronic and photovoltaic devices. This new method for vertical nanowire array that does not the need $SiCl_4$ and that makes possible of using lowered process temperature, would constitute a very impactful leap toward producing high quality silicon nanowires in more efficient process.

2 RESULTS AND DISCUSSION

A series of experiments were carried out by varying the treatment conditions of the silicon wafer and poly-L-lysine (PLL), and temperature of the nanowire growth. In general

silicon wafers were washed with a series of solvents with at least 5 minutes of sonication. The chemically treated PLL was coated on the silicon surface and gold nanoparticles were positioned the on the silicon surface. In order to compare the directional behavior of the silicon nanowire growth, gold dots and lines in the micron dimension were also used.

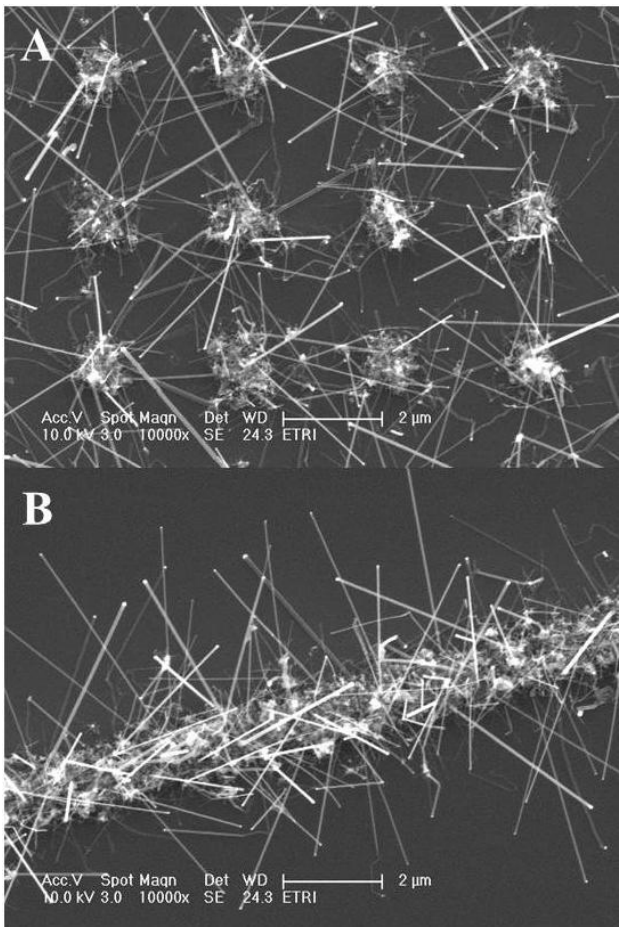


Figure 1. SEM images of the silicon nanowires grown on the patterned gold of (A) the dot shape and (B) the line shape.

Figure 1 shows the Si NWs grown on micron-size dots and lines of gold patterned on Si wafer. Multiple nanowires were grown even in one dot with no control over growth direction for the both the dot and line shape. It is interesting to observe that on the same gold surface multiple nanowires were grown. However this random mode in the nanowire growth is hard to find any usefulness in the future application of electronic or optical applications. In an effort to be able to control such random mode of the nanowire growth, uniform size nanogold was used for the nanowire growth. Figure 2 shows SEM image of the Au NP (80 nm) positioned on Si wafer with every nanoparticle well separated from each other. In the hope of confining one nanowire for one gold dot, gold nanoparticles (Au NP) were anchored on Si wafer by placing PLL adhesive layer

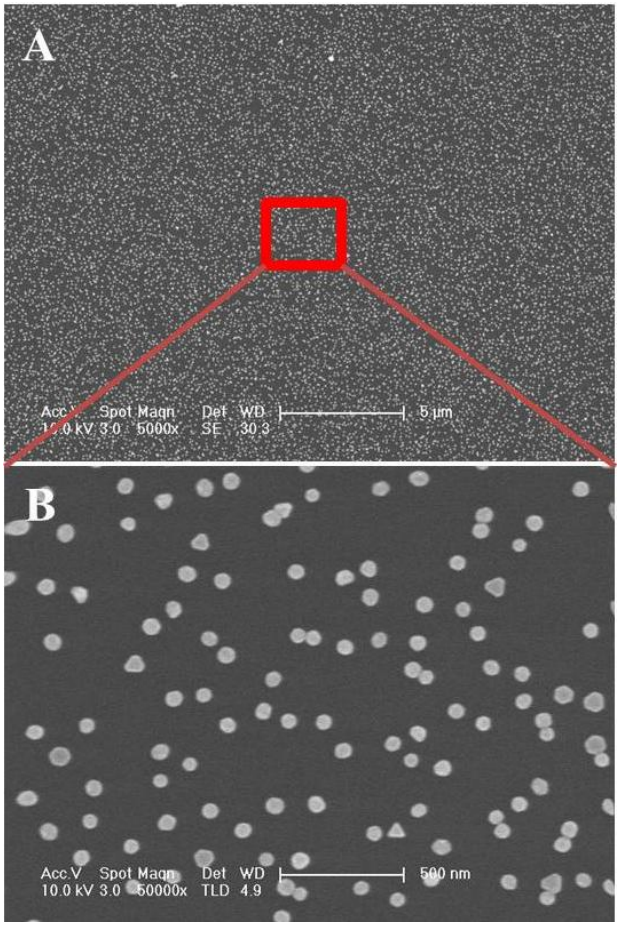


Figure 2. SEM image of the nanoparticle positioned on silicon substrate using poly-L-lysine layer.

between the nanoparticles and the wafer. It has been known that the positive property of PLL is the driving force for functioning as the adhesive between the silicon surface and the gold nanoparticles (figure 3). Since the silicon surface is coated with native oxide and the gold nanoparticle is formed by sitric acid the positively charged PLL can hold the gold nanoparticles fast to the silicon surface.

Figure 4 shows the Si NWs grown from Si wafers treated with no acid (A), with 2 % HF (B) and with buffered etchant oxide (BOE) (C). Generally the Si NWs grown from Au NPs showed better direction control and one nanoparticle is interpreted to have been involved in the growth of one nanowire. While the nanowires were grown in all the directions when gold dimension was in micron scale, a certain degree of control was found to be accomplished in the nanowires grown using nanoparticles. However among the nanowires for the nanoparticle, no appreciable amount of difference was observed in the direction control as can be seen from the figure 3. It turned out that prior treatment of silicon doesn't seem to be

affecting the growth direction whether the surface was treated with HF or BOE. Moreover untreated silicon surface ((A) in figure 4) produced nanowires that has almost same direction behavior with the treated silicon surface.

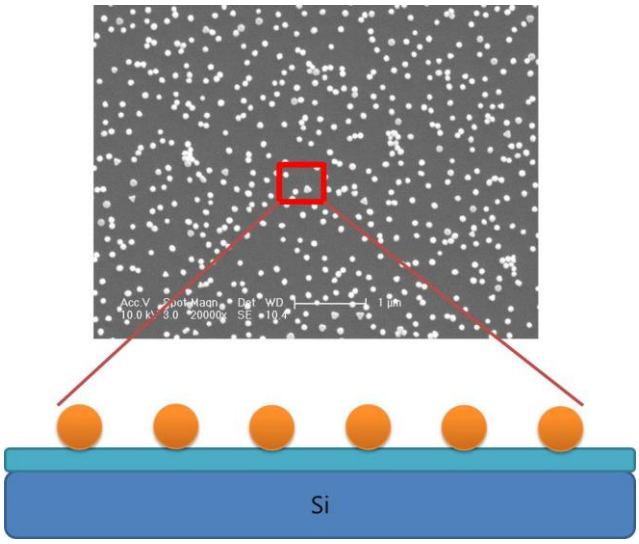
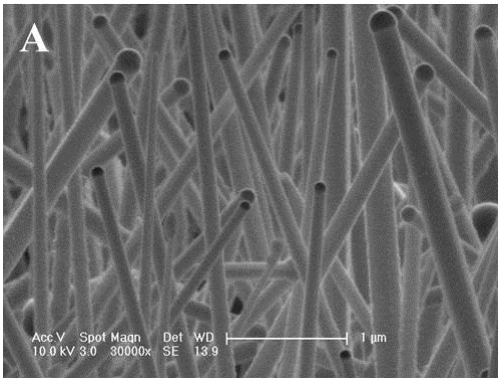


Figure 3. Schematic view of the gold nanoparticles positioned on the silicon surface suing poly-L-lysine.

In order to further control the growth direction of the nanowire, we used PLL treated with some chemical modification. Also nanowires were grown by varying the growth temperature. When 200 °C was used at the start of the nanowire growth, Si NWs were found to aggregate with crack-shaped surface. It is thought that the softening of PLL due to low temperature seems to have caused aggregation of Au NP and thus Si NW. Also use of low temperature may have led to carbonization of PLL as can be surmised from the surface crack. When 500 °C was used, highly aligned nanowires to the vertical direction was accomplished. It has been observed that the directionality of the nanowires was dependent on the degree of modification on PLL. Now we are working on fine-tuning the factors for nanowire growth hoping to find ways to ideally vertical silicon nanowires.



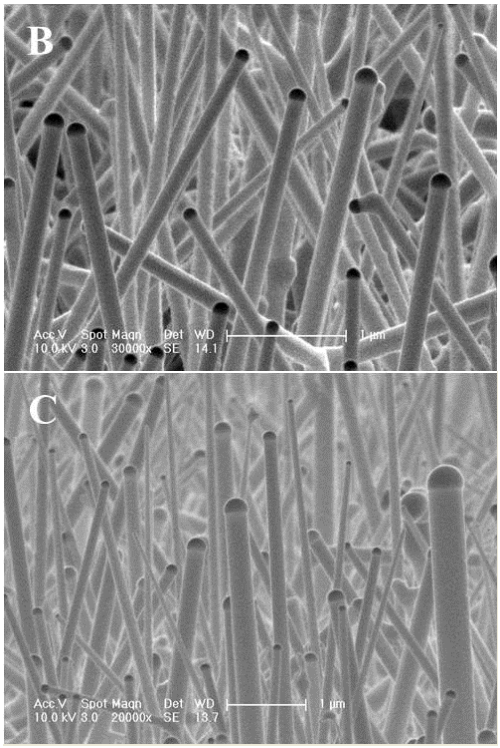


Figure 4. SEM images of the silicon nanowires grown on silicon wafers treated with (A) nothing (B) HF and (C) BOE.

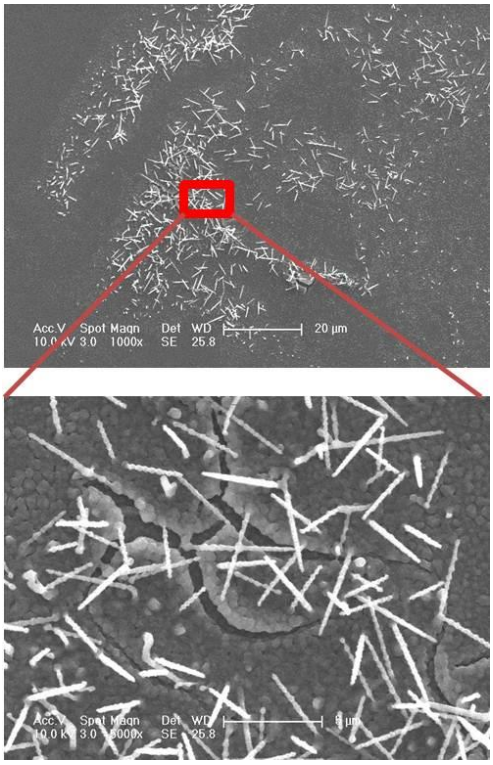


Figure 5. silicon nanowires grown on a chemically treated wafer with initial temperature of 200 °C.

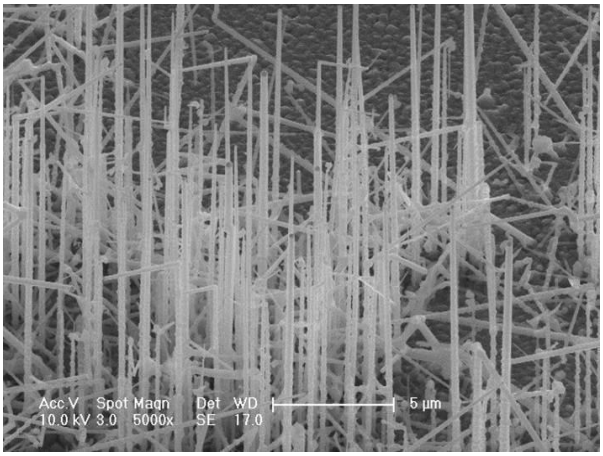


Figure 6. Silicon nanowires grown vertically using chemically treated PLL with initial temperature of 500 °C.

REFERENCES

[1] V. Schmidt, J. V. Wittemann, U. Gösele, Chem. Rev. 110, 361, 2010.

[2] A. I. Hochbaum, R. Fan, R. He, P. Yang, Nano Letters 5, 457, 2005.