Physics based Analytical Model for a Pocket Doped p-n-p-n Tunneling Field Effect Transistor

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ABSTRACT

This work presents a simple and device physics oriented analytical model based on the carrier concentration approach to study the various device electrostatic parameters of a halo doped (or tunnel source MOSFET) p-n-p-n Double gate Tunnel Field effect transistor (DG-TFET) architecture. The model takes into account the effect of drain-source voltage at the tunneling junction accurately at lower values. The most important parameter in the designing of a p-n-p-n TFET is the pocket doping and pocket width which can be optimized using the proposed modeling approach which takes into account the depletion width at the tunneling junction. The results obtained from analytical expressions are compared with device simulator results and in good agreement.

Keywords: Band to Band Tunneling (BTBT), Depletion Width, DG-TFET, Halo doped, p-n-p-n

1 INTRODUCTION

For last few years, the research focus has been shifted to explore alternative device designs and architectures which can overcome the major issue related to MOSFET scaling limitations [1]. Tunnel FET working on the principle of band-to-band tunneling mechanism has come up as a promising candidate with advantages of going below the limitation of 60mV/decade sub-threshold slope [2], and lower leakage current and thus capable of reducing the power consumption and achieving energy efficient fast switching transistors [3], [4]. The basic TFET architecture is that of a reverse biased gated p-i-n diode. Various design optimizations and modifications have been proposed to enhance the performance of TFET to make it a competing technology for future technology nodes [5], [6]. One of the techniques reported in this regard is creating a heavily doped pocket implantation between the source and channel region [7]. Pocket doped (also known as p-n-p-n TFET or tunnel source MOSFET) is a promising TFET architecture because of its advantage of steep band bending and reduction of barrier width to enhance the electric field at the tunneling junction and thus improving the tunneling current.

There have been several experimental as well as simulation studies, but efforts are required in the direction of development of compact analytical model based on device physics and working principle. This work is an attempt to model the device electrostatics of a pocket doped p-n-p-n TFET architecture by following a simple and physics based approach to obtain efficient and accurate expressions governing the device behavior. Since, working principle of Tunnel FET is mainly governed by the tunneling junction, accurately modeling the electrostatics at the tunneling junction is the most crucial factor, as this region determines the current component in the device.

2 DEVICE ARCHITECTURE AND SIMULATION

Fig. 1 Two dimensional cross section of Double gate p-n-p-n TFET with Silicon film thickness $t_{si}=10\text{nm}$, gate oxide thickness $t_{ox} (\text{SiO}_2) =3\text{nm}$ channel length ($L$) = 45nm. A metal gate work function of 4.2eV is used. Source doping (p+) $N_p=1\times10^{20}\text{cm}^{-3}$, channel doping (p-) $N_i=1\times10^{19}\text{cm}^{-3}$ and drain doping (n) $N_d=5\times10^{18}\text{cm}^{-3}$. Pocket width ($L_p$)=4nm, Pocket doping (n+) $N_p=5\times10^{19}\text{cm}^{-3}$
The modeling scheme is based on carrier concentration approach [9], wherein, the electrostatics in the channel region is computed by evaluating electron concentration in the channel region. The electron concentration is maximum at the Si/SiO$_2$ interface and decreases as moving towards the channel center. This helps in obtaining a variable barrier width of the tunnel junction along the transverse direction in case of a conventional p-i-n TFET [10]. In order to model the p-n-p-n architecture, the device design and its working principle (fig. 2) is taken into consideration and the approach taken is mentioned below.

The pre-requisite for p-n-p-n TFET to work properly is the optimization of n+ pocket width and pocket doping and these values should be such that the pocket region is fully depleted. In case of p-n-p-n TFET, the major advantage lies in the reduction of barrier width of tunneling junction due to the presence of a heavily doped n+ layer between the source and channel region. As reported, if the optimized doping and pocket width are considered then the tunnel width can be approximated to pocket width only [7]. Using this assumption, the extension of the depletion width in the channel region is truncated to the pocket edge ($L_p$) only. Moreover, the doping and width values are chosen such that the depletion width (calculated using p-n junction analysis for the source and n+ pocket junction) on the n-side (pocket side) is nearly equal to the pocket width (i.e. 4nm). But, once channel is formed (moderate to strong inversion condition), the drain voltage starts appearing at the tunneling junction through inverted channel region. For low $V_{ds}$ values the electron quasi Fermi potential in the channel region remains almost constant so the influence of drain potential at the channel region is evaluated for different gate voltages. The data obtained for the $V_{ds}$ contribution to the channel potential at different $V_{gs}$ values is curve fitted to a 4$^{th}$ order polynomial which is then used for boundary condition at the pocket edge to account for the influence of drain voltage at the tunneling junction. Using this boundary condition, the depletion width extension inside p+ source, and at the source/pocket junction is solved using a p-n junction methodology, and added to pocket width to determine the total barrier width at the junction wherein the electrostatic parameters, i.e. potential, Electric field and energy band diagram at the junction varies as a function of both $V_{gs}$ and $V_{ds}$.

A 2D Poisson’s equation is solved in the channel region and an expression for potential is derived by using appropriate source and drain boundary conditions.

$$\frac{\partial^2 \phi}{\partial x^2} + \frac{\partial^2 \phi}{\partial y^2} = \frac{q}{\epsilon_{si}} \left( \phi - \phi_{ch} \right)$$

where $n_i$ is the intrinsic carrier concentration of the channel and $\Phi_{ch}$ is channel potential. The 1D surface potential can be expressed as follows

$$\lambda^2 \left( \frac{\partial^2 \phi_s}{\partial y^2} \right) + (V_{gs} - V_{fb} - \phi_s) = \frac{Q_{inv}}{C_{ox}}$$

where $\Phi_s$ is the surface potential, $Q_{inv}$ is the inversion charge density and $C_{ox} = \epsilon_{ox} \epsilon_{o} / t_{ox}$ is the gate oxide capacitance. $V_{fb}$ is flat band voltage, $\lambda$ is generalized scale length [11] expressed in terms of channel and gate oxide thickness and relative dielectric permittivity as

$$\tan \left( \frac{\pi_{ox}}{\lambda} \right) \tan \left( \frac{\pi_{si}}{2 \lambda} \right) = \frac{\epsilon_{ox}}{\epsilon_{si}}$$

The general solution of (2) is given as

$$\phi_s(y) = V_{gs} - V_{fb} - \frac{Q_{inv}}{C_{ox}} + A_1 \exp \left( \frac{-y}{\lambda} \right) + B_1 \exp \left( \frac{-(L-y)}{\lambda} \right)$$

The coefficients $A_1$ and $B_1$ are determined using the boundary conditions at the pocket/channel (n+/p-) junction and channel drain junction (p-/n+) junction expressed as

$$\phi_s(L_p) = \frac{kT}{q} \ln \left( \frac{N_p N_i}{n_i^2} \right), \phi_s(L+p+L) = \frac{kT}{q} \ln \left( \frac{N_n N_d}{n_d^2} \right) + V_{ds}$$

Using eq. 4

$$\frac{\partial^2 \phi_s}{\partial y^2} \left( \frac{L_p + L}{L_p} \right) = \frac{1}{L_p} \int_{L_p}^{L_p+L} \frac{\partial^2 \phi_s}{\partial y^2} \, dy$$

Using the value of $\left( \frac{\partial^2 \phi_s}{\partial y^2} \right)$ from eq. (6)), and

$$Q_{inv} = q \int_{0}^{L_p/2} n(x) \, dx$$

and $\phi_s$ (from 4) in eq. (2) to determine the equation for the electron concentration at the centre of the channel ($n_d$).
function of position \((x)\), gate-source voltage \((V_{gs})\) and drain-source voltage \((V_{ds})\). \(W_p(V_{gs}, V_{ds})\) and \(W_n(V_{gs}, V_{ds})\) are gate and drain voltage dependent depletion width extension in the p+ source and pocket/channel region (eq. 11, 12) since the p-n junction built-in potential taken to evaluate these two are \(V_{gs}, V_{ds}\) dependent. Since the contribution of \(V_{ds}\) at the junction depends on the state of the channel (i.e. weak, strong inversion), so it’s a \(V_{gs}\) dependent quantity. Electric field at the tunneling junction can be obtained by taking derivative of eq. 10 and energy band diagram at the tunneling junction can also be obtained from potential expression.

\[
W_n(V_{gs}, V_{ds}) = \sqrt{\frac{2\varepsilon_{si}N_a}{q} \left( \frac{1}{N_a} + \frac{1}{N_p} \right) (V_{bi} + V_{ds}(V_{gs}))} \quad (11)
\]

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\]

### 4 RESULTS AND DISCUSSION

Fig. 3 depicts the variation of electron concentration along the channel thickness for different values of gate source voltage \(V_{gs}\) for p-n-p-n DG-TFET. The electron concentration profile is parabolic with maximum at the Si/SiO\(_2\) interface, and minimum at the channel center because of strong gate voltage control near the surface and decreasing \(V_{gs}\) influence inside the channel. Potential profile at increasing gate voltage is shown in Fig. 4 (a), (b). As can be observed that the potential rises very sharply at the source/pocket junction due to reduced barrier width with the incorporation of n+ heavily doped pocket. For high \(V_{gs}\) (after inversion) significant band bending takes place with increase in \(V_{gs}\) and thus reducing barrier width and increasing band to band tunneling. There is a steep rise in potential at the tunnel junction, while it remains constant over a major part of channel length. For a fixed \(V_{gs}\) when \(V_{ds}\) increases the potential in the channel increases globally (since \(V_{ds}\) drops across it). The lateral electric field is shown in fig 4 (c), (d). The maximum field is obtained at source/pocket junction and the energy band bending (fig. 5) is also high and p-n-p-n TFET has low tunnel barrier width as compared to a p-i-n TFET.
5 CONCLUSION

A physics based simplified analytical model has been proposed for pocket doped (p-n-p-n) DG-TFET and compact analytical expressions are derived for its electrostatic parameters – energy bands, potential and electric field. The model takes into account the gate voltage and drain voltage dependence of depletion at the tunneling junction and can be useful for optimizing the width and doping of the pocket region for a p-n-p-n TFET.

6 REFERENCES